



## Go tell it on the mountain

"OK, I have brought tablets from the mountain here. I have given out the word. Just do it. And why should I add to this, when people haven't finished learning what I told them the first time?"

—"Miss Manners"  
Judith Martin on her updated book that now covers technologies, such as cell phones, which she says are no excuse for disrupting events or ignoring people, in *The Boston Globe*, May 11, 2005

## Kit eases high-voltage-design woes

By Warren Webb

**G**OAL SEMICONDUCTOR recently announced a plug-and-play development and evaluation system for its HVDAC200-4 quad, high-voltage,

9-bit, serially configurable voltage/current D/A converter with outputs as high as 200V. The HVDAC200 finds

use in applications requiring high-voltage control, such as electrostatic MEMS (micro-electromechanical-system)



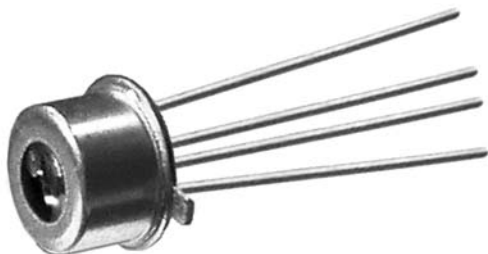
A new evaluation system for the HVDAC200-4 quad, high-voltage D/A converter features a local 8051 controller and PC-based demonstration and development software.

devices, test-and-measurement equipment, piezoelectric transducers, and high-voltage bias generation.

The development board features an 8051 microcontroller for communication with the PC-based demonstration software and to control the HVDAC200, adjustable voltage/temperature parameters, terminal blocks for high-voltage I/O, and a prototyping area. The UVK-HVDAC200-4 development kit comes with the evaluation board, a sample HVDAC200-4, CD-based user guides, source code, a serial cable, and a power supply. The kit also includes an 8051 compiler and debugger to develop custom programs for high-voltage control. The UVK-HVDAC200-4 costs \$250.

►Goal Semiconductor, [www.goalsemi.com](http://www.goalsemi.com).

## Receiver shoots fiber to TTL at 5 Mbps



For bridging the optical-link-to-TTL gap, the HFD3023 receiver supports bit rates to 5 Mbps with 850-nm fiber-optic signals.

Targeting use in data-communication and control applications, the 5-Mbps HFD3023 optical detector from Honeywell provides a TTL-compatible interface for short-distance, 850-nm fiber links and standard-diameter optical fibers. According to product-support manager Ian Anderson, the 5V device in a hermetic TO-46 package incorporates a monolithic IC with an integral photodiode and amplifier circuit, followed by an open-collector Schottky-transistor output. The \$14 (1000) unit has a typical sensitivity of  $2 \mu\text{W}$  ( $-27 \text{ dBm}$ ) and includes a mechanically centered, 0.024-in.-diameter microlens ahead of the 0.006-in.-diameter photodiode to optimize photon capture and consequent efficiency.—by Bill Schweber

►Honeywell International, [www.honeywell.com](http://www.honeywell.com).

## Bluetooth/UWB merger will take time

**T**HE ORGANIZATIONS SHEPHERDING Bluetooth and UWB (ultrawideband) have announced that they plan to merge their respective wireless-

communication technologies, but they released few technical details and allowed that end-user products sporting the combination are unlikely to appear for at least two years. The Bluetooth SIG (Special Interest Group) plans to collaborate with the WiMedia Alliance ([www.wimedia.org](http://www.wimedia.org)) and the Ultrawideband Forum to combine the two technologies. The objective, according to the Bluetooth SIG, is to build an architecture that allows Bluetooth-enabled devices to use high-speed UWB data rates to transfer large amounts of data, thus enabling high-quality video applications on portable devices.

"Two years is probably a best-case scenario," says Michael Foley, the SIG's executive director. "We have a lot of work to do in that area. Although the Federal Communications Commission has

approved UWB in the United States, it still has not received approval in Asia and Europe."

Freescale Semiconductor ([www.freescale.com](http://www.freescale.com)), which is quick to point out that it is the only chip supplier shipping commercial UWB silicon, voices its support for the effort. The company says that it will bring its experience with the MAC (media-access-control) layer that the IEEE 802.15.3 specifies and work with the Bluetooth SIG to develop a protocol-adaptation layer that works with Bluetooth protocols and profiles and Freescale's direct-sequence UWB technology.

"The big thing here is that the Bluetooth SIG is creating an architecture that allows users to employ other radios side by side with profiles it has published," says Martin Rofheart, director of UWB operations at Freescale. Consumers would have the choice

## Sense resistor's low TCR ensures consistency

A COMMON WAY to sense current in motors and power supplies is to use a low-value resistor in series with the load, but any drift in this resistor affects reading accuracy. The lead-free TLR-75ppm from KOA Speer Electronics features TCR (temperature-coefficient resistance) of 75 ppm/°C and is available in various resistance and power-handling combinations. The 2B, 2H, and 3AW sizes come in 1206, 2010, and 2512 cases and have 2- to 20-, 2- to 10-, and 3- to 8-mΩ resistances, respectively, with 0.5, 1, and 2W power ratings. All devices have 1% basic tolerance.

The price is 23 cents (1000).—by Bill Schweber

► **KOA Speer Electronics Inc**, [www.koaspeer.com](http://www.koaspeer.com).



The TLR-75ppm resistors combine low nominal resistance with low TCR for an effective load-current sensing.

of using whichever technology suited the application at hand. "There are a number of quick and cost-effective ways to achieve this goal," he says.

Foley notes that the faster data rates that UWB affords might also find use in Bluetooth-stereo headsets. With a

UWB-enabled design, a user could more quickly download an initial blast of music to the headphones than with a Bluetooth connection, presumably resulting in decreased power usage and longer battery life. Users will employ Bluetooth 2.0 radios to "speak with headsets, mice, and keyboards and UWB to talk to display-type devices and to replace cables," says Foley. UWB-enabled Bluetooth may also find use in the consumer-electronics space to connect DVD players to flat-panel televisions.—by Jeff Berman

► **Bluetooth Special Interest Group**, [www.bluetooth.org](http://www.bluetooth.org).

► **Ultrawideband Forum**, [www.uwbforum.org](http://www.uwbforum.org).

## DILBERT By Scott Adams



► The average percentage of employees using wireless-voice services within organizations increased on a year-over-year basis in all company sizes but especially at small-office/home-office companies, according to InStat/MDR.

## Silicon and quartz combine for advanced crystal entity

**C**RYSTALS ARE THE HEARTBEATS of today's synchronous circuits, but they face the challenge of reliably hitting and sustaining higher clock rates. According to Pericom/Saronix, its S1614XP

and S1613XP series of oscillators promises to improve that reliability by reducing the need for thin, fragile quartz elements that higher frequencies otherwise demand. Saronix Product Marketing Manager Brandon Ogilvie says, "The products use a thicker quartz blank paired with a non-PLL, patent-pending [upconversion] design." The company expects the new technology to reduce failure

rate by 75% and that its approach yields lower cost than and comparable performance with conventional, overtone-based legacy approaches.

The oscillators operate from 100 to 160 MHz. Computed phase jitter is 0.5 psec at a 1-sigma-rms level, and total stability is at least  $\pm 25$  ppm for the commercial range and  $\pm 50$  ppm for the industrial range. These specs make the device suitable for sensitive

applications, such as 1- and 10-Gbps Ethernet, Fibre, Fibre Channel, Serial Attached SCSI, and others. The 2.5/3.3V (30-mA) units are compatible with LVCMOS/LVTTL signals. They are available at standard, common operating frequencies in a 5 $\times$ 7-mm ceramic package, and prices begin at \$1.25 (10,000).

Not all applications need the Pericom unit's performance. Suiting those uses, Linear Technology's LTC6905xx silicon-oscillator family has typical jitter of 50 psec at 170 MHz and stability of 20 ppm/ $^{\circ}$ C but has lower current consumption: a maximum of 12 mA at 100 MHz. It is also, at 3 $\times$ 3 mm (SOT-23), small-

er than the Pericom device. It starts up in 100  $\mu$ sec—a critical factor in many low-power applications in which shut-down is the norm—and duty-cycle variation is just  $\pm 2.5\%$ . It is available with any of four master-clock frequencies of 80 to 133 MHz and includes circuitry to divide the clock by one, two, and four for a wide range of possible outputs. For factory- or field-adjustment situations, the IC is also available in a resistor-programmable version. It sells for \$1.15 (1000).

—by Bill Schweber

► **Pericom Semiconductor Corp.**, [www.pericom.com](http://www.pericom.com).

► **Linear Technology Corp.**, [www.linear.com](http://www.linear.com).

## SOC-hardware-debugging techniques extend to the system level

FOR SOC (SYSTEM-ON-CHIP) designs that are based on an embedded-processor platform, Novas Software is extending the reach of its debugging tools to cover a complete project originated in a system-level-design style. The company has a strong presence in hardware RTL (register-transfer-level)-based debugging with its Verdi product. The new offering, nESL, adds capabilities in the system and software areas. New features include transaction-debugging analysis, a SystemC compiler, visualization and tracing tools, and hardware- and software-debugging interfaces.

Novas aims nESL at complex designs using embedded-processor cores and bus-based communication. It provides a single environment with a common interface for debugging at all levels—from a system model through simulation-based verification to emulation of the complete system. It supports multiple languages, testbench and assertion code, mixed-signal analysis, hardware and software analysis on commonly used processor cores and buses, and protocol analysis.

Transaction analysis is a way of viewing communication within a design; nESL combines knowledge of a protocol

and signal data in an abstraction that presents information at the right level to provide an understanding of the system's bus-level behavior. The software simplifies complex device operation that engineers cannot easily understand from signal behavior alone. The company gained some of the protocol information through a partnership with Spiritech ([www.spiritech.com](http://www.spiritech.com)). An open transaction interface assists with capture and storage of this data. Modeling of C, C++, and SystemC allows both hardware and software views of a system. The software extracts hardware attributes from SystemC and presents the details in a separate window. It models software interactions in parallel, and users can study them in a familiar software-debugging style.

Users can then link multiple software environments, such as the ARM Realview debugger, into a hardware/software co-debugging environment. Novas says that this package covers all of the diverse methodologies that designers are using for debugging in the emerging system-level-design flow. Novas Software offers nESL as an option to the Verdi package; prices start at \$6000 for an annual license.—by Graham Prophet, *EDN Europe*  
**Novas Software**, [www.novas.com](http://www.novas.com).

► According to the Pew Internet and American Life Project, 8% of US citizens living in homes with Internet access don't use the Internet.

# Sign-off power network and electromigration-analysis tool decrease delay from voltage drop

**S**YNOPSYS HAS COMBINED static- and dynamic-timing-analysis technologies to create PrimeRail, a tool it bets will become the sign-off tool for gate-level power-network analysis and transistor-level EM (electromigration) analysis. Rajiv Maheshwary, senior director of sign-off and power products at Synopsys, says that, as voltage

drop becomes more common in large designs, it is having a greater impact on overall performance of ASICs and SOCs (systems on chips).

“Voltage drop is an increasing part of overall delay,” says Maheshwary. “At 90-nm processes, 10% of overall delay is a result of voltage drop, and, at 65 nm, it can be as much as 15%. A few years ago when signal integrity started to impact overall timing, full-chip sign-off tools for signal integrity emerged. Now, customers need such a tool for voltage drop.”

Maheshwary says that, thus far, the traditional static- and dynamic-timing-analysis tools have been inadequate for full-chip sign-off. Traditional gate-level static-power- and EM-analysis products, including the company’s AstroRail, are not thorough enough for use in full-chip sign-off because they neglect dynamic effects, such as on-chip decoupling capacitance and package parasitics. Similarly, gate-level dynamic-analysis

tools cannot analyze transistors, especially analog and memory, commonly in SOCs. And, says Maheshwary, dynamic transistor-level tools, such as Synopsys/Epic’s RailMill, are too slow and cannot do full-chip analysis.

To overcome the shortcomings of traditional tools and create a tool thorough enough for full-chip sign-off, Synopsys gives PrimeRail a hybrid static- and dynamic-timing-analysis engine. PrimeRail also includes a built-in RLC (resistance, inductance, and current)-extraction engine from StarRCXT, a kernel PrimeTime static timer for peak power or “vector-free analysis,” HSpice technology for characterizing standard-cell libraries, and NanoSim technology for modeling memories. For power-network sign-off analysis, users precharacterize standard-cell libraries and memory blocks and then run either RC or RLC on-chip extraction and RLC extraction on the package, all with PrimeRail. De-

signers then use PrimeRail for vector-based or vector-free power-rail analysis. For vector-free mode, Synopsys uses a PrimeTime kernel that looks at peak-power analysis based on the IC design’s switching activity, which PrimeRail then uses for dynamic rail analysis.

After dynamic analysis, PrimeRail generates voltage-drop and EM maps. “Once you do the dynamic voltage-drop analysis, you pass instance-specific voltage-drop information onto PrimeTime SI [signal integrity], which then does concurrent analysis of timing, signal integrity, and voltage drop,” says Maheshwary. For one beta customer, PrimeRail within eight hours analyzed a 20 million-gate design with 400 memories and IP (intellectual property) in a 130-nm process, and, for another beta customer, the product in just more than five hours, analyzed an 8 million-gate design with 100 memories and IP.

PrimeRail does not yet share ECO (engineering-change-order) data with tools further up in the flow. The company is working on integrating the tool with Synopsys’ recently announced IC Compiler to ease the implementation of corrections. The company is also looking at integrating it with its JupiterXT floorplanner in the hope of helping users gauge the impact of voltage drop on overall timing early in the layout process. The tool will likely

see its widest use as a sign-off tool for full-chip, mixed gate- and transistor-level design, but it also analyzes transistor-level voltage drop and EM tools in memory blocks. “A lot of IDMs [integrated-device manufacturers] have in-house memory compilers, and now they can use PrimeRail to ensure what comes out of the compiler is immune to EM effects,” says Maheshwary. For transistor-level blocks, users run extraction and use the NanoSim to create memory models. PrimeRail then runs in dynamic analysis with package parasitics. A beta customer in 9.5 hours ran EM analysis on a 4-Mbit SRAM with 12 million transistors in 90-nm silicon.

Maheshwary says that EM analysis is not yet a problem for standard-cell design. “We are seeing EM issues in memory cells, but for standard cells it may take some time. A lot of the IDMs we work with have homegrown approaches that look at current densities and measure whether traces are thick enough,” he says. “That is going to have to change over time, and we are addressing it before it becomes a mainstream problem.” PrimeRail is in limited production, and the company expects to offer it for general availability in September. The price for the tool starts at \$172,000 for a one-year subscription.

—by Michael Santarini  
► **Synopsys**, [www.synopsys.com](http://www.synopsys.com).

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► According to two surveys from the Pew Internet and American Life Project, 8 million US adults say they have created blogs. Blog readership jumped 58% in 2004 and now stands at 27% of Internet users.

# Processor and tools support dynamic reconfiguration

**D**YNAMICALLY RECONFIGURABLE silicon-sharing enables designers to implement a design with a smaller processor and possibly with lower power consumption than a fixed-function processor device. Atmel's FPSLIC (field-programmable system-level IC) II combines an 8-bit AVR processor core with an on-chip SRAM-based FPGA that enables multiple interfaces, peripherals, and coprocessors to share the same FPGA silicon at different times during application operation. Atmel's Reconfiguration Designer and Temporal Designer back-end EDA tools automate the im-

plementation, timing, and control of the silicon-sharing process.

The SRAM-based FPGA has not been the main obstacle to supporting dynamic silicon-sharing; rather, before the availability of these tools, designers would manually ensure that they had loaded the correct function into the FPGA at the correct time and that functions did not incorrectly load atop each other. The FPSLIC II employs a configuration controller, two DMA controllers, a dedicated FPGA-to-AVR interface, and a "virtual socket" in the FPGA portion of the

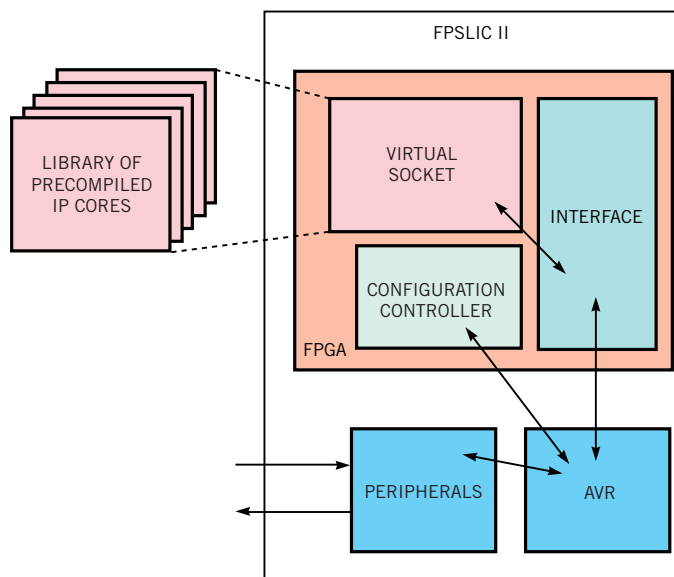
programmable SOC (system on chip) to enable the tools to automate reconfiguring the FPGA. Libraries containing previously designed peripherals, interfaces, and coprocessors load into the virtual socket to populate the FPGA. The FPSLIC II consumes 50  $\mu$ A in standby and 2 to 3

mA/MHz during operation.

Atmel provides a library of reference designs that includes Ethernet, memory, SPI, secure digital I/O, a multimedia card, DMA, speech synthesis, ADPCM (adaptive differential-pulse-code modulation), audio-codec interfaces, and DES (Data Encryption Standard)/triple-DES algorithms. FPSLIC II-family devices are available now at prices ranging from \$5 to \$15 (10,000) and FPGA densities of 256 to 2300 core cells in lead-free, 144-pin TQFP and 256-ball BGA packages.

—by Robert Cravotta

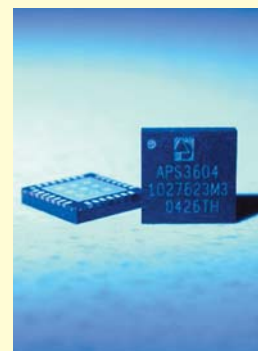
►Atmel, 1-408-441-0311, [www.atmel.com](http://www.atmel.com).



The on-chip configuration controller, DMA controllers, dedicated FPGA-to-AVR interface, and "virtual socket" in the FPGA portion of the programmable SOC enable the tools to automate the safe reconfiguration of the FPGA during operation.

## SMT DEVICE PAINLESSLY PERFORMS 1-GHz SPLITS

Set-top boxes driving multiple tuners need to split the input signal; the Anadigics APS3604 active splitter simplifies the task. This device, with a 75 $\Omega$  balanced RF input, accepts 50-MHz to 1-GHz signals and yields three balanced RF outputs. The 5V unit has a typical noise figure of 4.8 dB and maximum gain of 5 dB, thus



Take one RF signal in and get three signals out without attenuation, using the APS3604 1-GHz active splitter.

eliminating the need for separate front-end gain at the tuner. Typical current consumption is 175 mA for this \$3.90 (1000) product.

—by Bill Schweber

►Anadigics Inc, [www.anadigics.com](http://www.anadigics.com).

►A recent consumer survey from InStat/MDR found that more than half of respondents who have downloaded music from the Internet admit to not paying for it.