



DSP VENDORS ARE FIGHTING THE BATTLE ON SEVERAL FRONTS FOR HIGH-PERFORMANCE, LOW-POWER OPERATION AND OFFERING SCALABLE ARCHITECTURES AND OPTIMIZED INSTRUCTION SETS. BUT THE INDUSTRY STILL REQUIRES BETTER TOOLS.

DSPs for next-generation cell phones **BALANCE** performance and power

THE FIGURES ARE COMPELLING: Industry analysts forecast the number of worldwide cellular subscribers to grow at a 23% rate—from 611 million units this year to 1.7 billion in 2005 (**Reference 1**). With this growth comes a shift away from the circuit-switched, voice-only communications and Internet access that characterizes second-generation cell phones toward the more exotic

packet-switched functions of 2.5G (2.5-generation) and 3G (third-generation) handsets; these functions include audio, graphics, interactive games, and streaming video.

DSPs lie at the heart of both the current and the emerging technologies. Pressed to meet the opposing demands of faster throughput, miserly power consumption, and low cost, DSP vendors are

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conjuring new chip designs as well as full chip sets that serve as platforms for quickly bringing new cell phones to market. Multiple instruction cycles, scalable architectures, and optimized instruction sets are some of the technical tricks vendors are pulling from their hats.

In addition, to handle the demanding new applications, DSPs and their companion microcontrollers will make increased use of operating systems, including real-time versions. Meanwhile, having access to ready-made algorithms and keeping code compact to minimize costly memory requirements will also be priorities for new cell-phone designs, as will be the need to preserve software investments by reusing existing code. To quickly get these complex products to market, however, designers will need sophisticated development tools—as yet unavailable—similar to those that vendors use to build microprocessor-based systems. Time-to-market pressures will also require concurrent development of system hardware and software, the tools for which remain wanting.

PERFORMANCE APLENTY

From a hardware perspective, performance and power consumption are among the most pressing DSP specifica-

AT A GLANCE

- ▶ Scalable architectures and communications-specific instructions are helping DSPs meet 2.5G and 3G cellular-technology performance and power specifications.
- ▶ DSP vendors are expanding beyond chips to offer platforms and architectures.
- ▶ Tools are sorely lacking for developing hardware and software in parallel.

tions needed to meet 2.5 and 3G requirements (see sidebar “3G or not 3G: That is the question”).

With most third-generation standards supporting not only voice, but also data connectivity, the MIPS requirements are getting really large, according to Yueh-way Sun, a marketing manager for wireless communications products at Lucent Technologies. Other drivers for higher performance are the need to accommodate multiple application standards and a new turbo-decoding algorithm to reduce data errors. For 2.5G, says Sun, 100 MIPS is the “ideal target number.” Di-ping Chou, a DSP manager for Philips Semiconductors, also considers 100 MIPS a “comfort-

able” number for 2.5G systems now in the works.

But that figure will need to grow to deliver the high-bandwidth and complex applications being promised for 3G systems (figures 1 and 2). For example, Doug Grant, business development director for Analog Devices, targets 200 to 300 MIPS for 3G systems running full-duplex operation; that is, transmitting and receiving at the same time. At least one player, though, is shooting for a greater order of magnitude: Alex Bedarida, vice president for DSP at Infineon Technologies, pegs the “3G challenge” at nothing less than 3000 DSP MIPS. Perhaps ironically, their respective targets do not daunt these vendors; cranking out performance alone from a DSP is relatively easy. The problem is getting that performance at acceptably low power levels.

People want longer talk and standby time, according to Nick Marshall, a marketing manager for subscriber technology at Motorola’s Semiconductor Products Sector. As a result, he adds, systems have to exhibit ultra-low-power consumption to preserve battery life—a specification that butts heads with the high clock rates that can deliver performance.

3G OR NOT 3G: THAT IS THE QUESTION

Based on emerging technologies and standards, precise performance definitions for 2.5G and 3G cellular phones remain somewhat elusive. As the haze begins to lift, however, some

characteristics and specifications consistently emerge (Table A). For example, 2.5G phones mark a shift from circuit-switched to packet-switched networks and a heavy emphasis on data and

voice transmissions. As for bandwidth, the General Packet Radio Service, widely considered a 2.5G specification, defines data rates of 64 to 115 kbps. In comparison, 2G systems typically reach 9.6 kbps, though some services offer data rates as high as 28 kbps. Another emerging specification, EDGE (Enhanced Data Rates for GSM Evolution), which some consider to be 2.5G and some consider 3G, moves data at a rate as high as 384 kbps. In contrast, the UMTS (Univer-

sal Mobile Telecommunications System) and Wideband CDMA (code-division multiple-access) specifications, both firmly in 3G territory, call for data rates as high as 2 Mbps if you are stationary, 384 kbps if you are walking, and 144 kbps if you are in a moving car or train. But as Doug Grant, business development director for Analog Devices notes, from the consumer’s standpoint, the difference between 2.5G and 3G data rates is moot.

“It is really splitting hairs because the fact is, given today’s 9.6-kbps rates, getting to even 384 kbps is a huge quantum leap,” says Grant.

TABLE A—KEY 3G REQUIREMENTS

Media-rich applications in a mobile environment

Highly DSP intensive

Video streaming, digital audio, interactive games, encryption, voice recognition

Applications will be dynamic

Software will be downloaded

Operating systems to handle dynamic task management

Cache-based hardware architectures

Security: encryption, firewall, virus...

High data rates will be required

384 kbps to 2 Mbps

Mix of real-time communications and a range of real-time applications

Extended battery life

Increasingly, DSP vendors have addressed the problem by offering new scalable architectures. One example is Lucent and Motorola's StarCore family of DSP cores, a successor to Motorola's DSP56600 line. The first member, the SC140, has four MAC (multiply-accumulate) units and executes four instructions per clock cycle. The more recent SC110 has just one MAC unit, providing moderate performance but using little power. On the other end of the scale, performance takes priority; designers who license the StarCore family could synthesize a unit with eight MAC units.

Also stressing modularity is the second generation of Infineon's Carmel family of 16-bit DSPs cores, the DSP 20xx, which boasts PowerPlug modules that accelerate computationally intensive tasks. Software sees these PowerPlug modules, which are tightly coupled to the Carmel DSP core (Figure 3), as built-in execution units along the DSP datapath. In this way, the modules can implement computationally intensive tasks to accommodate multiple data rates and complex modulation schemes without exacting a heavy toll in power dissipation or system cost.

Low power consumption is also an important feature for Texas Instruments' new TMS320-C55x DSP core. Drawing just 0.05 mW/MIPS and churning through data at as much as 800 MIPS, the C55x takes one-sixth the power of its popular predecessor, the TMS320C54x. By quadrupling battery life, the C55x is said to push cell-phone operating times from days to weeks.

Even on the microcontroller side, the growing need for DSP cycles in coming generations of cell phones is forging changes. For example, one of ARM's latest introductions, the ARM9E processor core, touts added DSP functions. Based on the ARM9TDME core, but with signal-processing extensions of the ARM instruction set, the ARM9E performs at 200 MIPS at 200 MHz. It executes one 16x16- or 16x32-bit MAC instruction per cycle.

THE SOFTWARE SIDE

Vendors are also meeting performance and power requirements by improving the DSP's software side. Among the first things needed to make software "less of

an issue," says Analog's Grant, is to optimize instruction sets for the algorithm that communication systems use. (Although Analog Devices and Intel have embarked on a joint DSP-development project, neither company offers details of the deal, except to say that a progress report is forthcoming.)

Infineon's Carmel, for example, exploits "instructional-level parallelism" through its use of 144-bit CLIW (configurable long-instruction words). A CLIW comprises a 48-bit reference instruction in program memory and a 96-bit block instruction in CLIW memory. The architecture reserves such instructions for the code's inner loop, which is the 10% or so of code that executes most of the time. Other instructions in the set include basic 24-bit instructions and full-word, 48-bit operations that include large operand fields and direct operand references.

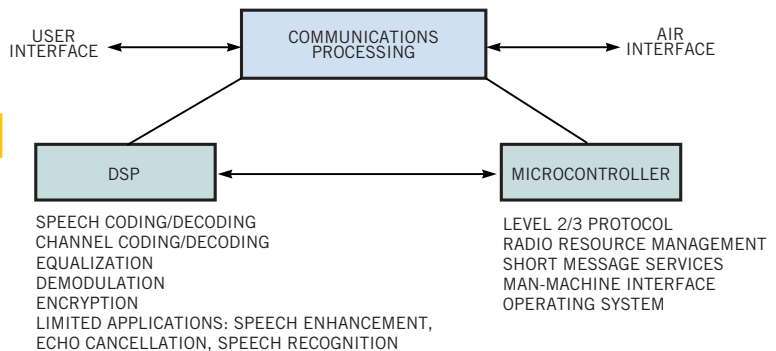
To further enhance the DSP performance of some of its microcontroller de-

signs, ARM plans to announce SIMD (single-instruction multiple-data) extensions. In this way, a μ C can, for example, process video data by encoding and decoding MPEG4 images suitable for small appliances. Moreover, to minimize the amount of code stored in costly memory, ARM reduces what would otherwise be 32-bit instructions to 16 bits for the most common operations.

The urgency to keep code tight and fast within the cell phone's limited resources means that you must do hand-coded assembly, says Krishna Yarlagadda, founder and chairman of Hellosoft, which develops communications systems. When you are switching to a new architecture, hand-coding becomes a problem: How do you preserve your software investment? As a result, says Yarlagadda, a tremendous opportunity exists for companies that make the right tools and compilers.

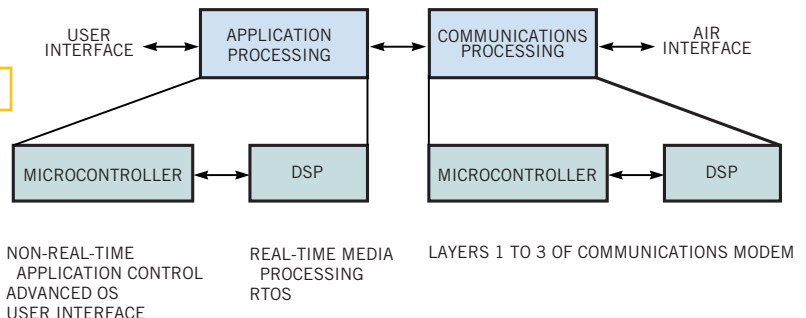
"Building a new phone from scratch takes a huge dollar investment," he says,

Figure 1



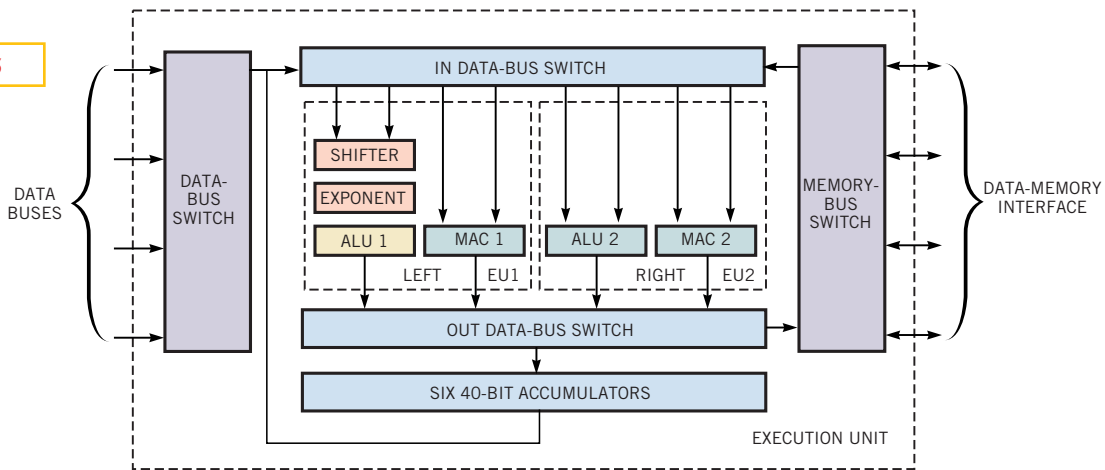
In current 2G cellular phones, the DSP handles channel functions, such as speech encoding and decoding, equalization, modulation and demodulation, and encryption. The μ C processes protocols and performs user-interface functions (courtesy Texas Instruments).

Figure 2



Forthcoming 3G cellular phones will require advanced and real-time operating systems to execute such applications as audio, graphics, and streaming-video algorithms (courtesy Texas Instruments).

Figure 3



Modular, scalable DSPs, such as Infineon's Carmel 20xx 16-bit DSP core, help designers make the performance and power trade-offs for delivering advanced functions and long operating time.

and tools that help to write or reuse software offer the designer a significant time advantage. Grant agrees that now is the time for better development tools.

"Tools have got to become as easy to use as those for writing microcomputer code." Toward that end, Analog has acquired White Mountain DSP, a leading supplier for emulators for DSPs, and Edinburgh Portable Compilers, which specializes in software compilers for high-performance, embedded applications. Having readily available software is another piece of the cell-phone-software puzzle.

A designer "shouldn't be worrying about what algorithm to use for a Viter-

bi decoder or the channel equalizer," says Grant.

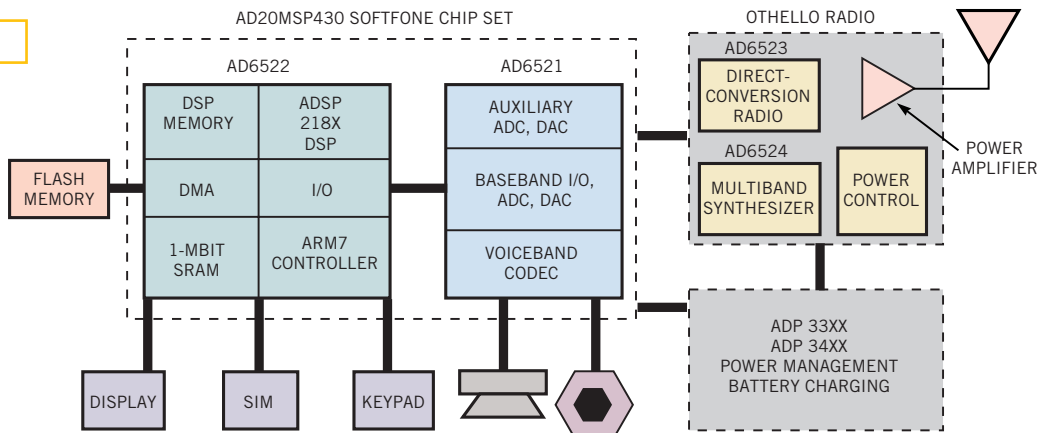
Operating systems are one type of software component that has until now not played a big role in the DSP portion of a cell phone design.

"There have been a bunch of kernels running on the MCU side and no operating system on the DSP, except for a little tasking routine," says Hellosoff's Yarladda. But as applications, such as personal-information managers, calendars, and Web browsers, increasingly target the cell phone, "we are starting to see operating systems take hold." Moreover, he notes, these OSs, such as Symbian's EPOC, can be sophisticated.

To help cell-phone designers get up to speed, DSP vendors are branching out to offer complete highly integrated chips and chip sets. These ready-made platforms will help them launch their products in the market. For example, in September, Infineon announced that it had delivered to one customer the dual-mode M-Gold UMTS (Universal Mobile Telecommunications System)/GSM (Global Systems for Mobile Communications) baseband chip, which combines Infineon's Carmel DSP with its TriCore 32-bit microprocessor system.

And, in January, Analog Devices introduced its AD20msp430 SoftFone, the first completely RAM-based baseband

Figure 4



To speed the design of next-generation cell phones, DSP vendors are offering complete chip sets, such as the AD20msp430 SoftFone from Analog Devices.

chip set for wireless handsets (**Figure 4**). With it, designers can build not only GSM mobile phones, but also PDA (personal-digital-assistant) platforms and Internet appliances that meet 2.5G wireless-data-communications standards. The chip set is also said to be forward-compatible with future 3G cellular standards.

SoftFone comprises an AD6522 digital baseband processor, which includes an ADSP-218x DSP core, and an ARM7-TDMI RISC processor, and the AD6521 advanced baseband converter. The two chips complement Analog Devices' Othello chip set, which completes the signal chain by providing direct-conversion radio technology for GSM.

Also, in May 1999, Texas Instruments announced that Nokia would build wireless information devices around TI's OMAP (Open Multimedia Application Platform). The platform embeds a 320-MIPS DSP with a 130-MHz ARM processor and high-speed dedicated logic blocks. The platform's hardware includes building blocks, such as complex megacells and peripherals, that connect easily to the customer's own circuit blocks. Although Nokia targeted Symbian's EPOC operating software, OMAP is operating-system and data-standards "agnostic," says Alain Mutricy, a wireless-business-



unit director at Texas Instruments. This year, according to Mutricy, Sony and Ericsson also selected OMAP for their 3G products, and, in September, Handspring chose the platform to power a wireless voice and data module for its Visor PDA.

Looking ahead, Yarlagadda sees a powerful combination in ARM processors, with its newly acquired DSP prowess, and Symbian's EPOC software, suggesting that together the two could become the cell-phone equivalent of the Intel x86/Microsoft Windows de facto standard platform. But, as he sees it, politics as much as technology will decide how

cell-phone makers take to the standard-platform idea.

For one thing, cell-phone makers tend to build their own chips. For example, cell-phone maker Qualcomm has practically become a chip-set company, Yarlagadda says. And these companies count on their proprietary platforms to distinguish their products. Moreover, these vendors—again Qualcomm in particular—have invested a lot of IP (intellectual property) in their chips; this IP can serve as roadblocks to other vendors.

"If you want to make all these standards homogenous, you have to give up some of this IP," says Yarlagadda. But with new players entering the market, anything can happen, and a standard platform may be in the industry's future.

"For the first time, the market shares held by Nokia and Ericsson fell—this in a market that has been growing all along. We are going to see more players in this space," he says. □

REFERENCE

1. "Wireless Infrastructure Technology and Markets: Evolution to 2.5G and 3G," Forward Concepts, July 2000.

You can reach Contributing Editor Gil Bassak at 1-914-941-1823, fax 1-914-941-2634, e-mail gil@word-warrior.com.

FOR MORE INFORMATION...

For more information on DSPs for 2.5G and 3G cellular phone technology, such as those discussed in this article, go to our information request page at www.rscachners.ims.ca/ednmag/. When you contact any of the following manufacturers directly, please let them know that you read about their products in *EDN*.

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