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AS YOU RAISE THE CLOCK RATE—AND THUS THE SIGNAL RISE AND FALL TIMES—TO SQUEEZE MORE PERFORMANCE FROM A DESIGN, UNDERSTANDING THE EFFECTS OF TERMINATION SCHEMES IS MORE IMPORTANT THAN EVER. EASY-TO-USE PC-BASED SPICE TOOLS PROVIDE USEFUL INSIGHT INTO THE BEHAVIOR OF TERMINATION SCHEMES IN HIGH-SPEED INTERCONNECTS.

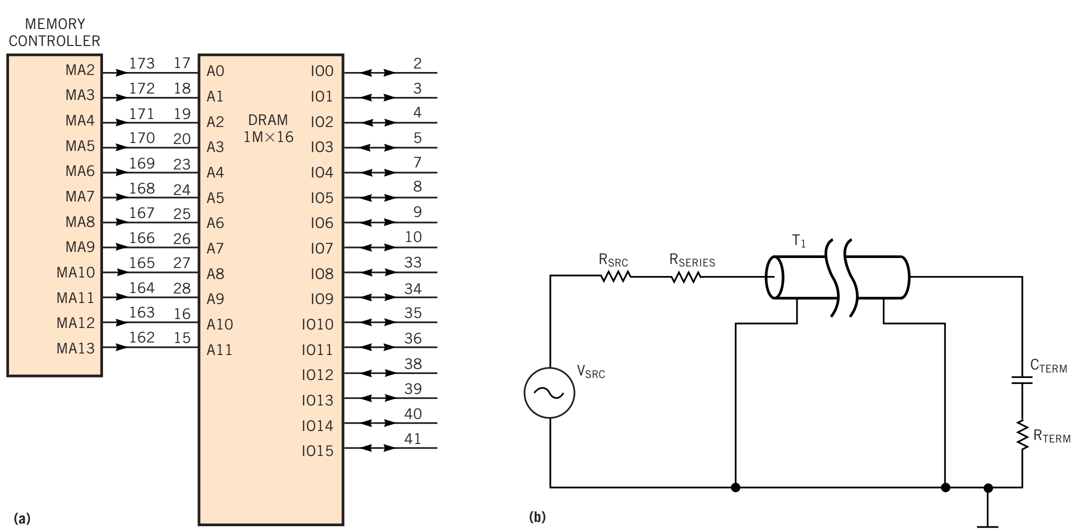
Spice provides signal-integrity clues for high-speed systems

Many engineers use a trial-and-error approach to fix transmission-line problems in high-speed digital circuits. They experiment on the same interconnecting trace with series termination, parallel ac termination, and sometimes both.

There is a better way. Spice tools allow you to perform simple simulations with various termination and bus topologies. The simulations work equally well at 10 MHz or 10 GHz, and they don't need exotic high-frequency test fixtures. The simulation results can provide you with a seat-of-the-pants understanding of the behavior of a high-speed digital bus. For exotic and critical applications for which you can justify the training and purchase costs, more complex signal-integrity tools are available. However, Spice can provide lots of insight with little investment. Most Spice vendors offer free evaluation versions and training time.

PSpice from Orcad Inc (www.orcad.com) lets you build circuits with a graphical user interface so that you don't have to memorize Spice syntax. PSpice also has a built-in waveform-graphing function. The interface allows you to perform "what-if" scenarios, varying circuit parameters to understand how these parameters affect the circuit's behavior. This ability can provide you with an important qualitative understanding of a circuit's behavior.

Figure 1



A simple circuit (a) can model any of these digital interconnects (b).

You can use Spice to model a high-speed digital bus by first drawing its equivalent circuit (**Figure 1**). The circuit in **Figure 1a** can model any one of the digital interconnects in **Figure 1b**. The circuit includes the driver voltage and rise time (V_{SRC}), the source impedance (R_{SRC}), any series impedance you add to match the driver's impedance to the transmission line (R_{SERIES}), the transmission line, and any terminating capacitance and resistance you add to terminate the line (C_{TERM} and R_{TERM}). You can perform experiments by varying the values of the components. Using a tool such as Spice to perform these experiments before board layout can reduce project costs and lead times. **Table 1** shows the parameters you need to know to model the circuit.

For simplicity, examine a logic signal as it switches from a low level to a high level. The analysis and conclusion of the high-to-low case would be identical if you turn the resultant graphs upside-down. You can compare several termination schemes by varying the values of R_{SERIES}, C_{TERM}, and R_{TERM} (**Table 2**). If your Spice tool does not accept zero or infinite as a component value, you can substitute a suitably large or small number. After you enter these values, you can perform a PSpice simulation with a single mouse click. **Figure 2** shows the voltage levels at a device close to the driver. Series termination is the winner here, producing the fastest rise time with the least overshoot. The unterminated line shows the most overshoot, and both of the lines that use parallel ac termination require a longer settling time for the series capacitor to charge.

At high speeds, the location of a device on a transmission line can influence both the timing and the shape of the transient switching waveform at its inputs. **Figure 3** shows the voltages that appear at the end of the transmission line. In these cases, the range of the voltages exceeds that of the voltages in **Figure 2**. Also, the overshoot for the unterminated transmission line is more severe at the end of the transmission line.

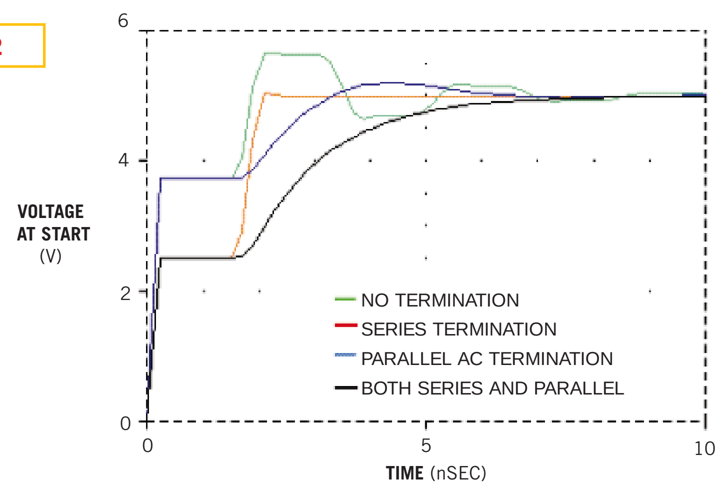
MODEL GROUND BOUNCE

A Spice simulation can also measure the driver current. Driver current is important because rapid changes in the current cause ground bounce. Ground bounce happens when a high-frequency

TABLE 1—TRANSMISSION-LINE PARAMETERS TO MODEL

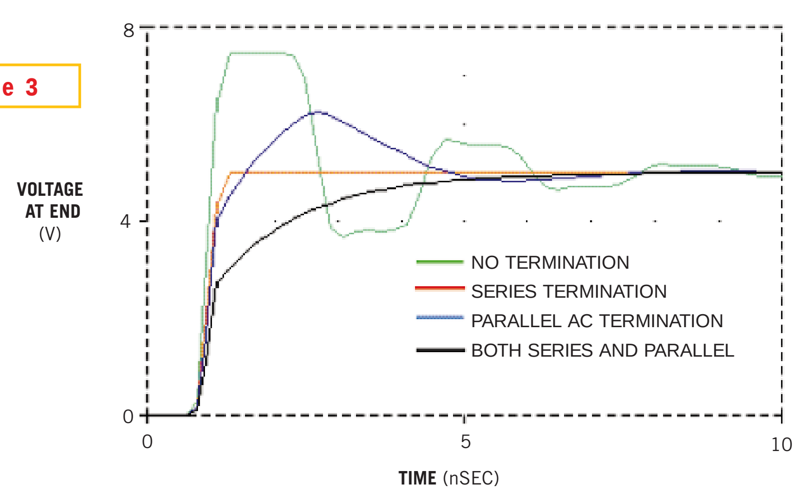
Parameter	Source	Value
Driver output impedance	Manufacturer's data or experiments	24Ω
Driver rise time	Function of driver strength and capacitance at driver	0.259 nsec
Input impedance of driven device	Manufacturer's data or experiments	Infinite
Transmission-line impedance	Manufacturer of pc boards; varies with trace width; typical values for a four-layer board are 70Ω for a 5-mil trace and 58Ω for an 8-mil trace	70Ω
Transit time	Divide trace length by the speed of the wave in the transmission line, which depends on the board's dielectric coefficient	0.83 nsec

Figure 2



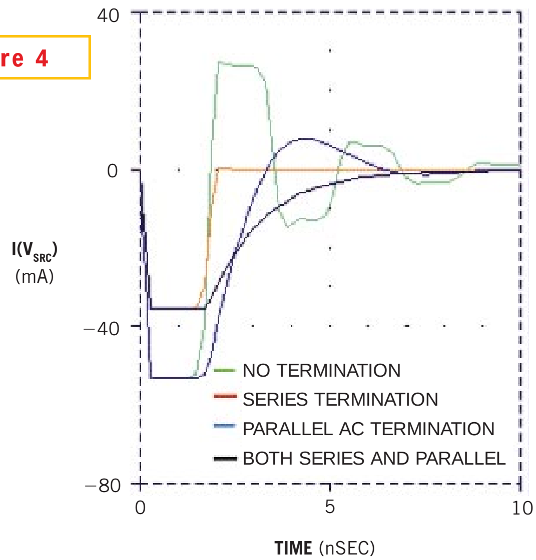
At a device close to the driver, the series-terminated transmission line shows the fastest settling characteristic, and the unterminated line shows the most overshoot. Both lines that use parallel ac termination require a long settling time for the series capacitor to charge.

Figure 3



The termination scheme has a different impact at the end of the transmission line than at a device close to the driver, as in Figure 2. The overshoot of an unterminated transmission line is even more severe at the end of the transmission line.

Figure 4



PSpice lets you display the driver current necessary to perform switching, which can give you an idea of the impact of the termination scheme on ground bounce. Although a series termination improves switching waveforms and reduces ground bounce, a parallel ac termination also helps with ground bounce.

TABLE 2–TERMINATION-SCHEME VARIATIONS

Termination	R_{SERIES} (Ω)	C_{TERM} (pF)	R_{TERM} (Ω)
None	0	0	Infinite
Series	46	0	Infinite
Parallel ac	0	10	70
Series plus parallel	46	10	70

current must sink to ground through a finite inductance, such as a bond wire or packaging lead. Ground bounce is most pronounced on falling transitions because the digital circuit must sink current to ground to discharge the interconnecting trace and its loads. On rising edges, the voltage source sees most of the noise. Ground bounce is more serious than power-supply bounce because logic circuits reference ground. Therefore, changes in the ground can change the perceived value of a logic signal. If this change causes the system to perceive high logic levels as low logic levels, spurious clocking and other problems can occur.

Figure 4 shows the driver current for the various termination schemes; a positive value in the graph represents a current that would flow into the ground plane. The **figure** shows currents for one driver only; the effects are even more pronounced when simultaneously driving eight or 32 signals. Although a series termination improves switching waveforms and reduces ground bounce, parallel ac termination also helps with ground bounce. Specifically, these termination schemes reduce the height and slope of the current spike. **Figure 4** also shows that the unterminated line alternately dumps current onto the ground and requires positive V_{CC} current during switching.

PERFORM A FOURIER ANALYSIS

The high-frequency components of the driver current are of the greatest concern because the inductive impedance of the ground path increases linearly with frequency. Spice includes a Fourier-analysis feature that shows the frequency components of the signals listed above (**Figure 5**). Not the highest value but the weighted product of the magnitude and the frequency is relevant here. Series termination comes out a clear winner in **Figure 5**. Parallel ac termination shifts the no-termination spectra to a lower frequency but does not diminish its magnitude.

You can download the Spice listings for this article from *EDN*'s Web site, www.ednmag.com. □

References

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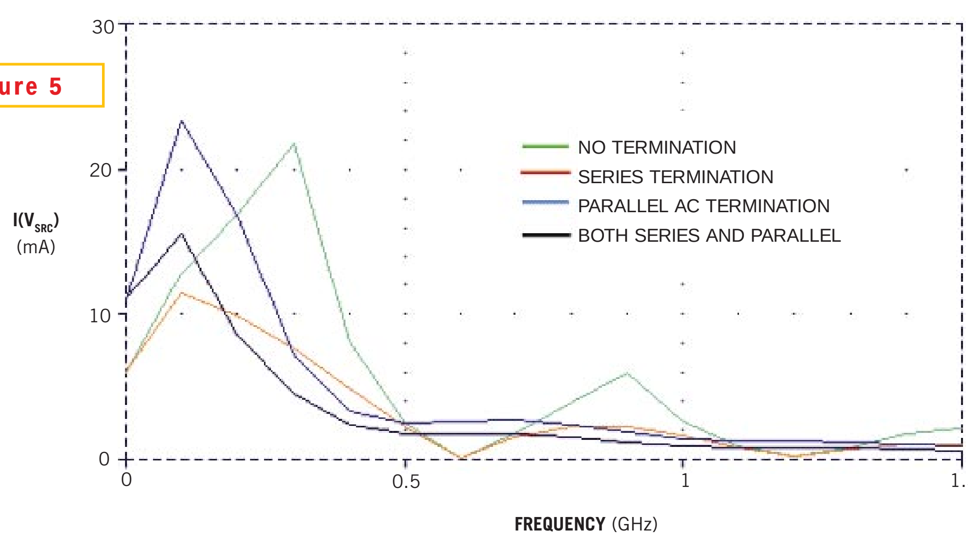
Author's biography

Ken Boorom works for Hewlett-Packard Co's Laserjet Solutions Group in Boise, ID, where he is responsible for ASIC and circuit-board qualification. He holds a BSEE and an MSEE from Stanford University (Palo Alto, CA).

Figure 5



A Fourier analysis of the switching current can be a guide in evaluating ground bounce. You can expect termination schemes that produce switching currents with strong high-frequency components to exacerbate ground bounce because all current must reach ground through inductive impedance.