

Digital countdown timer may never need battery replacement

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Comprising a microprocessor, an LCD, a 32.768-kHz crystal, and little else, the basic countdown-timer circuit in **Figure 1** operates from a commonly available CR2032 lithium-coin-cell battery. Based on the circuit's calculated current drain, the battery may never need replacement over a projected 10-year operational life. Careful selection of the battery and diligent exploitation of the microprocessor's low-power modes help minimize power consumption and thus maximize battery life. The coin-cell battery's size and flat form factor encourage miniaturization for portable-system applications. In addition, the lithium cell presents a flat voltage-versus-time discharge curve that allows direct drive of the LCD's segments to produce high contrast without additional compensation circuitry.

A typical CR2032 cell delivers ap-

proximately 200 mAhr of rated energy capacity. To achieve the design goal of 10 years of continuous operation, the system's average current consumption must not exceed $2.28 \mu\text{A}$, which you calculate by dividing the battery's energy capacity by the system's operational life: $200 \text{ mAhr}/10 \text{ years}/365 \text{ days}/24 \text{ hours} = 2.28 \mu\text{A}$. A microprocessor from Texas Instruments' MSP430 family presents a low-standby-current demand of only $0.8 \mu\text{A}$, which includes current drawn by its crystal oscillator, integrated LCD driver, and interrupt-driven wake-up timer. The $3\frac{1}{2}$ -digit LCD, a Varitronix model VI-302-DP, consumes an additional $1 \mu\text{A}$. The total standby-current consumption for all active countdown-timer components is thus $1.80 \mu\text{A}$.

In normal (standby) operation, the microprocessor's 32-kHz external-crystal clock drives an internal counter that

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generates an interrupt once per second. The interrupt awakens the processor, which executes an active main-software loop that decrements a countdown register via direct BCD (binary-coded-decimal) subtraction. Adding a value of 99 (decimal) to the countdown register and discarding the leftmost digit perform a one-digit subtraction. For example, $21 + 99 = 120$; dropping the one in the 100s place yields a value of 20. As a bonus, this method directly displays the countdown register's contents on the LCD without requiring current-hungry binary-to-BCD conversions. (You can download the timer software's assembly-language listing from the online version of this Design Idea at www.edn.com/050623di1.)

As a final step, the main loop compares the countdown register's contents with zero to determine whether the pre-programmed time interval has expired. If so, the display flashes the time-out message. The main loop activates the CPU and its on-chip high-speed oscillator, which consume a total of $250 \mu\text{A}$. Writing the software to execute 100 or fewer clock cycles—equivalent to 100 μsec at the default 1-MHz CPU clock frequency—reduces current demand. With such a short active period, the main loop's total current consumption is virtually negligible: $\text{Main loop} = 250 \text{ mA} \times (100/1 \text{ million}) = 0.025 \mu\text{A}$.

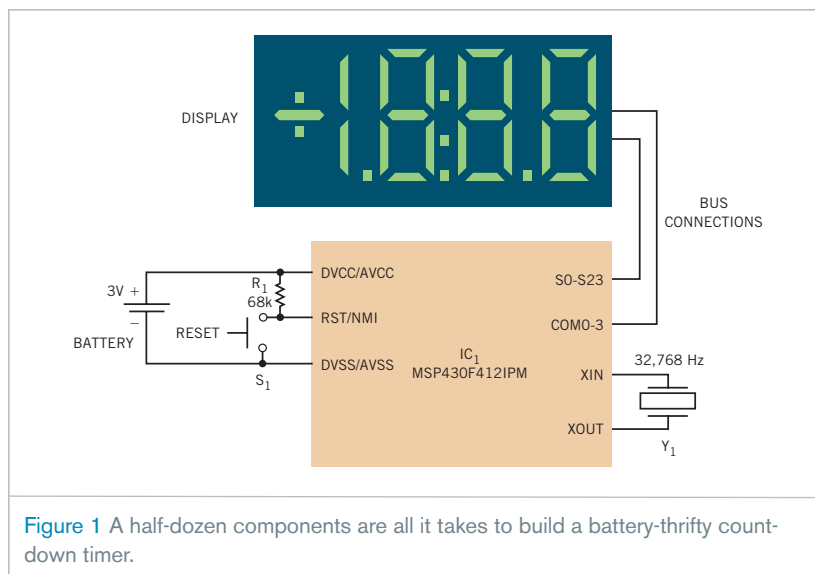


Figure 1 A half-dozen components are all it takes to build a battery-thrifty countdown timer.

Thus, total current consumption for the digital countdown timer is the sum of the standby- and main-loop currents: $1.8 + 0.025 \approx 1.8 \mu\text{A}$.

At approximately $1.8\text{-}\mu\text{A}$ average current consumption, the countdown timer easily meets the $2.28\text{-}\mu\text{A}$ design goal and ensures more than 10 years of continuous operation. Given the device's low current drain, a designer


could reduce the timer's cost and complexity by packaging the circuitry along with a nonreplaceable battery. Many of the microprocessor's functions and I/O pins remain unused and available for additional features, and the compact firmware for implementing the counter occupies less than 250 bytes of 8 kbytes of available flash memory.

Applications for the circuit range

from exercise-routine timing to a restaurant-service-guarantee timer. In such an application, the restaurant's greeter presses the timer's reset switch to reset the processor and start a pre-programmed countdown interval. If the time interval expires without the customer's being seated, the timer's display flashes to indicate that a guarantee of service went unmet. **EDN**

Wide-range regulator delivers 12V, 3A output from 16 to 100V source

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 Synchronous buck regulators offer high efficiency and are popular in applications in which available input voltages are 12V or less. However, as input voltage approaches 100V, wide-range-regulator design becomes more difficult, and the choice of suitable ICs narrows considerably. This Design Idea combines a current-mode PWM IC for flyback-regulator circuits with a 100V gate-driver IC to produce

a relatively high-performance synchronous buck regulator that can operate at inputs as high as 100V.

The circuit in **Figure 1** uses National Semiconductor's LM5020 current-mode PWM, IC_1 , to drive an LM5104 gate driver, IC_2 , forming a synchronous controller. The LM5020 contains an internal linear regulator that accepts input as high as 100V and can also deliver an output that can supply drive

current to the LM5104. To reduce power dissipation at high input voltages, after initial power application, diode D_1 , a 1N4148, supplies an 11.5V bootstrap voltage to the remainder of the circuit. Transformer T_1 , a 100-to-1 current transformer from Pulse Engineering, provides current feedback during MOSFET Q_1 's on-time. Q_1 and Q_2 are Siliconix Dpak devices, which have low gate-charge requirements and low on-resistances to minimize total switching losses at the circuit's 200-kHz operating frequency. All capacitors are of ceramic-dielectric construction to withstand high temperature to meet packaging-size constraints.

For sustained operation at high input voltage, maximum current, and elevated-temperature conditions, transistor Q_1 requires an adequate heat sink or cooling airflow to maintain its junction temperature below the 175°C maximum specification. Q_1 has a low junction-to-case thermal resistance, and thus its case temperature must not exceed 160°C . L_1 , the model DO5010 unshielded ferrite-core inductor from Coilcraft, presents a small pc-board footprint and offers a high saturation-current rating but represents this design's dom-

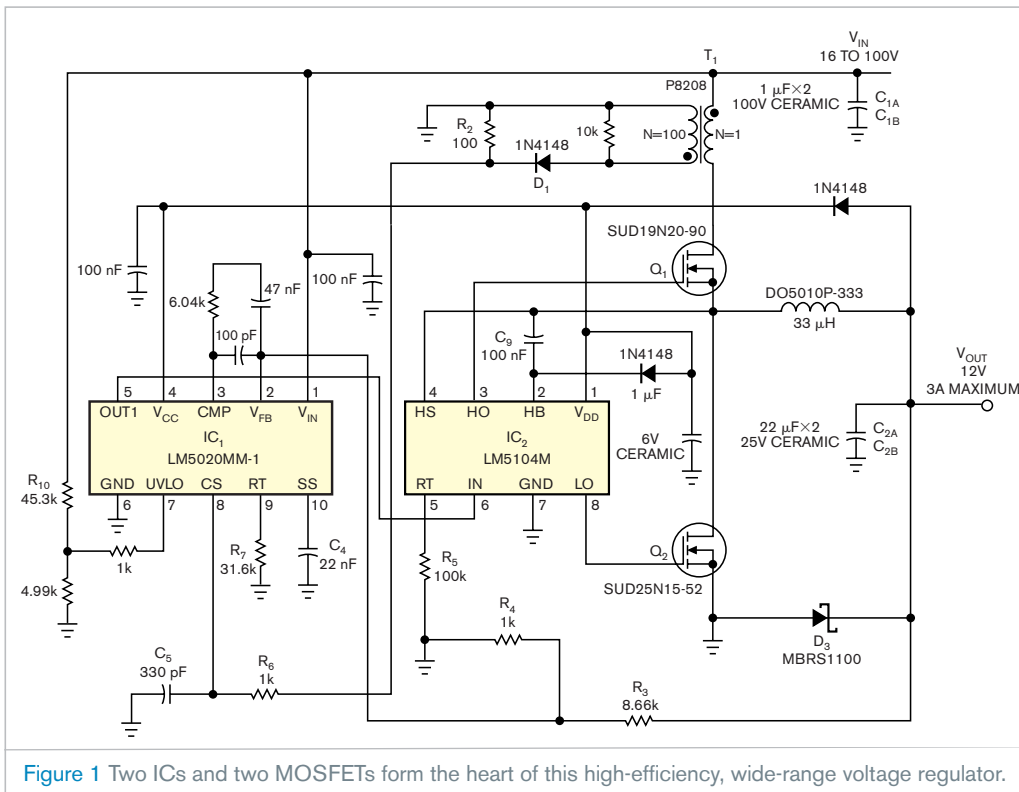


Figure 1 Two ICs and two MOSFETs form the heart of this high-efficiency, wide-range voltage regulator.

inant loss component. For applications with less critical space requirements, you can improve circuit efficiency by increasing L_1 's inductance and size, thus reducing ripple current and enabling use of a larger core and increased winding-wire gauge. Reducing the output voltage improves efficiency, but, as output voltage drops below the circuit's 8V bootstrap voltage, IC_1 dissipates additional power and requires caution to avoid exceeding its ratings. **Figure 2** shows the circuit's measured efficiency versus output current for three input voltages.

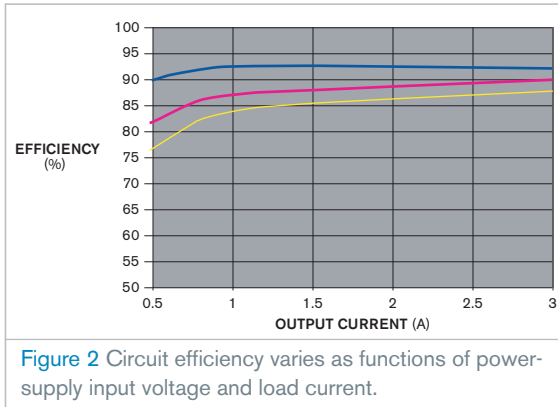



Figure 2 Circuit efficiency varies as functions of power-supply input voltage and load current.

One practical application for the circuit met a customer's requirement for a dc/dc converter that would operate from a 24V source and deliver 12V output at

currents as high as 3A. This routine-sounding specification also requires operation in a physically and electrically harsh environment in which the packaged circuit resides on an engine block that reaches a temperature of 125°C, and ambient-air temperature reaches 100°C. In addition, the power source comprises two series-connected 12V batteries that provide a nominal voltage of 24V, which in practice varies from 18 to 40V and includes inductively induced load-dump voltage spikes that reach 100V. **EDN**

Stable, 18-MHz oscillator features automatic level control, clean-sine-wave output

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 A recent Design Idea described a method for designing simple, high-frequency LC oscillators with few passive components (**Reference 1**). However, for best results, practical hardware design of a stable oscillator requires more parts and greater complexity. **Figure 1** shows a stable, 18-MHz oscillator with automatically leveled output amplitude control and an output buffer that delivers a sine wave with low harmonic content (**Reference 2**). In addition, this Design Idea replaces the original JFET oscillator with an inexpensive dual-gate MOSFET: an Infineon Technologies BF998, available from DigiKey and other sources.

The heart of the circuit comprises a Hartley oscillator, Q_1 . To minimize loading, a 10-k Ω resistor couples the output from Q_1 's source to the high-input-impedance gate of source follower JFET Q_2 . In turn, Q_2 drives Q_3 , a BJT (bipolar-junction-transistor) emitter follower, which in turn drives BJT amplifier Q_4 . Toroidal-core transformer T_1 couples Q_4 's output to a 50 Ω load, delivering 2.61V p-p or 12.3 dBm. A

Spice-circuit simulation predicts a second-harmonic amplitude of 35 dB below the fundamental. The second harmonic exceeds the amplitudes of all higher order harmonics, and an oscilloscope measurement displays a clean-looking sine wave across the 50 Ω load.

To provide a good termination for the amplifier and still obtain 7.3 dBm (1.47 V p-p)—for example, to drive a diode-ring mixer—you can insert a 50 Ω , 5-dB pad between output transformer T_1 and the load. Potentiometer R_2 adjusts the RF output level, and, for increased stability, you can replace R_2 with a fixed resistive divider built with low-temperature-coefficient, metal-film, fixed resistors. Part of the signal at Q_4 's collector drives the gate of JFET source follower Q_5 through C_7 and R_9 . Diode D_1 rectifies the signal, which, after filtering, feeds operational amplifier IC_1 's inverting input. Resistor R_1 and low-temperature-coefficient potentiometer R_2 divide the 12V supply to produce a dc reference voltage for IC_1 's noninverting input and set the output signal's level. After filtering, IC_1 's dc

output drives Q_1 's Gate 2 to set the device's gain and thus control RF output.

Connected to the center tap of coil L_1 , trimmer capacitor C_{18} allows fine adjustment of the oscillator's frequency. If decreased frequency stability is acceptable, you can replace C_{18} with a low-cost ceramic trimmer. Piston-type trimmers are rather expensive and less available than ceramic trimmers, but a typical ceramic trimmer exhibits a temperature coefficient that's at least an order of magnitude worse than a piston trimmer's. To operate the oscillator at a frequency other than 18 MHz, multiply the inductance of L_1 and the capacitances of C_{12} , C_{13} , C_{16} , C_{17} , and C_{18} by $18/f_{OSC2}$, where f_{OSC2} is the new frequency in megahertz. Adjust the tap for Q_1 's source connection so that it remains at about 20% of the winding's total number of turns as counted from the inductor's grounded end.

You can replace the series combinations of C_{12} and C_{13} with a 13-pF capacitor, and you can replace C_{14} and C_{15} with a 2.5-pF capacitor. If you redesign the circuit for a different frequency, adjust the values of C_{14} and C_{15} or their single-capacitor replacement for just enough capacitance to ensure reliable start-up under all anticipated operating conditions. Also, note that using two capacitors for C_{16} and C_{17} helps reduce start-up drift, as does

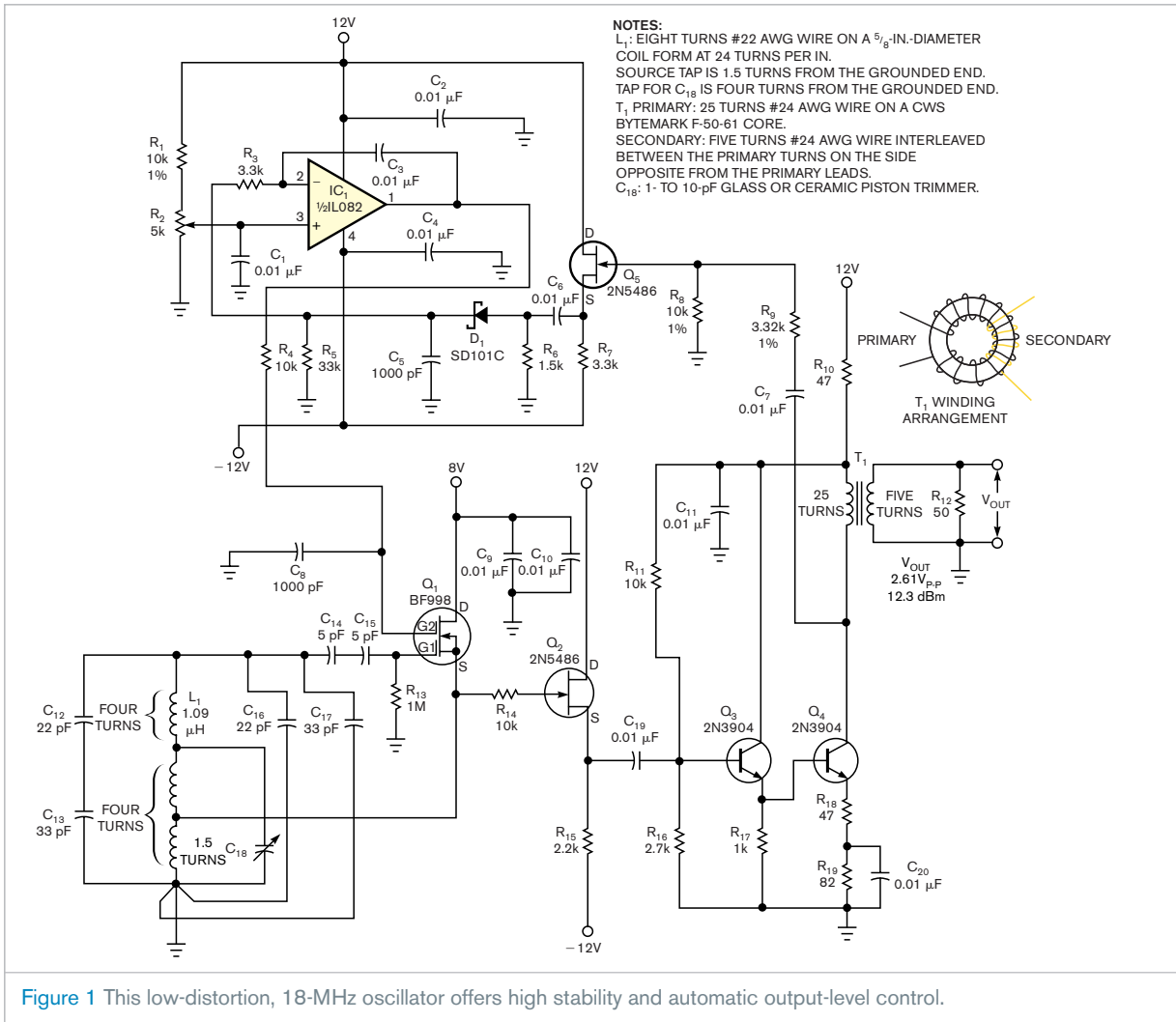


Figure 1 This low-distortion, 18-MHz oscillator offers high stability and automatic output-level control.

using temperature-stable (NP0-characteristic) ceramic-dielectric capacitors for C₁₂ through C₁₇. The buffer amplifier, Q₂ through Q₄, requires modifications for operation at frequencies above approximately 25 MHz.

A well-regulated external dc source (not shown) provides 12, -12, and 8V to the circuit. To maintain high stabil-

ity and remain within Q₁'s 12V maximum drain-to-source-voltage rating, the 8V supply powers only the oscillator. Using the specified components and at a constant ambient temperature of 22°C, after an initial 10-minute warmup period, the oscillator's frequency drifts at an average rate of -2 to -3 Hz per minute over one hour. **EDN**

REFERENCES

- 1 Martínez, H, J Domingo, J Gámiz, and A Grau, "JFETs offer LC oscillators with few components," *EDN*, Jan 20, 2005, pg 82.
- 2 Reed, DG, editor, "A JFET Hartley VFO," *ARRL Handbook for Radio Communications*, 82nd Edition, American Radio Relay League, 2005.

Ultra-low-noise low-dropout regulator achieves 6-nV/√Hz noise floor

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Many low-dropout-voltage regulators see service in electronic systems, but relatively few are designed for low-noise operation. (For example,

Maxim's MAX8887 achieves a noise voltage of approximately 42 μV rms. However, certain applications, such as ultra-low-noise instrumentation oscil-

lators, demand even lower levels of power-supply noise. To reach this level, the circuit in **Figure 1** combines low-noise components and extra filtering to achieve an output noise floor of only 6 nV/√Hz.

Voltage reference IC₁, a Maxim MAX6126, features low output noise. Lowpass filter R₁-C₁ further reduces this noise by attenuating noise frequencies

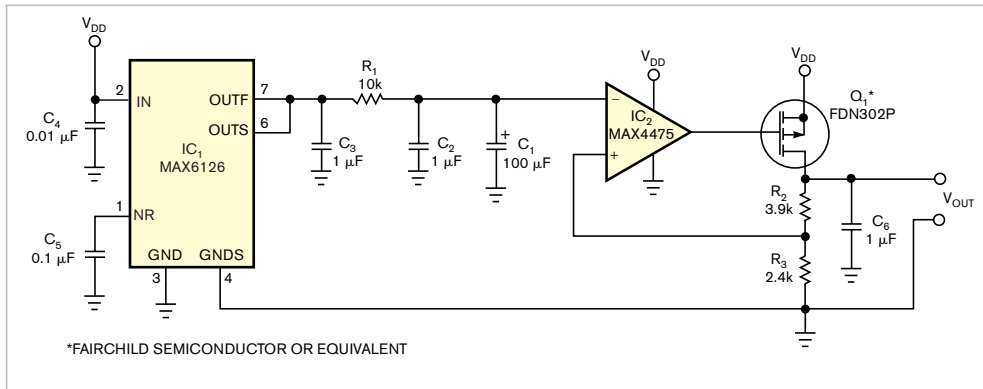


Figure 1 This low-dropout-voltage regulator features a noise floor of only $6 \text{ nV}/\sqrt{\text{Hz}}$, making it an ideal power source for low-noise oscillators.

where V_{N_OUT} represents the low-dropout circuit's output noise, V_{N_REF} represents the reference noise, V_{N_OPAMP} represents the op amp's input-referred noise, and $H(f)$ represents the R_1 - C_1 low-pass filter's transfer function. If a noise frequency of interest falls well below the filter's cutoff frequency, the reference noise is negligible, and the low-

dropout circuit's output noise comprises only the op amp's noise multiplied by the closed-loop gain. The feedback loop suppresses V_{N_FET} , the MOSFET's noise contribution, which therefore can't contribute to the output noise. For frequencies within the loop's bandwidth, the low-dropout circuit also rejects ripple and noise voltages that the power supply introduces.

Figure 3 shows a plot of noise density versus frequency for the circuit of **Figure 1**, which exhibits a noise floor of about $6 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz. For comparison, the plot shows the noise-measurement instrument's noise floor and a typical low-dropout circuit's much higher noise density—for example, $500 \text{ nV}/\sqrt{\text{Hz}}$ at 1 kHz for the MAX8887 low-noise, low-dropout circuit.

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above IC_1 's 0.16-Hz cutoff frequency. The filtered reference voltage drives the inverting terminal of error amplifier IC_2 , a Maxim MAX4475, which regulates the output voltage by means of Q_1 , a P-channel power FET source follower. Feedback resistors R_2 and R_3 determine the output voltage as follows: $R_2 = R_3[(V_{OUT}/2.048V) - 1]$.

The simplified noise-analysis diagram illustrates the components' noise contributions (**Figure 2**). Lowpass filter R_1 - C_1 attenuates high-frequency noise on the voltage reference's output. The op amp's noise current, $0.5 \text{ fA}/\sqrt{\text{Hz}}$, is negligible with respect to its voltage noise, $4.5 \text{ nV}/\sqrt{\text{Hz}}$. The reference-noise source adds to the op-amp voltage noise because they effectively connect in series. The MOSFET's noise contribution appears at Q_1 's input.

The noise at IC_2 's inverting terminal equals the noise at its noninverting terminal:

$$V_{N_REF}H(f) + V_{N_OPAMP} = V_{N_OUT} \left(\frac{R_3}{R_2 + R_3} \right),$$

and

$$V_{N_OUT} = (V_{N_REF}H(f) + V_{N_OPAMP}) \left(\frac{R_2 + R_3}{R_3} \right),$$

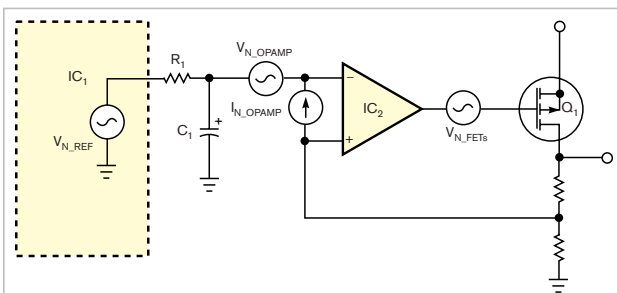


Figure 2 This simplified version of **Figure 1** highlights noise sources for analysis.

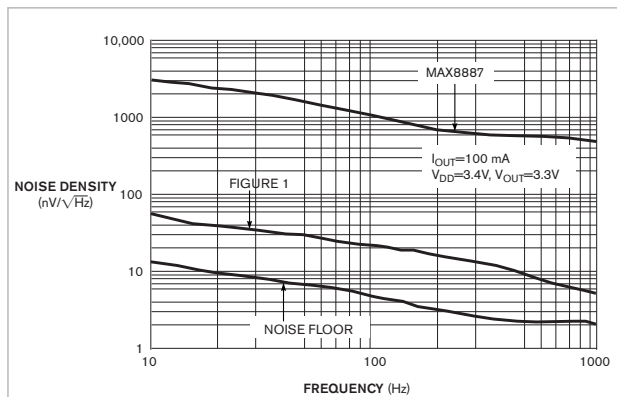


Figure 3 A noise-density-versus-frequency plot for the low-dropout circuit in **Figure 1** is 38 dB lower than that of a conventional low-noise, low-dropout-voltage regulator—in this case, a Maxim MAX8887.