



Tea party

"We need a language that lets us scribble and smudge and smear, not a language where you have to sit with a teacup balanced on your knee and make polite conversation with a strict old aunt of a compiler."

**—Paul Graham,
in *Hackers & Painters:
Big Ideas
from the Computer Age*
(O'Reilly Media, 2004)**

Embedded device server swings both wired and wireless ways

By Bill Schweber

IF YOU DON'T KNOW whether you need Ethernet or 802.11b-only connectivity, the WiPort embedded device server from Lantronix may be for you. The module lets you add high-end connectivity to a variety of applications, such as sec-

urity systems, medical instruments, industrial automation, retail installations, and building automation for remote access, monitoring, and overall networked management.

With a footprint of about 1 in. sq, this module builds on the Lantronix XPort to combine a processor, memory, an 802.11b transceiver, and dual high-speed serial ports. But it is more than just hardware; it includes the operating system,

embedded Web- and device-server functions, a TCP/IP protocol stack, and security protocols. The 40-pin device includes a flexible antenna configuration, serial data speeds to 920 kbaud, and as many as 11 configurable I/O points. The WiPort sells for \$119 (single units); the developer's kit costs \$299.

► **Lantronix Inc.**, 1-949-453-3990, www.lantronix.com.



With the WiPort embedded device server, you can quickly add wired or wireless IEEE 802.11-compliant Ethernet access to your products; it's a complete hardware module that also has the necessary operating-system software and layers.

ACCEPT THE CHALLENGE

IF YOU KNOW YOUR WAY around a microcontroller, we have a challenge—and, possibly, a reward—just for you. Together, NEC Electronics America and *EDN* have launched Cornelius van Drebbel's Mad Design Contest.

We challenge you to be as innovative as the not-so-famous 17th-century inventor. However, you'll have more modern tools to work with, such as a highly integrated, 8-bit processor with a display controller onboard. The most innovative among you will walk away with a piece of more than \$26,000 in prize money, and everyone that submits a valid entry will receive at a minimum a consolation award.

You can play the game in one of two ways: You can submit your concept for a microcontroller-based design and

request a development board that you'll then use to build the project. Selected entrants who choose this route will receive the necessary development tools along with the board and will compete for a top prize of \$10,000. Alternatively, you can simply compete on paper, developing an innovative concept and striving for a \$2000 top prize.

Our Mad Design Contest is under way now. Go to www.maddesigncontest.com to register and learn about good-old Cornelius, too. You'll have plenty of time to complete your entry—provided that you act now. Game on, and good luck.—by Maury Wright



Synopsys again tries its hand at FPGA synthesis

FPGA DEVICES offer enough speed and size to be viable tools for ASIC prototyping and, in many cases, substitute for ASIC devices for short periods during product introduction. Although Synopsys is the undisputed market leader in ASIC synthesis, it has been unsuccessful with its FPGA-synthesis offerings. Previous offerings, such as FPGAXpress, suffered because the company viewed the FPGA market as less important than the ASIC market, and all technical and

marketing decisions favored ASICs.

In another attempt at the market, Synopsys has announced DC (Design Compiler) FPGA, which targets designers who prototype ASICs using FPGAs. The new product links directly with Design Compiler, a product that has practically become a synonym for logic synthesis. The major difference between the attempt to penetrate the market with FPGAXpress and the current one seems to be technical, because the new prod-

uct is a true clone—not a derivative—of Design Compiler. Design Compiler provides approximately 80% of the DC FPGA code, whereas the remaining code is a new Adaptive Optimization module that processes the generic-cell netlist to the target FPGA family. DC FPGA compatibility with Design Compiler enables the integration of the prototyping flow within the ASIC-development flow. DC FPGA accepts the same RTL code, constraints, scripts, and IP (intellectual-property) libraries as Design Compiler and provides the same interface to the Formality formal-verification product.

Although Synopsys mentions only ASIC prototyping as its intended market, designers targeting leading-edge FPGA devices could use DC FPGA as the synthesis tool in their development flow. Prices for a stand-alone license of DC FPGA start at \$36,750 for a one-year technology-subscription license. Users of Design Compiler may purchase an add-on DC FPGA license for \$19,600 for a one-year technology subscription license.—by Gabe Moretti

►Synopsys, 1-650-584-5000, www.synopsys.com.

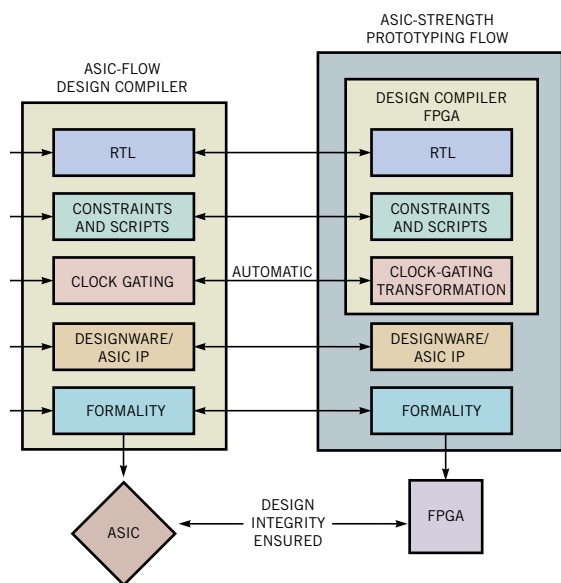
FABRIC STANDARD SUPPORTS SAR LAYER, ETHERNET NETWORKING

The RapidIO Trade Association recently released details about its new Rapid-Fabric extensions, which build upon the transport mechanisms of RapidIO to replace proprietary fabrics. A data-streaming logical layer supports SAR (segmentation and reassembly); virtual streams for flow identification; an efficient logical protocol; traffic management for end-to-end flow control for millions of streams with 256 traffic classes; and internetworking of Ethernet, Utopia, SPI-3, SPI-4, and CSIX, among others.

The fabric includes multicast capabilities and extends the physical layer of the specification to higher speeds. The road map for the new specification targets the second quarter for completion of encapsulation and networking details and the fourth quarter for traffic management. Products conforming to the new extensions will become available in 2005.

—by Nicholas Cravotta

►RapidIO Trade Association, www.rapidio.org.



Design Compiler FPGA targets designers who prototype using FPGAs.

DILBERT By Scott Adams



►Fundrace.org, a six-month-old Web site, lets users plug in any address and retrieve a list of all the campaign donors in the neighborhood and the names of their favored candidates; the site attracts as many as 150,000 visitors a day.—The New York Times, May 20, 2004

Math, simulation updates offer new programming tools, faster development

AS IS ITS custom, The MathWorks has announced a new release that encompasses all of its products. Of these, the two best known are Matlab, the flagship mathematical and technical-computing package, and Simulink, the dynamic-system-simulation and embedded-system-development package. With this release, the revision level of Matlab goes to 7, and the revision level of Simulink goes to 6. The price for Matlab 7 starts at \$1900; the price for Simulink 6 starts at \$2800.

Matlab 7 offers built-in support for integer and single-precision floating-point math, as well as language features that handle larger data sets. To improve application perfor-

mance, the new version implements many optimizations across data types, operators, functions, and hardware. Also new is an enhanced compiler that supports the full Matlab

language, enabling developers to deploy many more applications that run independently of Matlab.

Among its new programmer-productivity capabilities,

Matlab 7 features a redesigned desktop that includes new programming and debugging tools, automatic creation of code-quality reports, and publishing of code and graphics directly to HTML and Microsoft Word. New interactive point-and-click plotting tools enable faster and easier creation of graphics, including the generation of code that automatically re-creates plotting sessions for later use or redistribution.

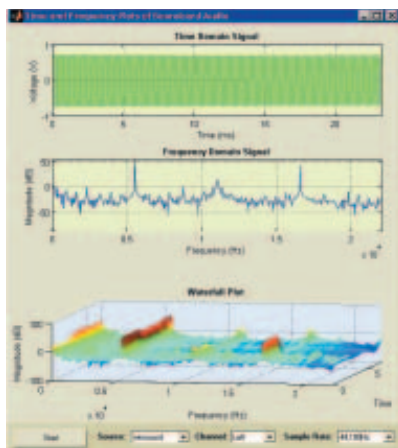
The new features of Simulink 6 enable fast-

er development, eliminate manual-coding errors, and facilitate innovation and exploration in control and signal-processing-system development. Simulink 6's new features support the development of large-scale, real-time embedded systems. Component-based modeling and unified data-management capabilities enable design teams to work efficiently on multiple configurations and subsystems within and across organizations.

Simulink 6 also enables engineers to model, simulate, and implement more types of systems, including RF electronics for wireless, video, and image-processing applications and digital filters implemented in VHDL and Verilog. With the new package, engineering teams can also design, implement, and verify systems that consist of fixed-point hardware and software.

—by Dan Strassberg

►The MathWorks, www.mathworks.com.



This spectrum-analysis application, developed in Matlab and deployed with the package's compiler, runs outside Matlab. The application processes and displays signals that a data-acquisition board acquires.

Tool measures impact of software on power use

THE EXECUTION SPEED available in chips fabricated with the latest process technologies allows engineers to use software programs instead of dedicated hardware systems to implement many of the functions an application requires. Yet, one of the drawbacks of using software is that this approach often requires more power than an equivalent hardware implementation due to the demands of using a memory subsystem. Knowing how much power a given block of code requires is important to designers. To address these issues, a new company, PowerEscape, has introduced PowerEscape Analyzer and PowerEscape Analyzer+Cache to help system architects and software developers to estimate the amount of power software routines consume.

PowerEscape Analyzer works with any ANSI C-compliant software module compiled using GCC (Gnu C Compiler) 2.95 or higher and produces detailed reports on the memory subsystem's memory access and energy consump-

tion, pinpointing the source code that causes the most costly data transfers. The tool also records the source-code location at which memory use peaks, along with data structures in memory at that time. The Analyzer+Cache tool works with the Analyzer and provides simulation of L1, L2, and L3 caches in a variety of configurations.

The feedback on data-transportation bottlenecks and cache behavior aids designers in balancing the costs of developing dedicated hardware circuits with the need for shorter implementation times and system flexibility and upgradability. A one-year single-user license for PowerEscape Analyzer has a list price starting at \$10,000, and the list price for the equivalent license for PowerEscape Analyzer+Cache starts at \$25,000. Both products run under Linux, Solaris, Windows using Cygwin, and Apple Mac OS X.—by Gabe Moretti

►PowerEscape, 1-360-753-5999, www.powerescape.com.

►On a typical corporate-software project employing 40 programmers for a year, the savings from offshore outsourcing in India would be 20 to 40% less than employing higher priced labor in the United States, estimates Joseph Feiman, an analyst at Gartner Inc.

—The New York Times, Dec 22, 2003

System targets WLAN verification in design and on site

TOOLS FOR VERIFYING the proper operation of wireless LANs have mostly targeted the deployment phase, in which developers assume that the system design is sound, despite the fact that many location- and configuration-specific problems can still prevent proper operation. Designers of new WLAN hardware and protocols have been more or less on their own, however; the lack of test equipment intended for design verification and debugging has forced these engi-

neers to assemble setups from general-purpose equipment. Such setups are often bulky, expensive, difficult to make work, and tedious to use, and they often present results that are ambiguous, unrepeatably, or difficult to interpret.

Less than two years old, VeriWave has taken as its mission the creation and manufacture of test equipment for this challenging application. The company bills its \$74,000 WaveTest system as the first true IEEE 802.11 protocol-test system to provide complete conformance testing, the most accurate 802.11 protocol and timing analysis, and the ability to perform tests at every stage of WLAN development.

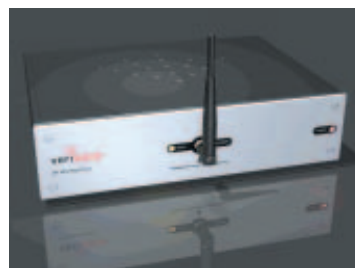
The WaveTest system, which comprises Test Points, lightweight PC-controlled units, can operate in a shielded lab environment, in cabled configurations, or in open air. It fully tests

WLANs' function, timing, and spatial features for compliance with the 802.11 standard and is appropriate for use in design, manufacturing,

quality assurance, and on-site customer support.

—by Dan Strassberg

►VeriWave, 1-503-473-8350, www.veriwave.com.



The PC-controlled WaveTest system uses these lightweight Test Points in either a cabled or an open-air configuration to verify the protocol compliance and timing of IEEE 802.11 wireless LANs.

Dude, where's my system?

PARVUS CORP recently announced the OrbiTrak 8R GPS (global-positioning-system) receiver for automotive, marine, and airborne PC/104-embedded-computer systems. Supporting National Marine Electronics Association 0183, Trimble ASCII Interface Protocol, and binary-GPS data formats, the board includes an eight-channel Trimble Lassen LP GPS module, two TTL serial ports, 16 digital I/O lines, external battery backup, an odometer input, and a clock input.



The OrbiTrak 8R provides GPS location data for vehicle-navigation, telematics, and fleet-management applications in a rugged, PC/104 form factor.

The PC/104 form-factor module interfaces with the host computer through a standard 16C550-compatible UART to provide a direct connection to most commercial-navigation- or map-software packages. The OrbiTrak 8R is currently in stock and sells for \$239 each (100 or more).

—by Warren Webb

►Parvus Corp, 1-801-483-1533, www.parvus.com.

Libraries turn math algorithms into intellectual property

MANY COMMUNICATION AND GRAPHICS applications are computation-intensive, yet no one has paid much attention to optimizing the hardware that implements mathematical functions. Traditional implementation methods use a combination of pipelining, manual gate- or circuit-level design, or automatic synthesis with special constraints. Turning an equation into a numerical implementation is difficult because it requires a special knowledge of both numerical analysis and hardware design.

Aiming to eradicate this oversight, start-up Arithmatica has developed CellMath libraries and support services that provide optimized arithmetic modules. The company based the CellMath modules on fast carry-propagate logic, fast parallel counters, and better floating-point and SIMD (single-instruction multiple-data) computational operations.

The CellMath product line includes libraries for configurable instances, graphics applications, and processor design. Engineering-support services include development of new instances, custom design of cells, and logic- and transistor-level designs. Customers, for example, can generate the required permutation of floating-point-product and multiply-accumulate configurations that also include gate-level netlists and bit-accurate simulation models. Designers can tailor each function for bit-width, speed, and area goals; pipelining; and internal precision.

Arithmatica licenses the CellMath graphics library, processor library, and configurable instances for \$175,000. The licensing model includes a project-based, non-royalty-free pricing structure.—by Gabe Moretti

►Arithmatica, 1-650-632-4542, www.arithmatica.com.

►The overall market for PBXs (private-branch exchanges) will grow at a 4.2% compound-annual-growth rate between 2003 and 2008, according to InStat/MDR.

Hardware accelerator compiles at 50 million RTL gates/hour

FUNCTIONAL TEST SUITES or pseudorandom test vectors are still the two most popular forms of design verification. To realize the im-

pressive computational capabilities these techniques require, engineers use compute farms that employ tens or hundreds of networked CPUs. Engineers use hierarchical methods to limit the size of the design they need to debug, but they sometimes must simulate the design to obtain an accurate picture of how it will function.

To perform this task, the Hammer 100 hardware accel-

erator from Tharas Systems compiles Verilog, VHDL, or mixed-language designs at 20 million to 50 million RTL-gate equivalents per hour on a single workstation. The product complies with the IEEE 1364-2001 Verilog and IEEE 1076-2002 VHDL standards. To increase engineering efficiency, the system allows incremental compilation so that only the portions of the design that have changed require

recompilation. Engineers can incrementally change both the design and the testbenches. The Hammer 100 includes as much as 4 Gbytes of memory and hundreds of built-in arithmetic operators to further speed common computational functions in numerical-analysis, graphics, and DSP applications.

To provide efficient visual feedback, the product converts the simulation results into a number of formats, including VCD (value-change dump) and VPD (VCD-post-processing data). The Hammer 100 concurrent-waveform-conversion capability

compresses the trace data and concurrently converts it into waveforms. Designers can start to debug a design with the existing portion of the waveform while the simulation continues and the product generates new waveforms. The price of the product starts at \$150,000 for a 2 million-RTL-gate-equivalent configuration and depends on the user configuration. The product supports both Solaris and Linux operating systems and is also available through a rental program.

—by Gabe Moretti

► **Tharas Systems**, 1-408-855-3200, www.tharas.com.

32-channel, 40-MHz pulse-pattern-generator board works with seven logic families, stores 4-Gbit patterns

STRATEGIC TEST'S ULTRAFAST UF7221, a 32-channel, 40-MHz pulse-pattern generator, whose output is compatible with ECL, PECL, TTL, LVDS, LVTTTL, CMOS, and LV-CMOS logic levels, fits onto a full-length PCI card, which costs \$5290. For that price, the manufacturer equips the unit with 128 Mbits of pattern memory, whose width you can configure in 4-bit increments. When you select the pattern width, the board automatically configures its memory to provide the greatest possible pattern depth. Four-bit-wide patterns are thus 32 Mbits deep, and 32-bit-wide patterns are 4 Mbits deep. The largest memory—4 Gbits (\$12,717)—can store 32-bit-wide, 128-Mbit-deep patterns or narrower patterns of greater depth. A 6U CompactPCI version, UC7221, and a 3U PXI version, UX7221, are also available.

You can separately program the output levels of each 4-bit output group in 10-mV increments from -2 to +10V. Each channel supplies as much as 100 mA to a maximum of 200 mA per 4-bit group. You can also separately configure each 4-bit group to produce single-ended or differential outputs. Choosing a differential configuration—for example, to drive LVDS or ECL inputs—does *not* reduce the number of channels in the group.

Prices include software drivers for Windows XP, 2000, NT, ME, 98, and Linux; drivers for The MathWorks' Mat-

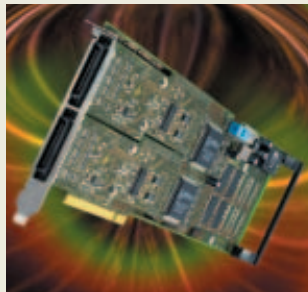
Lab, National Instruments' LabView and DasyLab, and Agilent's VEE (www.mathworks.com, www.ni.com, www.agilent.com) are available at additional cost.

The board has two operating modes. In the standard mode, you transfer data to the onboard memory before starting the output. In this mode, you can use all 32 channels at the maximum 40-MHz output rate. The FIFO mode uses the card's PCI-bus-master capability to continuously transfer data from the PC to the card during output, allowing generation of patterns deeper than the available onboard memory. In either mode, the board can repeat patterns much faster than traditional IEEE-488-based pattern generators, whose maximum data-transfer rate from the host PC to the instrument is typically 1 Mbyte/sec.

—by Dan Strassberg

The UF7221 unit offers many unusual features, including programmable output levels, compatibility with the inputs of seven logic families, and memory depth as great as 4 Gbits.

► **Strategic Test Corp**, 1-617-621-4010, www.strategic-test.com.



► **The technology and communications industries spent more than \$111 million on lobbyists in the second half of 2003, according to data compiled by the campaign-finance site PoliticalMoneyLine.**

Test suite measures protocol compliance

As SOC (system-on-chip)-design complexity continues to grow, the verification effort expands rapidly and continues to account for at least half of the development cost of a new product. This problem becomes worse when chip designs incorporate complex serial protocols, such as PCI Express. Chip designers require specialized approaches to verifying compliance with complex protocol standards and interoperability with other cores on chip or with de-

vices in the final system.

To address these problems, Denali Software has introduced the PureSuite verification package, which exercises PCI Express designs and measures both compliance with the specification and interoperability with other PCI Express designs. PureSuite covers the entire PCI Express specification, including all items in the Compliance Checklist document from the PCI-SIG (PCI Special Interest Group). The tests cover all aspects of the

specification—from physical layer, data link, transaction layer, and configuration space to initialization and power management. Tests use both compliant and noncompliant traffic to measure error-recovery capabilities.

Each test covers checklist items and details a description of purpose, assumptions, scenario, expected results, and corresponding PCI-SIG checklist-item number. Engineers can drive tests from PureSpec, a companion product to Pure-

Suite, across the PCI link toward the design under test, or they can initiate them from the application interface of the design under test. PureSuite maintains a cumulative report of compliance results listing the pass-or-fail status for all tests. PureSuite's list price is \$50,000 per year per project. The product operates on all major platforms.

—by Gabe Moretti

► **Denali Software Inc**, 1-650-461-7200, www.denali.com.

Can you C acceleration?

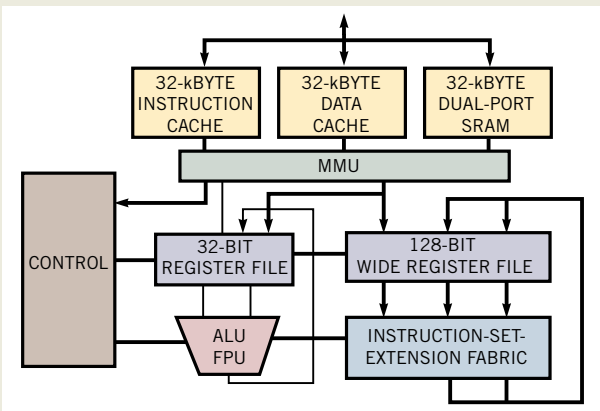
THE STRETCH S5000 family of software-configurable processors allows you to create hardware-acceleration blocks and extend the processor-instruction set of an Xtensa-based RISC-processor core based on your application's C/C++ code. User-defined instruction extensions reside within the ISEF (instruction-set-extension fabric), which is a proprietary programmable-logic block that interlocks and interfaces with the RISC-processor pipeline. The Stretch C compiler implements the hardware-acceleration blocks by analyzing the C/C++ code that you manually mark after profiling your code and identifying the performance hot spots. Stretch intends the C compiler to be

the only tool for implementing the hardware-acceleration blocks, so you may have to manually restructure your target C/C++ code, based on a set of guidelines from Stretch to assist the compiler to squeeze the most performance from a block of marked code. Instrumenting your software source code so that the compiler can optimize how it implements the hardware-acceleration blocks does not break the portability of your code.

Stretch has not disclosed the organizational details of the ISEF, which accesses data through a 32×128-bit register file using three 128-bit input paths and two 128-bit output paths. The wide register file tightly couples with the Xtensa registers and memory. The Stretch C compiler creates and schedules the user-defined instructions in the ISEF so that they are fully pipelined and interlocked with the Xtensa core so that instructions that cannot complete in one cycle are spread over the necessary number of cycles.

The S5610 is the first of three devices in the S5000 processor family that will be available this July for \$100 (10,000). The S5500 and S5400 are lower cost devices that will become available in the months following the availability of the S5610, and they will offer the same S5 processor engine and memory resources, but they will include fewer integrated I/O peripherals and interfaces, and they will come in smaller packaging. The S5610 operates at 250 or 300 MHz and includes 256 kbytes of on-chip SRAM, an MMU, 64-bit DDR-400 SDRAM with ECC, PCI-X, 64-bit SysAD, and four 10/100/1000 Ethernet MACs (media-access controllers).—by Robert Cravotta

► **Stretch**, 1-650-864-2700, www.stretchinc.com.



C-derived custom instruction extensions reside in the instruction-set-extension fabric, which is a proprietary programmable-logic block that provides interfacing and interlocking with the processor core.

► **Worldwide unit shipments of personal video recorders grew from 1.5 million in 2002 to 4.6 million in 2003. In 2004, shipments will top 11 million and will reach 40 million by 2008, according to InStat/MDR.**

Easy bridge for Ethernet to RS-232

By Graham Prophet

If you have an application that you need to “put online,” to add Ethernet connectivity but you are not yet ready to do a board revision to incorporate a port such as Lantronix’s X-Port (www.lantronix.com), you may find a module from Alphamicro useful. The Netport is, in effect, a packaged X-Port, an external solution that bridges Ethernet and serial-port standards. It can also be used to provide an additional COM port on an existing PC-based system. It provides an embedded Web-server function and e-mail client so that applications can send notification and reports by SMTP. You can power it from a line adapter, and it has reserves to feed power to an application device, or it can draw power from the RS-232 socket using the unallocated Pin 9. It ac-



Plug-and-play serial-to-Ethernet connectivity can let you develop connected applications ahead of integrating an Ethernet port.

cepts 5 to 24V dc and uses about 180 mA. It also has a built-in voltage regulator, and you can daisy-chain a few such devices.

Netport comes with software utilities, such as a COM-port redirector. You can configure it via your application,

or by a Telnet window, or via the Web server, setting parameters such as speed, flow control, and port ID. Achieved data rates are 230 kbps, with a faster version to come. Netport will sell for around €100. **▶Alphamicro**, +44 1256 851770, www.alphamicro.net.

ColdFire updated with real-time subsystem

On May 5, Motorola Semiconductors was rebranded as Freescale Semiconductor—a Motorola subsidiary pending a forthcoming IPO to float Freescale as a separate company.

In one of its first announcements, the company introduced an extension to the ColdFire-processor line—12 new devices in the MCF547x and 548x number sequences. Employing the V4e ColdFire core, the processors aim at the mid to high end of embedded 32-bit control applications and feature a range of connectivity options, plus the enhanced timing processor unit, or eTPU. This dedicated, real-time-control coprocessor handles tasks such as high-speed I/O, freeing up the main processor and reducing its burden of interrupt servicing. You could use it in motor control, or you can set it up to look like a serial interface using a standard high-speed protocol. In its maximum configuration, the 548x has dual CANbus and dual Ethernet support; 547x is better suited for use as a networked device with its twin Ethernet controllers.

Options include flash/flashless devices and advanced security and encryption features. Freescale sees the part being used in applications that bridge the industrial-control and IT worlds, such as building/HVAC/access control; memory-management and floating-point options support multi-threaded Linux. Encryption support extends to protection of software IP, with decryption at the instruction level.

Freescale has also introduced the 523x family, this time using the V2 core with a 16/32-bit eTPU option; you typically use these parts, the company says, for motion control. For both families, the company will introduce a library of pre-coded application segments using the eTPU, and the code will be available on the company’s Web site. With the 523x (which you can think of as an upgrade to the 68332), you get 144 MIPS max at 150 MHz; the 54xx parts offer 410 MIPS max at 266 MHz.—by Graham Prophet

▶Freescale Semiconductor, e-www.motorola.com.

A presence in the configurable DSP sector

ARM's OPTIMODE is a configurable core based on technology acquired from Philips (out of the former Adelante, which had acquired the technology from Frontier Technology). Noting that standards are becoming "less standardised" (for

example, witness the many varieties of video codecs). ARM describes the offering as a framework that produces a data engine, which you can program to run multiple variants of an application. The vendor also says you should view it as a configurable core plus tool set, rather than as a tool-based offering. The approach is algorithmcentric—you are configuring a signal-processing datapath using a VLIW-based approach with instruction lengths of 16 to 256 bits.

The tool set works from a base library of DSP functions and produces a C compiler for the resulting engine. You can trade silicon area, clock speed, and bit width for an optimum result in the design flow. You get a set of 14 typical starting configurations on

which to build a design, which act as seeds for the optimisation process; size and arrangement of local storage and interconnect are also fully configurable. Profiling tools examine the operation of your code in a given configuration, identifying remaining areas for improvement and directing the optimisation. You can output to Verilog or to FPGA configuration code; a "shell" around the data engine handles interfacing to a system AMBA bus. An OptimoDE engine core can be as small as 9500 gates and can implement a 128-point FFT in 226 clock cycles.

In a separate announcement, ARM offered multiprocessing support with a synthesisable multiple core, the MPCore. The aim is to provide improved system-re-

sponse time in complex multithreaded applications; with fewer processes running on any given core, you'll get quicker attention from the hardware. You can invoke four ARMv6 cores in an instance of MPCore, but the unit of IP remains the complete MPCore. It supports hybrid symmetry; that is, it can run symmetrical and asymmetrical multiprocessor code at the same time. You can therefore support existing asymmetric applications while writing newer code in a fully symmetric fashion. In the (up to) four-way cache structure, dedicated hardware maintains coherency. The MPCore looks to SOC design tools like a dual-AMBA-structured uniprocessor and is configurable with respect to the number of CPUs and interrupts and to whether floating-point support is included. The device has broadcast modes that software can use to address all CPUs within the processor, and it offers full software control of interrupts directed to the cores.

—by Graham Prophet
 ▶ARM, +44 1223 400400,
www.arm.com.

Configurable supply reaches for new efficiency levels

IN THE SEARCH for ever-higher efficiencies in the power-conversion chain, Lambda has turned its attention to the ac/dc (offline) multiple-output power supply. With the introduction of the NV series, the vendor uses a new topology with reduced switching losses. As efficiencies rise to 90% and above, companies are making incremental gains by paying attention to the fine detail of tracking the energy through every part of the switching cycle; the NV is no exception. It uses a topology based on synchronous rectification in a resonant mode. Previous configurable Lambda products used a magnetic-amplifier-based architecture and were config-

urable by adding discrete secondary windings to the main isolation transformer. This series, however, is structured as an ac/dc converter (to 400V) configurable by adding dc/dc converters as required.

First units in the range have 175 and 300W; a modular 600W unit will follow. For compatibility with 1U rack-mount applications, the units measure 95 mm high. The design uses reduced-value inductors for lower losses, multilayer ceramic capacitors in inductor-less filters, and silicon-carbide diodes in the power-factor-correction input stage, all leading to increased efficiency. Other gains the vendor claims for the design are reduced cooling re-



Component selection and switching control yield configurable power-supply efficiencies of 90%.

quirements (the 350W unit has small twin fans, and the 175W device has an open

frame and is ambient-cooled), lower EMI, and preapproval for medical-equipment standards. You can specify up to three single- or dual-output modules on the 350W version, spanning 3.3 to 32V, with 2 to 40A output-current ratings. The nonconfigurable, open-frame supply can provide as many as five outputs from 0.9 to 15V, 1 to 25A, with all outputs regulated. You cool it with forced airflow, and you can derate it to fully convection-cooled. Resulting overall energy densities are 6.6 and 9.36W/in³, respectively, for the two supplies.

—by Graham Prophet
►Lambda, +44 1271 856666, www.lambda-europe.com.