

Edited by Bill Travis and Anne Watson Swager

Missing-codes tester checks 16-bit ADC in 7 sec

Mark A Shill, Burr-Brown Corp, Tucson, AZ

AS THE RESOLUTION OF ADCs increases from 12 to 16 bits and higher, the difficulty in testing the “no-missing-codes” specification grows proportionately. To fully guarantee no missing codes for a 16-bit ADC requires testing all $2^{16}-1$ possible output codes. Undertaking such a production test could add much extra cost to the ADC without a quick method for testing all codes. Fortunately, a simple approach can test the no-missing-codes specification for a 16-bit ADC—in this case, a 10- μ sec ADS7805, in typically less than 7 sec (Figure 1).

This missing-codes tester comprises an analog ADC servo loop that you can also use to measure the integral nonlinearity and differential nonlinearity of 16-bit ADCs (Reference 1). The servo loop works by finding the ADC’s input voltage that corresponds to the Code_{*i*}-to-Code_{*i+1*} output transition. The circuit uses an 18-bit DAC729, IC₁, as a pedestal DAC to quickly set the input voltage to the ADC

under test to approximately the level corresponding to the programmed input code. The output transfer function of the pedestal DAC matches the transfer function of the ADC under test—in this case, $\pm 10V$ for the ADS7805. The DAC729 MSB bit-adjustment pins, pins 36 to 40, are open because the unadjusted DAC729’s linearity is sufficient for performing only the ADC missing codes test.

The procedure successively tests each possible output code of the ADC under test by programming a PC with the desired 16-bit code, Code_{*i*}. Applying a 100-kHz clock to pin 24 of the ADC provides for continuous operation of the ADS7805. When the ADC completes a conversion, two 8-bit 74HC682 magnitude comparators, IC₂ and IC₃, and accompanying interface logic, IC₄ and IC₅, compare the ADC’s output code to the programmed data-bus code. The signal output from IC_{4A} signifies whether the input voltage to the ADC needs to increase or decrease to achieve an ADC output equal to the programmed Code_{*i*}. The signal from IC_{4B} indicates whether the output code from the ADC matches Code_{*i*}; a logic-low level indicates that the code was found.

Because both the $\overline{P>Q}_{16}$ and $\overline{P=Q}_{16}$ signals from IC_{4A} and IC_{4B}, respectively, can be momentarily indeterminate during the ADC conversion, the circuit latches these signals into flip-flops IC₆ and IC₇ when the conversion is complete. The clock signal for these latches is a delayed version—approximately 200 nsec—of the rising edge of the ADS7805 end-of-conversion signal, BUSY. The circuit uses the $\overline{P>Q}_{16}$ signal clocked into IC₆ to control the ramp direction of integrator op amp IC₈. The 0 to 5V output of HC-type flip-flop IC₆ directly drives the integrator

input of IC₈. R₁, R₂, and the $-15V$ power supply shift the 0 to 5V output level to approximately -2 to $+2V$. C₁ filters any high-speed transients that arise from the switching action of IC₆’s output.

Op amp IC₉ attenuates the integrator’s output by 100 and sums the result with the output of the pedestal DAC. For the component values of IC₈’s integrator stage, the maximum ramp rate at the input of the ADC is approximately 2 $\mu V/\mu$ sec, which is equivalent to 0.067 LSB per conversion. Feedback of the servo-loop circuit maintains the dc level of the integrator’s output by continuously adjusting the input voltage of the ADS7805 to the level required for the Code_{*i*}-to-Code_{*i+1*} output transition. Thus, the servo-loop circuit locks in the input voltage to the ADC to maintain the Code_{*i*}-to-Code_{*i+1*} output transition.

The $\overline{P=Q}_{16}$ signal that the circuit clocks into flip-flop IC₇ indicates whether the programmed Code_{*i*} exists for the ADC under test. The output of IC₇ connects to an input control line, CNTL₆, on the controlling PC’s I/O card. After the control program sends each new Code_{*i*} to the tester, the PC reads the state of CNTL₆. A high level on CNTL₆ indicates that Code_{*i*} exists and is not missing.

ALIGN PEDESTAL DAC WITH ADC UNDER TEST

Before starting the missing-codes test, the procedure requires alignment of the pedestal DAC’s endpoints with those of the ADC under test. This alignment ensures that the pedestal DAC’s output closely matches the corresponding ADC input voltage for all codes programmed to the tester. Under this condition, the voltage needed to sum with the pedestal DAC output should be only a few LSBs (referred to the ADC input), thus keeping the dc output level of the integrating op

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amp, IC₈, close to 0V. Thus, for each Code_i setting, the integrator output never needs to slew very far from the dc level of 0V.

Comparators IC_{10A} and IC_{10B} form a window comparator for the output of IC₈. The window voltage is equal to 100 mV, which corresponds to approximately 3.3 LSBs, referred to the ADS7805 input. I/O control lines CNTL₄ and CNTL₅ read the outputs of IC_{10A} and IC_{10B}, respectively to determine the level of the integrator's output voltage. If CNTL₄ is high, the integrator output is more than 100 mV. If CNTL₅ is high, the integrator is less than -100 mV. If both CNTL₄ and CNTL₅ are low, the integrator output is

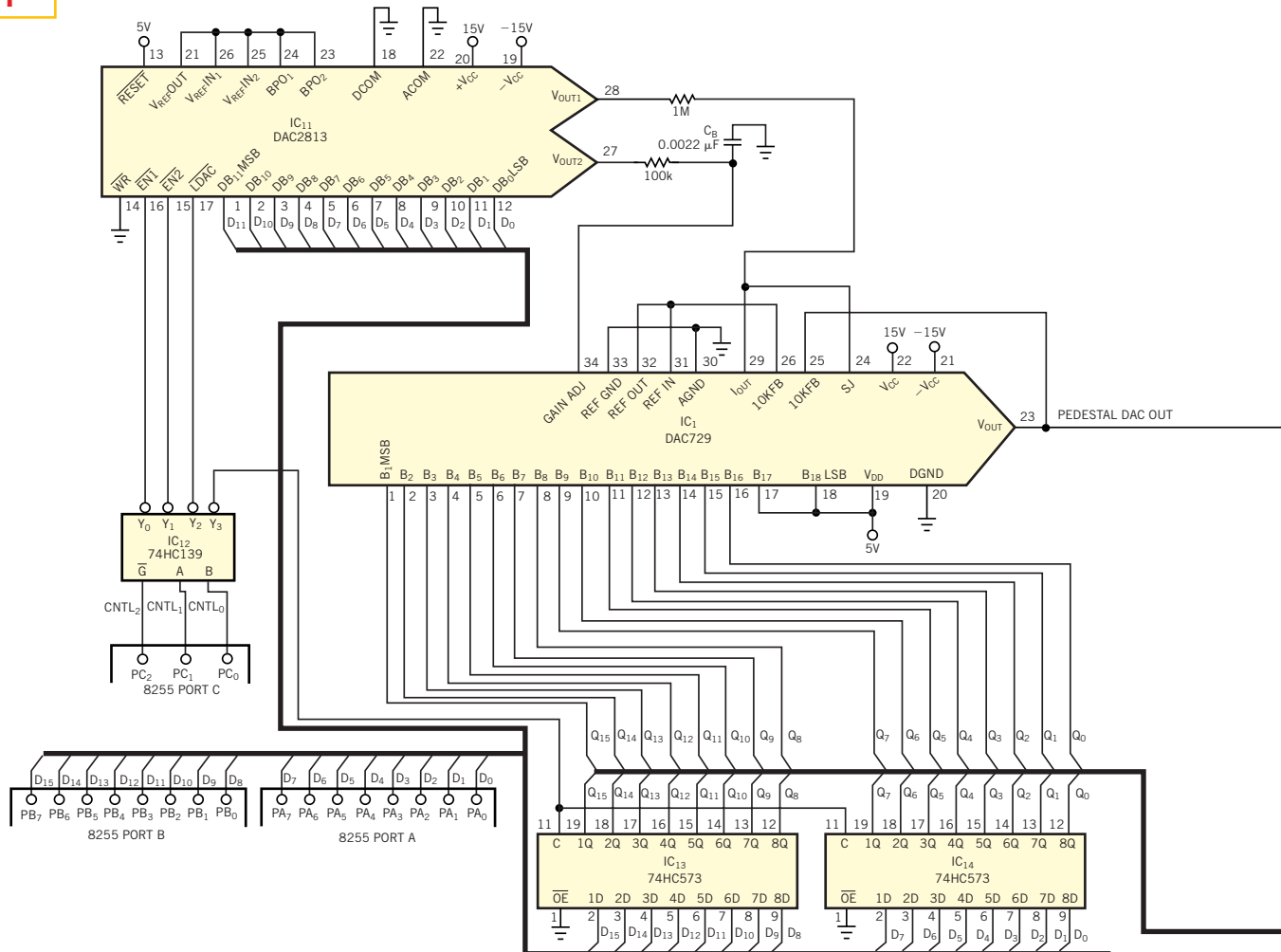
within the 100-mV window.

A dual, 12-bit latched DAC, IC₁₁, adjusts the pedestal DAC's endpoints. V_{OUT1} and V_{OUT2} adjust the pedestal DAC's offset and gain, respectively, to the endpoints of the ADC under test. First, the control program adjusts the DAC729's offset by programming and latching Code_i to FFFE (hex) and then counting up or down accordingly so that V_{OUT1} brings the integrator voltage within the 100-mV setting of the window comparator. Next, the program sets IC₁₁'s gain by programming and latching Code_i to 0000 and again counting up or down so that V_{OUT2} brings the integrator output to a null.

The same I/O data bus programs both the DAC2813 and the 74HC682 digital comparators. The 74HC139 decoder, IC₁₂, selects either the input Code, latches, IC₁₃ and IC₁₄, or the internal latches of the DAC2813. IC₁₁ has two input-latch-enable pins, one for each of its output DACs. Input $\overline{\text{LDAC}}$ loads the DAC's input latch data into the internal latches, thus simultaneously programming both V_{OUT1} and V_{OUT2}. I/O control lines CNTL₀ and CNTL₁ select the desired latch, and CNTL₂ strobes in the data from the bus.

The listing of the Pascal program for controlling the missing-codes tester is available for downloading from EDN's

Figure 1



An analog servo loop tests for no missing codes by finding the ADC's input voltage that corresponds to the Code_i-to-Code_{i+1} output transition.

web site, www.ednmag.com. Click on "Search Databases/Links Page" and then enter the Software Center to download the file for Design Idea #2334. The section of the program that outputs codes to the data bus and reads the state of the CNTL₆ line is based on a custom I/O card built with an Intel 8255A programmable peripheral interface. The I/O routines are for reference only, and you should modify them according to the protocol used by the user's specific I/O card.

The EndPoints procedure in the listing aligns the offset and gain of the pedestal DAC to that of the ADC under test. It programs IC₁₁ as necessary to null the in-

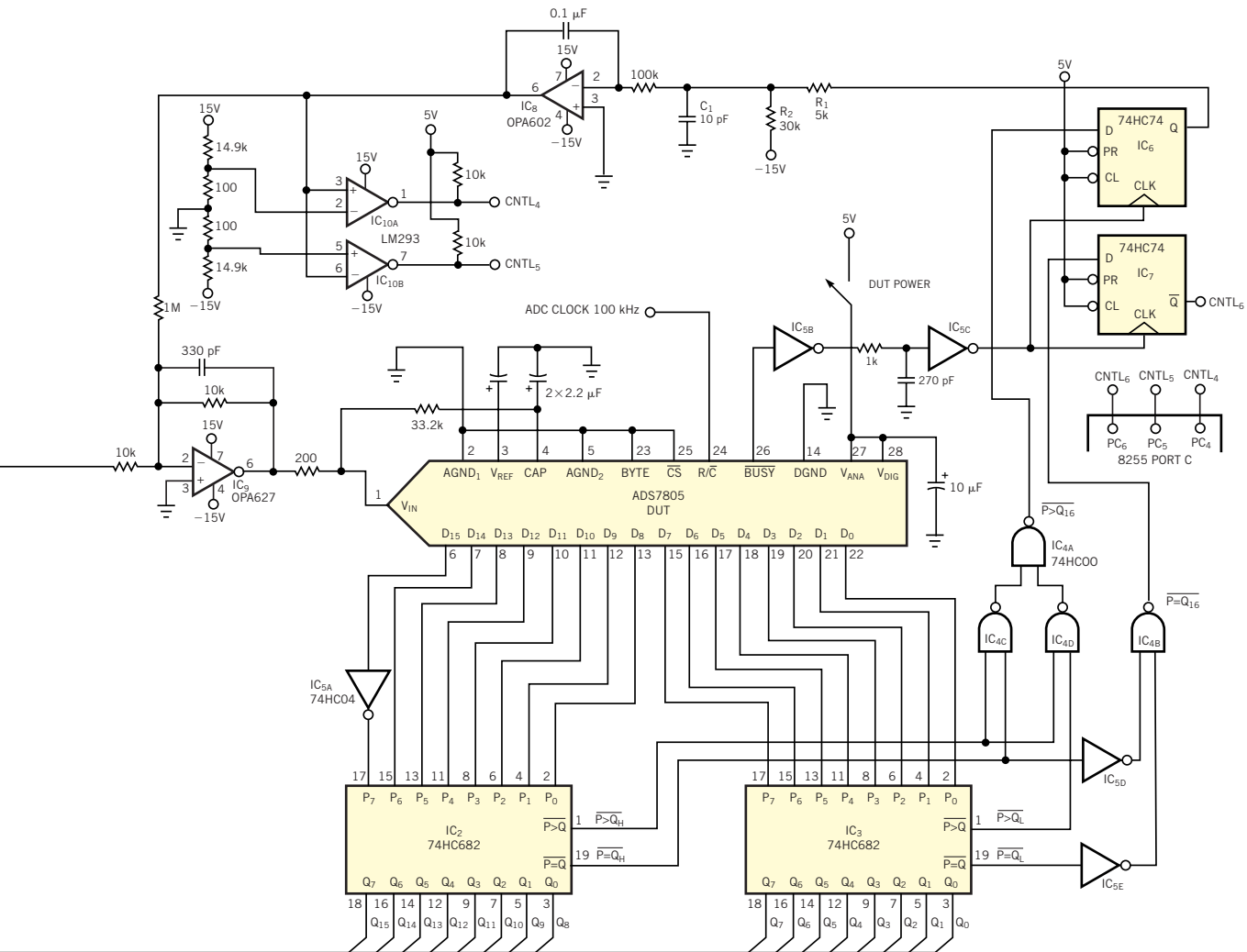
tegrator output for both offset and gain. The Detect procedure programs each Code_i from 0 to 65534, to the missing-codes test board. After programming each new code, the program reads the state of the CNTL₆ line. If CNTL₆ is a logic high, indicating the programmed code exists, the Count variable is incremented. The Detect procedure loops for the given code until a minimum number of occurrences are detected, set by the variable MinCount. The variable MaxTry sets the maximum number of times that the program tries to find Code_i. The program loops for an appropriate delay time to ensure that measurements of the state of

the line occur only once per analog-to-digital conversion or, in the case of the ADS7805, approximately every 10 μsec. For the variable MinCount set to 3 and MaxTry set to 30, the missing-codes tester can test the 10-μsec ADS7805 for all 2¹⁶ - 1 codes in less than 7 sec. (DI #2334)

REFERENCE

1. Shill, Mark A, "Servo loop speeds tests of 16-bit ADCs," *Electronic Design*, Feb 6, 1995, pg 93.

TO VOTE FOR THIS DESIGN,
CIRCLE NO. 415



Switch-mode supply draws 43-mW standby power

Christophe Basso and François Lhermite, Motorola SPS, Toulouse, France

SWITCH-MODE OFFLINE SUPPLIES offer better efficiency than linear supplies. However, the efficiency of a switchmode power supply (SMPS) seriously degrades with light loads, and commutation losses provoke power dissipation well above 1W even with no load. A good way to build a low-standby-current SMPS is to use a hysteretic architecture, which delivers high-frequency pulses until the output passes a threshold and then no pulses until the output again drops below the threshold. The SMPS consumes little energy delivering the refreshment pulses. **Figure 1** shows a circuit that uses an MC34063 controller IC and an insulated-gate bipolar-transistor (IGBT) output device.

The MC34063 operates in current

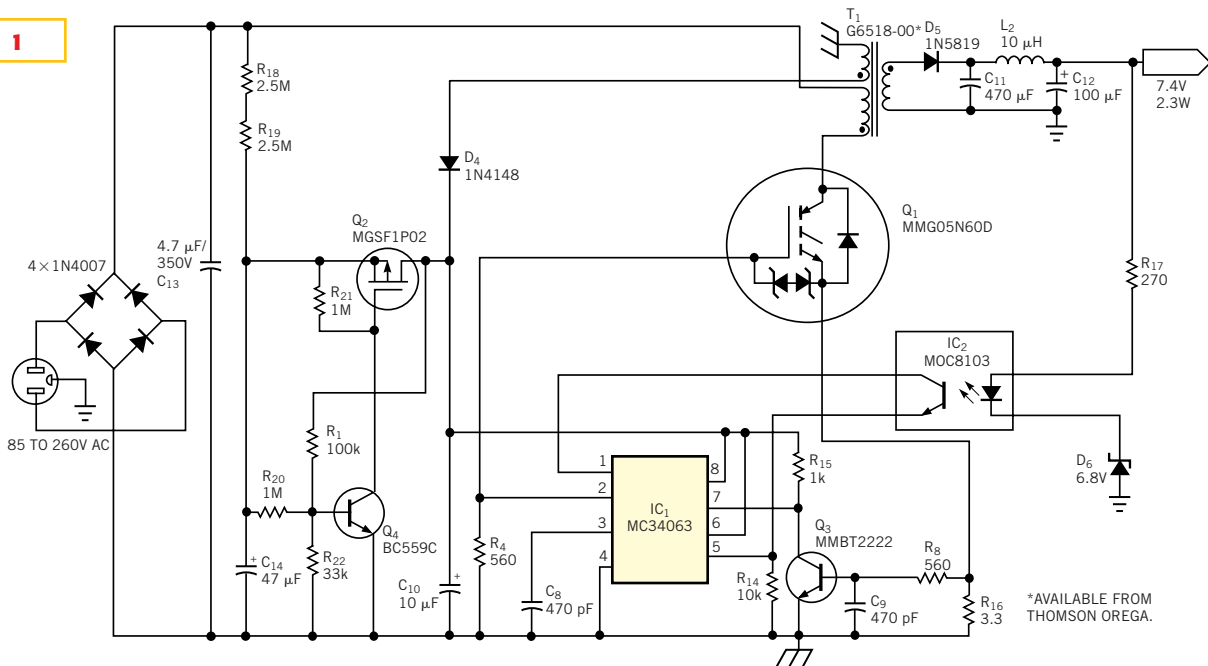
mode. Q_3 trips the IC when the voltage on sense resistor R_{16} drops to approximately 550 mV. ($I_{PEAK}=160$ mA in this example.) You can adjust the peak current to compensate for the transformer's magnetostrictive effects. Any transformer you use in an SMPS produces audible noise at a low frequency. You can either buy an expensive transformer whose construction ensures low audible noise or keep peak current low, as in **Figure 1**'s circuit. When reducing the peak current, you need to increase either the primary inductance or the switching frequency (by varying C_8) to keep the output power constant.

The MMG05N60D IGBT has low parasitic capacitance that degrades efficiency at low peak currents. When you open

the high-voltage switch in a MOSFET-based flyback converter, the peak current does not immediately drop to zero. Depending on the amount of parasitic capacitance, the current keeps circulating while the drain voltage rises, and efficiency suffers. **Figure 2a** illustrates this wasteful behavior in a high-voltage, MOSFET-based switcher. The MMG05N60D IGBT has low parasitic capacitance; its total gate charge at $V_{GS}=10$ V is only 4 nC. **Figure 2b** shows the current in **Figure 1**'s circuit with zero output power.

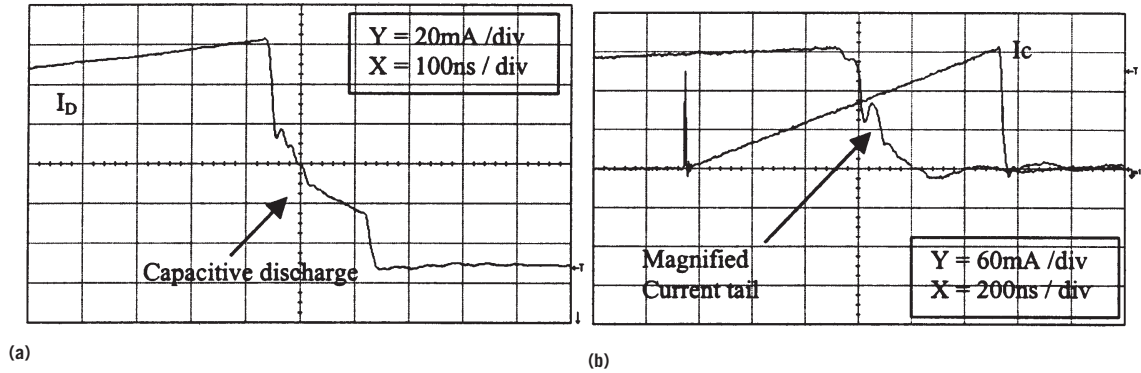
The start-up circuit for the MC34063 uses Q_4 and Q_2 . When you apply the power main, the voltage on C_{14} starts to rise. The ratio of R_{20} and R_{22} causes Q_4 and Q_2 to remain open. The IC receives

Figure 1



A hysteretic architecture in an offline switch-mode power supply makes it possible to achieve less-than-100-mW standby power.

Figure 2



The turn-off characteristic of a lateral MOSFET (a) results in significant wasted power in a no-load condition; lower parasitic capacitance in an IGBT leads to lower dissipation during the turn-off period.

no power, and the current that flows in from C_{14} is small. When the voltage reaches a threshold, Q_4 starts to conduct and pulls Q_2 's gate toward ground. Q_2 's drain voltage rises and strengthens the

conduction in Q_4 . C_{14} rapidly discharges into C_{10} , and the MC34063 oscillates. The circuit offers efficiency ranging from 59.4 to 73%. It dissipates no-load power levels of 42.5, 65, and 82.8 mW at dc input

voltages of 120, 325, and 360V, respectively. (DI #2363).

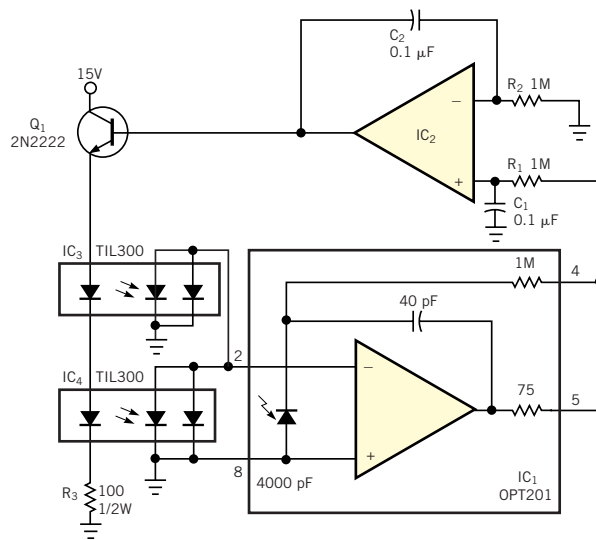
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Circuit rejects ambient light

Massimo Gottardi, IRST, Trento, Italy

IN SOME APPLICATIONS, you need to detect light signals in the presence of background light whose intensity can change by orders of magnitude. The circuit in **Figure 1** uses an integrated photodiode/amplifier (OPT201) in conjunction with an integrator that drives two linear optocouplers (TIL300). The optocouplers subtract the background-light-generated current from the current the optical sensor produces. C_2 integrates any dc signal present at the output of IC_1 . The output of IC_2 drives two optocouplers, IC_3 and IC_4 . The four photodiodes in both TIL300s connect in parallel with the diode in the OPT201 to subtract the dc component from the signal path. IC_3 and IC_4 need 60-mA drive to produce rejection current as high as 1.5 mA. This design uses the optocoupler configura-

Figure 1



The two optocouplers use input-series, output-parallel connections to halve the driving current and double the output rejection current.

tion instead of a simple resistor, because the optocouplers' nonlinear characteristic allows a higher current range without substantially affecting the noise gain of

the transimpedance amplifier. The total output noise in the circuit is 80 μV rms. A 6.8-k Ω resistor can reject the same 1.5-mA dc current, but it produces 200-

μV output noise. (DI #2364).

TO VOTE FOR THIS DESIGN,
CIRCLE NO. 417

V/I converter accommodates grounded load

Michele Frantisek, Brno, Czech Republic

The voltage-to-current (V/I) converter in **Figure 1** uses three common op amps, two medium-power transistors, and only a few passive components. The first op amp (IC₁) inverts the sum of voltages V_{IN} and V_{OUT} to V₁ = -(V_{IN} + V_{OUT}). The second op amp (IC₂) and transistors Q₁ and Q₂ invert this voltage to produce V_{IN} + V_{OUT}. The formula for calculating the output current is thus:

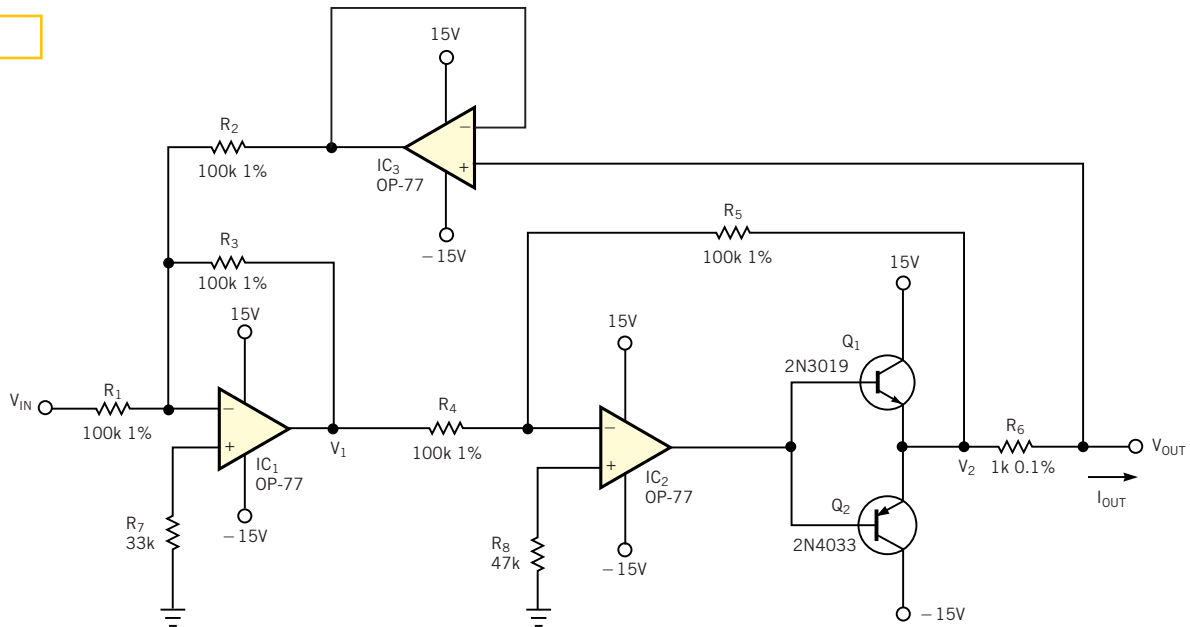
$$I_{\text{OUT}} = \frac{V_2 - V_{\text{OUT}}}{R_6} = \frac{V_{\text{IN}} + V_{\text{OUT}} - V_{\text{OUT}}}{R_6} = \frac{V_{\text{IN}}}{R_6}$$

The formula shows that the value of I_{OUT} depends only on V_{IN} and R₆. Voltage follower IC₃ reduces to a negligible level the current from the circuit output to IC₁. The advantages of the circuit are:

- load-grounding possibility;
- simple control of I_{OUT}/V_{IN} ratio;
- high precision, linearity, stability, and bandwidth;
- wide I_{OUT} range, approximately 1 μA to I_C(max) of Q₁ and Q₂; and
- high output resistance of approximately 50 M Ω . (DI #2365).

TO VOTE FOR THIS DESIGN,
CIRCLE NO. 418

Figure 1



A versatile voltage-to-current converter provides a handy current source in many analog applications.

Digitally controlled potentiometer sets cutoff frequency

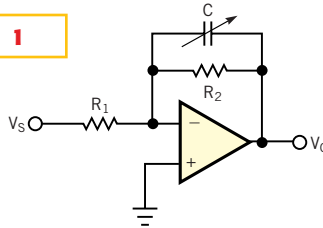
Chuck Wojlaw, Xicor Inc, Milpitas, CA

THE TRADITIONAL METHOD OF controlling the upper cutoff frequency in the basic inverting-amplifier circuit of **Figure 1** is to add capacitor C in parallel with R_2 . The value of C controls the cutoff frequency. R_1 and R_2 independently establish the magnitude of the circuit gain, which equals R_2/R_1 . If you need a variable cutoff frequency, you use a variable capacitor. However, this approach has two major problems: The circuit does not lend itself to computer control, and few variable capacitors are available with values in the nanofarad region.

The circuit in **Figure 2a** is an inverting amplifier that uses a digitally controlled potentiometer and a fixed capacitor as an input Tee network. The magnitude of the gain for this inverting circuit is also R_2/R_1 . However, in this case, R_1 , C, and the location of the wiper along the resistor array of the potentiometer establish the cutoff frequency. The upper cutoff frequency is programmable because the wiper of the potentiometer is under digital or computer control.

Several analysis approaches help determine the circuit gain as a function of frequency. One approach is to use y, or admittance, parameters. If you treat networks A and B as two ports (**Figure 2b**), the ratio of the short-circuit admittance coefficient for the input port, y_{21A} , to y_{12B}

Figure 1



Controlling the cutoff frequency using a traditional inverting amplifier circuit has some limitations, such as a limited selection of variable capacitors.

for the feedback port produces the following gain expression:

$$\frac{V_O}{V_S} = -\frac{y_{21A}}{y_{12B}} = -\frac{\left(\frac{R_2}{R_1}\right)\left(\frac{1}{R_1 C k(1-k)}\right)}{j\omega + \frac{1}{R_1 C k(1-k)}}$$

In this equation, k is a number that varies from 0 to 1 and reflects the proportionate position of the wiper from one end of the potentiometer (0) to the other end (1).

The circuit's gain expression is

$$\frac{V_O}{V_S} = \frac{A_o \omega_C}{j\omega + \omega_C}$$

This equation has the same form as an equation for an amplifier or lowpass filter with a gain of $-R_2/R_1$ and a cutoff frequency of

$$f_C = \frac{1}{2\pi R_1 C k(1-k)}$$

As you program the wiper from one end of the potentiometer to the other, k varies from 0 to midscale ($1/2$) to 1, and the cutoff frequency varies from infinite hertz to a minimum frequency and back to infinite hertz. The minimum frequency is

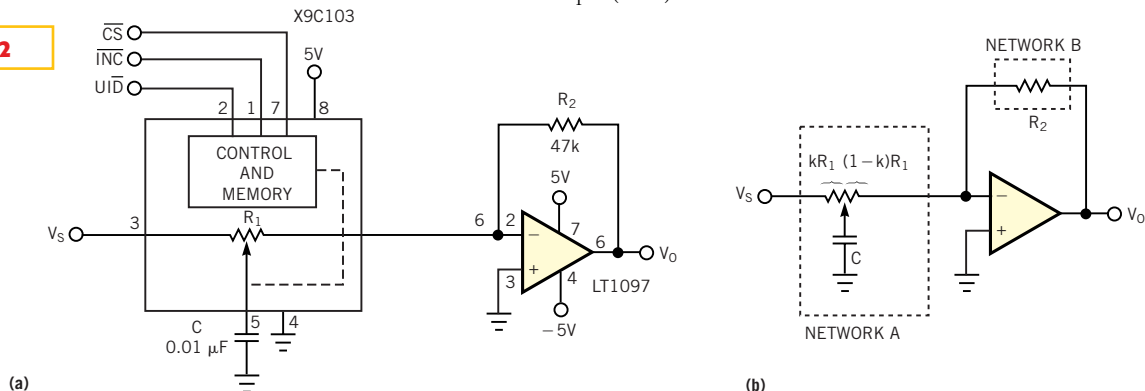
$$f_{C(MIN)} = \frac{4}{2\pi R_1 C}$$

For the XDPC family of digitally controlled potentiometers (Xicor Inc, www.xicor.com), k can vary from 0 to 1. The number of taps or programmable wiper positions determines the resolution. R_1 represents the R_{TOTAL} of the potentiometer. The number of taps varies from 32 to 256, and R_{TOTAL} varies from 1 k Ω to 1 M Ω , depending on the potentiometer. The potentiometer can store a wiper or cutoff-frequency setting in nonvolatile memory, which permits the circuit's cutoff frequency to return to a predetermined value on power-up.

For the circuit in **Figure 2a**, gain is 4.7, and the cutoff frequency varies from 6.4 kHz to a theoretically infinite hertz. The circuit uses a 10-k Ω potentiometer, the X9C103, which has 100 taps and a three-wire interface. The circuit is useful for audio, control, and signal-processing applications. (DI #2367)

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Figure 2



An inverting amplifier that uses a digitally controlled potentiometer and a fixed capacitor provides for a programmable cutoff frequency (a). You can analyze the circuit as a two-port network (b).

Precision reference bans precision resistors

Budge Ing, Maxim Integrated Products, Sunnyvale, CA

COMBINING A SWITCHED-CAPACITOR charge pump with a precision reference yields an inverted reference from a positive power supply (Figure 1). Unlike the more typical combination of a positive three-terminal reference and an op-amp inverter, this circuit performs accurate inversions without the need for precision resistors and a negative supply. The compact circuit requires only three surface-mount capacitors, and the ICs occupy tiny SOT-23 packages.

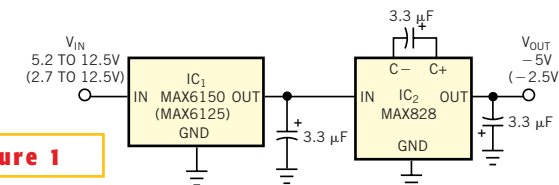
The charge-pump inverter, IC₂, delivers -5V by inverting the out-

put of a 5V precision reference, IC₁. IC₁ has an input range of 5.2 to 12.5V. Replacing IC₁ with a 2.5V reference that accepts 2.7 to 12.5V inputs produces a -2.5V output.

Output-voltage accuracy depends

partly on the initial accuracy of IC₁, which in this case is 1%. To determine the overall accuracy, you must add the error from the dropout voltage, which is less than 2 mV for 90 μA of load current (Figure 2a). For a -2.5V output, the circuit draws quiescent current that ranges from 86 μA for a 2.7V input to 105 μA for a 12.5V input. For -5V outputs, the circuit draws 127 μA for 5.2V inputs and 140 μA for 12.5V inputs (Figure 2b). (DI #2368)

Figure 1



Combining a voltage reference and a charge-pump inverter forms a precision negative reference.

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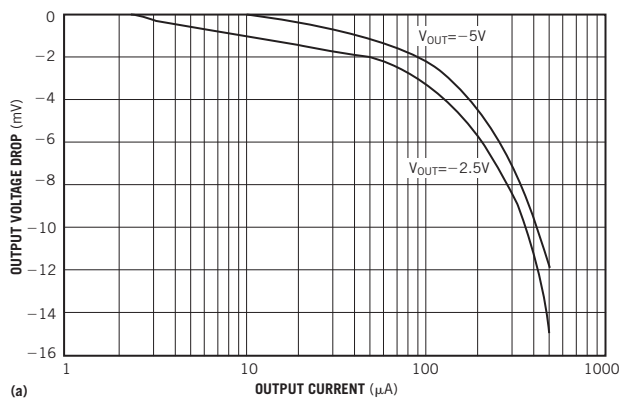
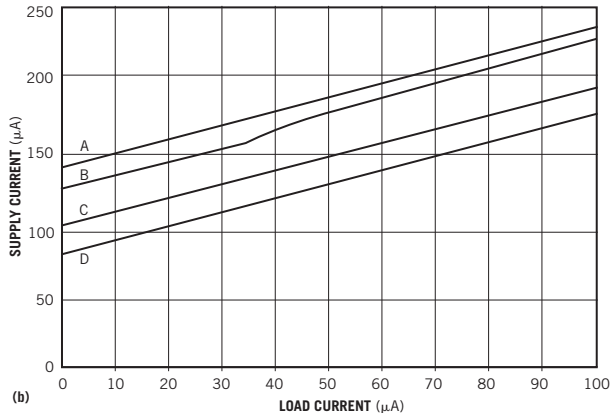


Figure 2



NOTES:
FOR TRACE A, V_{IN}=12.5V, AND V_{OUT}=-5V.
FOR TRACE B V_{IN}=5.2V, AND V_{OUT}=-5V.
FOR TRACE C, V_{IN}=12.5V, AND V_{OUT}=-2.5V.
FOR TRACE D, V_{IN}=2.7V, AND V_{OUT}=-2.5V.

For a -5V output, the dropout voltage is less than 2 mV at 90 μA of output current (a). For a -5V output, quiescent current ranges from 127 to 140 μA.

Easy method calculates comparator trip points

Virgil Lawrence, Micro Linear, San Jose, CA

USING MILLMAN'S THEOREM to calculate the resistor ratio reduces the time it takes to calculate the trip points on a comparator with hysteresis.

This method eliminates lengthy computations and substitutions. Using this resistor ratio, you select two resistors, assign convenient values, and then

calculate the third value.

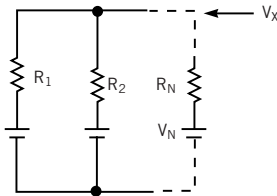
Assume an inverting comparator with an upper limit of 4V and a lower trip voltage of 1.333V. The voltage on the in-

verting input needs to reach 1.333V for the output to switch to V_{CC} . Then, for the output to return to zero, the input voltage needs to reach 4V.

Millman's Theorem states that the sum of the products of the voltages times their respective conductances divided by the sum of the conductances gives the common junction-point voltage V_x (Figure 1). Or,

$$V_x = \frac{\sum V_N G_N}{\sum G_N}$$

Figure 1



Millman's theorem states that the sum of the products of the voltages times their respective conductances divided by the sum of the conductances gives the common junction point voltage V_x .

where $G = 1/R$.

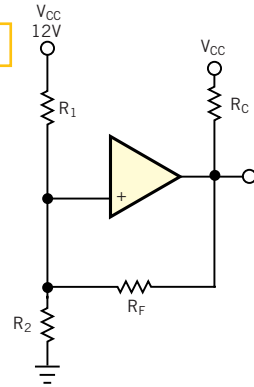
Using Millman's Theorem, with V_{CC} at the top of R_1 and R_F (Figure 2), set up the numerator with a Millman equation. Set up the denominator with another Millman equation when the output voltage is zero (with only one voltage source in the denominator). Assume that R_C is $\ll R_F$ and therefore negligible in the calculations. The resultant equation for the voltage ratio is:

$$\frac{V_{IN(HIGH)}}{V_{IN(LOW)}} = \frac{\sum V_N G_N}{\sum G_N} = \frac{12}{R_1} + \frac{12}{R_F}$$

$$= \frac{R_F + R_1}{R_F} = \text{VOLTAGE RATIO.}$$

This large fraction equals the voltage ratio 4/1.3333. First solve for R_F in terms of R_1 , and select R_1 in relation to R_F , such as $R_1 \approx 1\text{ M}\Omega$, and $R_F \approx 500\text{ k}\Omega$. Then solve for R_2 . The resistance ratio always equals the voltage ratio minus one. (DI #2372)

Figure 2



Using Millman's theorem, you can calculate that the voltage ratio of the trip points equals $(R_F + R_1)/R_F$.

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EDN selects 1998 Design Ideas grand-prize winners

EDN is pleased to announce the grand-prize winners for Design Ideas published in 1998. Lukasz Śliwczynski and Marcin Lipiński of the Institute of Electronics at the University of Mining and Metallurgy, Kraków, Poland, specialize in fiber-optic transmission for nontelecommunications applications and other optoelectronic circuits. The pair takes the honors for "Circuit uses simple LED for near-IR light," *EDN*, Sept 1, 1998, pg 92. The choice was difficult given the high quality of 1998's Design Ideas. *EDN* chose the winning Design Idea for its simplicity, cleverness, and usefulness. The circuit eliminates the need to configure a bulky and expensive mechanical fixture to generate light with precisely controlled power levels. The honors took the pair by surprise.

"We never suspected that, among so many interesting ideas, ours might be prized as the best one," says Lipiński. He says that he and co-designer Śliwczynski thought of the idea after participating in a project involving some optical reflectometers re-

quiring a precise and stable light source. "We have done lots of experiments with semiconductor lasers, but found that they are unsuitable for this purpose," says Lipiński. After these experiments, the pair decided to use the hybrid LED module that the winning Design Idea describes. The idea has already found use in a real-world application. A pro-ecological installation uses the reflectometer to measure the fumes from industrial chimneys. It has been in use for a long time and performs well, according to Lipiński. This Design Idea was one of six that Śliwczynski submitted and the only one Lipiński submitted last year.

In his spare time, the 30-year-old Śliwczynski, who is single, plays electric guitar and travels to historical sites. Lipiński, 52, is married with two children and likes classical music, skiing in the wintertime, and camping in the summertime. Each designer plans to use his half of the \$1500 cash prize for the upcoming summer holidays.

Every month readers pick one Design Idea from the issue as the winner. Congratulations to all the winners, and keep the innovative ideas coming.

Jan 1, 1998, "Fax saver cuts wear, tear, and power," Hugh Adams, Fort Walton Beach, FL.

Jan 15, 1998, "LED flasher and triac pulser work off ac line," Dennis Eichenberg, Parma Heights, OH.

Feb 2, 1998, "Vital-signs monitor consumes less than 50 μ A," Leonard Schupak, Discovision Associates, Irvine, CA.

Feb 16, 1998, "Antenna extension provides open-door policy," Richard Panosh, Vista, Bolingbrook, IL.

March 2, 1998, "Isolated driver forms solid-state circuit breaker," Bob Watson, Corley Manufacturing Co, Chattanooga, TN.

March 13, 1998, "Inexpensive relays form digital potentiometer," Robert Perrin, Z-World, Davis, CA.

March 26, 1998, "Alternating LED blinker uses four parts," Andy Meng, Cincinnati, OH.

April 9, 1998, "10-kHz VFC uses charge-pump variation," Stephen Woodward, University of North Carolina, Chapel Hill, NC.

April 23, 1998, "\$5 junk-box circuit determines phase sequence," Hugh Adams, Fort Walton Beach, FL.

May 7, 1998, "MCS-51 endows MicroLan-like protocol to UARTs," SK Shenoy, NPOL, Kochi, India.

May 21, 1998, "High-frequency AGC has digital control," Ron Mancini, Harris Semiconductor, Melbourne, FL.

June 4, 1998, "25-kV generator tests insulation," Lukasz Śliwczynski and Przemyslaw Krehlik, University of Mining and Metallurgy, Kraków, Poland.

June 18, 1998, "Use a printer port to record digital waveforms," Dean Shen, Dycam Inc, Chatsworth, CA.

July 2, 1998, "Circuit protects against ac-line disturbances," Basilio Simoes, ISA, Coimbra, Portugal.

July 16, 1998, "Step-up/step-down converter takes 2 to 16V inputs," Luciano Bordogna and Luca Vasalli, Maxim Integrated Products, Milan, Italy.

Aug 3, 1998, "Circuit translates TTY current loop to RS-232C," Jerzy Chrzaszcz, Warsaw University, Poland.

Aug 17, 1998, "Replace an external gate with a resistor," Stan D'Souza, Microchip Technology Inc, Chandler, AZ.

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