

Structured ASICs deserve serious attention at 90 nm

THE COST OF 90-NM—NOT TO MENTION 65-NM—SILICON IS OUTRAGEOUS. USERS SHOULD TAKE A LONG, HARD LOOK AT STRUCTURED ASICs WHEN CONSIDERING WHICH FABRIC TO USE FOR THEIR NEXT LOGIC DESIGN.

Four years after ASIC vendors introduced their first structured-ASIC devices in response to FPGA vendors eating up their market share, the structured-ASIC market has yet to become a popular choice for logic designs.

But analysts say that the structured-ASIC market is a viable business today and may exceed \$1 billion by 2008, as designers add up the cost of 90-nm ASIC design and run up against the hard limitations of FPGAs.

Analysts and structured-ASIC vendors put up good arguments about why you should at least consider structured fabric for your next IC-design project. But you should consider a number of variables—both technical and business—when evaluating FPGAs, structured ASICs, and cell-based ASICs.

Companies market structured ASICs as the midvolume, midprice missing link between fast-turnaround, reprogrammable but low-volume FPGAs and high-cost, high-volume, hard-to-design cell-based ASICs.

A structured device resembles a gate array on steroids. Like gate arrays, structured ASICs have a limited number of designable layers (usually one to six), a low tool and NRE cost, and a turnaround time ranging from days to months. As with gate arrays, silicon vendors have taken care of most of the nasty physical-design effects with prerouted and pre-tested layers. In most devices, they've also pre-designed the clock tree. But structured-ASIC devices offer much larger designable gate counts and much more on-chip memory than gate arrays.

A VIABLE MARKET?

The structured-ASIC market has not yet seen widespread adoption among users and has not yet become the \$300 million market many proponents had predicted. FPGA proponent Tom Hart, CEO of Quicklogic, goes so far as to say, "Structured ASIC is the last dying gasp of the ASIC business," and John East, president and CEO of Actel, says that structured ASIC "suffers from the same drawbacks that have caused ASICs to lose market share to programmable devices over the past two decades."

Many analysts, however, disagree with Hart's and East's assessments of the structured-ASIC market, saying that FPGAs, structured ASICs, and cell-based ASICs all have unique functions and their own place in the logic-device market.

"This is not about who is going to win," says Semico Research Corp's senior ASIC and SOC (system-on-chip) analyst Richard Wawrzyniak. "It is about what combinations of features and functions, power, time to market, and cost best suit your needs."

Although the structured-ASIC market posted 2004 revenue ranging from only \$86 million (iSuppli) to \$209 million (In-Stat), not \$300 million as previously expected, the market, say analysts, shows signs of picking up (Figure 1).

Research company IBS Inc predicts

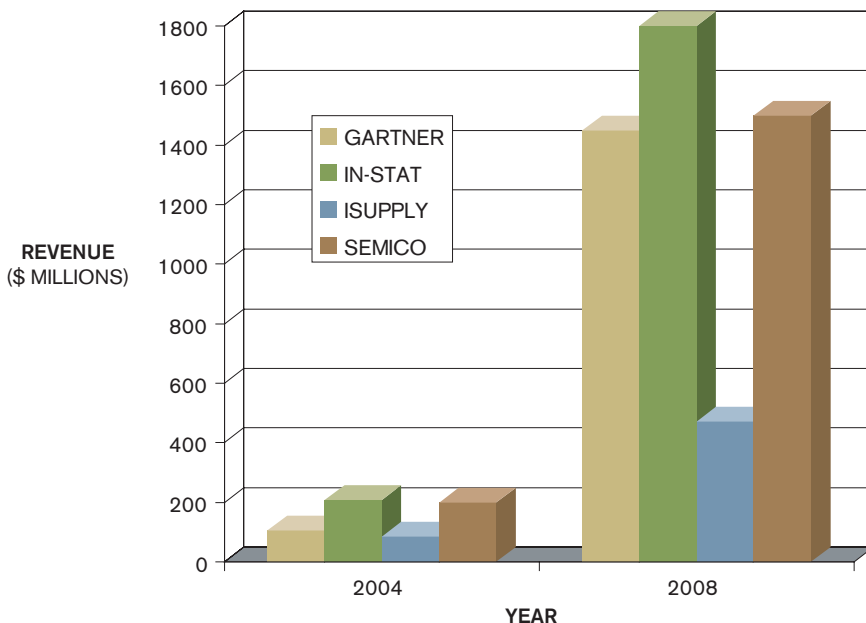


Figure 1 Semiconductor analysts say that the structured-ASIC market isn't going away.

AT A GLANCE

▣ The structured-ASIC market has yet to produce big revenue, but analysts say that it may be the best bet for complex and midvolume designs.

▣ The cost of 90-nm silicon and the hard limitations of FPGAs will boost the structured-ASIC market past the \$1 billion mark by 2008, analysts say.

▣ A 90-nm ASIC costs anywhere from \$30 million to \$50 million to produce.

▣ Structured ASICs have NREs of \$0 to \$250,000, low to no tool cost, and turnaround times of days to weeks, giving them lower engineering and overall costs than traditional ASICs.

▣ When it comes to volume, FPGAs are the right choice to 20,000 units, and structured ASICs are the right choice for 100,000 to 3 million units. Traditional ASICs still have the strongest play at greater than 3 million units.

that by 2007, one-third of all ASICs will employ structured-ASIC fabric. Bryan Lewis, research vice president and chief semiconductor analyst at Gartner, more or less concurs.

“By 2008, structured ASIC will be about a third of the designs out there, but the revenue is less than 10% of the overall ASIC market,” he says. “For a structured ASIC, the typical revenue per design is running around \$3 million or \$4 million, and in a traditional ASIC, it is running at \$5 million or \$6 million.”

Lewis believes that the structured-array market, which in 2004 was worth \$104 million, will become a \$1.45 billion market by 2008, with design starts moving from 181 in 2004 to 1230 by 2008. He believes Altera and LSI Logic are currently the structured-ASIC market leaders. He says most structured-ASIC vendors, with the exception of Altera, have been tightlipped when asked about revenue. He notes that Altera reported \$19 million in revenue from its HardCopy structured family in 2004. Altera was the only company to provide tapeout and customer data for **Table 1**.

Alain Bismuth, vice president of the HardCopy product group at Altera, says that the company's customer base for HardCopy has increased from 20 to 30 customers over the last year and that there were 12 design starts in 2003 and 20 in 2004. In 2005, the company has doubled capacity to accommodate growing demand for structured ASIC.

“We exited 2004 with one tapeout a week, and so as we entered 2005, we decided to double our capacity,” says Bismuth. “This means we can now accommodate 100 tapeouts per year. We did this to support growth across all market segments.”

Simone Shaghafi, ASIC-marketing manager at Fujitsu Microelectronics, says that Fujitsu customers are also showing increased interest in the company's structured-ASIC lineup.

“For the past six months, over 70% of the RFQs [requests for quotes] we have received are for structured ASICs,” says Shaghafi, noting as does Bismuth that the main reason for customer interest in structured fabric is the rising cost of ASIC and hard limitations of FPGA fabric.

“At 90 nm is when this industry will really kick in,” says Lewis.

AFFORDABLE DESIGN?

At 90 nm, an ASIC mask costs more than \$1 million, and, as the process matures, the industry expects that cost to drop to approximately \$750,000. That's still roughly twice the cost of a 0.13-micron mask when vendors introduced that process. When TSMC announced its 65-nm process earlier this year, its officials said that the normalized cost of a TSMC mask would cost approximately \$1.5 million. Meanwhile, IBM and Chartered Semiconductor say that the initial cost of a 65-nm mask will likely be well over \$2 million.

AT 90 NM, AN ASIC MASK COSTS MORE THAN \$1 MILLION, AND, AS THE PROCESS MATURES, THE INDUSTRY EXPECTS THAT COST TO DROP TO APPROXIMATELY \$750,000.

It's especially disconcerting considering that a given design group's next design will likely require more than one mask set and maybe a few mask sets simply because design complexity continues to increase at the 90-nm node.

Designs at 90 nm, say vendors, require more functional verification than 130-nm designs. They also require extra steps in physical design, such as optical proximity correction for all layers, resulting in higher engineering cost. The tools to handle these advanced process effects and verification also are becoming more expensive.

Thus, analysts estimate the total development cost for a 90-nm ASIC will run anywhere from \$30 million to \$50 million, with the bulk of that cost coming from engineers designing and verifying the functions of the design.

That lofty price, say analysts, will limit the number of designs targeting that node to high-volume applications, such as cell phones, game consoles, graphics ICs, and automotive products.

HARD LIMITATIONS OF FPGAs

FPGAs' instant reprogrammability and in-circuit verification have made them invaluable in any designer's toolbox. Over the last two decades, FPGA vendors have made leaps and bounds in reducing the volume cost of their devices. At the same time, they have increased gate counts and device performance and in turn annually taken over more of the ASIC business. Designers no longer use FPGAs just for ASIC prototyping. Each year, FPGA vendors offer more gates at prices that make devices reasonable for high-volume use.

Semico's Wawrzyniak says that FPGA has grown into a \$3 billion market, which is one-third smaller than the ASIC market, at \$9 billion, he estimates.

But although FPGAs have improved on all fronts, even the highest end FPGAs don't have the density, performance, and especially the midvolume and high-volume unit costs of ASICs, which are 10 times less expensive than high-end FPGAs at volume, analysts estimate.

FPGAs also have hard limitations and are unsuitable for use in wireless designs, especially cell phones, which require very low power, small die/package size, extremely large gate counts, and top performance.

FPGAs use more transistors than do structured or cell-based designs for functions other than logic, says Ronnie Vasishta, executive vice president of marketing at eASIC. “Transistors in FPGAs are used for buffering, look-up tables, and

switching, not just logic. That means that static-power leakage is immense,” says Vasishta. “FPGAs leak like sieves, and a function in FPGA consumes 400 times more power than an equivalent function in standard cell.”

“If you are pad-limited or need IP that is not available in FPGA, you might have to jump into a platform or cell-based ASIC regardless of volumes or complexity,” says Yousef Khalilollahi, director of RapidChip marketing at LSI Logic.

TABLE 1 STRUCTURED-ASIC ALTERNATIVES TO FPGAs AND CELL-BASED ASICs

Company	Structured-ASIC family	Designable layers	Total No. of layers	Designable gates (ASIC equivalent)	Process geometry and fab	Memory (bits)	Top speed (MHz)
Altera	HardCopy II	Two layers of metal, three vias	NA	3.6 million	TSMC 90 and 130 nm	8.8M	350
AMI Semiconductor	XPressArray XPA-1	Hybrid, five to seven	20 to 24	49,000 to 1.7 million	TSMC 0.18 micron through metal 2; metal 3 to 7 with AMIS 0.35 micron	38k to 1.4M DPRAM	200 system, 350 local
	XPA-HD	Hybrid, five to seven	20 to 24	64,000 to 2.7 million	TSMC 0.18 micron through metal 2; metal 3 to 7 with AMIS 0.25 micron	38k to 1.4M DPRAM	200 system, 350 local
	XPA-II	Hybrid, seven	25	511,000 to 4.9 million	TSMC 0.15 micron through metal 2, metal 3 to 7 with AMIS 0.25 micron	332k to 4.2M DPRAM (18-kbit blocks)	210 system, 500 local
ChipX	CX3000	Two	Three	20,000 to 200,000	Charter 350 nm	352k	100
	CX4000	Two	Five	20,000 to 550,000	UMC 250 nm	448k	125
	CX5000	Two	Six	25,000 to 1.1 million	UMC 180 nm	2.5M	200
	CX6000	Four	Eight	100,000 to 1.5 million	UMC 130 nm	3.5M	300
eASIC Corp	FlexASIC	One via layer, configured with one mask or by direct-write eBeam (zero masks)	Eight (eight metal/one poly)	3 million	STMicro, CMOS 130 nm	3M	250
Faraday Technology Corp	Netcomposer (NC-1) family (September 2005)	Four metal layers	One poly, eight metal, 42 layers	4 million raw gates, 2 million usable	0.13-micron UMC HS process	1M	Maximum CPU, 450; block, 300
	Peripheral Composer (PC-1) family (August 2005)	Three metal layers	One poly, six metal, 32 layers	1 million raw gates, 500,000 usable	0.18-micron UMC G2 process	0.5M	Maximum CPU, 190; block, 100
	PowerSaver Template (PST-1) family (December 2005)	Four metal layers	One poly, eight metal, 43 layers	4 million raw gates, 2 million usable	0.13-micron UMC HS process	1.5M	Maximum structured ASIC, 150
Fujitsu	AccelArray	Three to five metal and via layers	Six metal	4 million maximum	Fujitsu 0.11-micron technology, 0.08-micron physical gate length	4.5M	311
LSI Logic	RapidChip Platform ASIC	Four metal layers	NA	As many as 5.6 million usable ASIC gates	TSMC 110 nm and LSI Logic Gresham 110 nm	8M	More than 400, 20 levels of logic at 312
NEC Electronics	ISSP1	Two	Seven	1.7 million	150 nm NEC	3.6M	200
	ISSP1-HSI	Two	Seven	1.7 million	150 nm NEC	3.6M	200
	ISSP-90	Two	Seven	6.5 million	90 nm NEC	5.6M	333
	CMOS12M (in July)	Five	Five to six	2.4 million	150 nm NEC	2.7M	200

Steven Kawamoto, senior marketing manager at NEC Electronics America Inc, says that design constraints offering high performance and low power sometimes force users to go directly to ASIC fabric and can't be adequately prototyped,

even in FPGAs. "In these cases, structured ASIC allows users to prototype," says Kawamoto. "If you need low volume but the speed of an ASIC, you can move right away with structured ASICs."

FPGA vendors also offer volume

breaks. Xilinx, for example, offers its EasyPath option to allow its users to mass produce FPGAs for 30% less in volume, starting at 3000 units by locking down a large portion of the design and cutting out test costs. "We don't create a new sil-

Power (V)	Type of programming	Average NRE	Time from hand-off to silicon	Minimum unit volume	No. of structured-ASIC customers in 2004	No. of structured-ASIC customers as of May 5, 2005	Total structured-ASIC design starts in 2003	Total structured-ASIC design starts in 2004	Total structured-ASIC design starts in 2005
1.2	None	\$150,000	Eight to 10 weeks	1500	More than 20	More than 30	12	20	50
1.8	Metal mask	\$50,000 to \$100,000	12 to 14 weeks	5000 to 10,000	NA	NA	NA	NA	NA
1.8	Metal mask	\$50,000 to \$100,000	12 to 14 weeks	5000 to 10,000	NA	NA	NA	NA	NA
1.5	Metal mask	\$125,000 to \$225,000	12 to 14 weeks	5000 to 10,000	NA	NA	NA	NA	NA
5/3.3 (I/O)	Metal mask	Less than \$40,000	Five to six weeks	100	Claims 1600 designs since inception	NA	NA	NA	NA
2.5/3.3 (I/O)	Metal mask	Less than \$50,000	Four to six weeks	100		NA	NA	NA	NA
1.8/2.5/3.3 (I/O)	Metal mask	Less than \$100,000	Six to eight weeks	100		NA	NA	NA	NA
1.2/1.8/2.5/3.3 (I/O)	Metal mask	Less than \$225,000	Eight to 10 weeks	100		NA	NA	NA	NA
1.2	Bit stream for logic plus direct-write eBeam or single photolithographic mask for routing	\$0	Three weeks	No minimum	NA	NA	NA	NA	NA
1.2 (core), 3.3/5 (I/O)	Metal mask	\$250,000	35 to 40 days	2000	NA	NA	NA	NA	NA
1.8 (core), 3.3 (I/O)	Metal mask	\$144,000	25 to 30 days	2000	NA	NA	NA	NA	NA
1.2 (core), 3.3/5 (I/O)	Metal mask	\$200,000	35 to 40 days	2000	NA	NA	NA	NA	NA
1.2	Metal mask	\$150,000	Four to eight weeks, depending on design	1000	NA	NA	NA	NA	NA
1.5, 1.8	Metal mask	\$125,000	Eight to 10 weeks	1300	NA	NA	NA	NA	NA
1.5	Metal mask	\$60,000 to \$90,000	10 days	400	NA	NA	NA	NA	NA
1.5	Metal mask	\$80,000 to \$100,000	10 days	400	NA	NA	NA	NA	NA
1	Metal mask	\$150,000 to \$190,000	Four to six weeks	400	NA	NA	NA	NA	NA
1.5	Metal mask	\$65,000 to \$100,000	14 days	10,000	NA	NA	NA	NA	NA

icon product. We apply a new test methodology to the same product,” says Patrick Dorsey, director of EasyPath and Configuration Solutions Division at Xilinx. “It is exactly the same silicon and the same product.”

Because they are on the same silicon, the devices still have power and die-size limitations. Analysts say that until FPGAs vendors address those hard limitations, a market opportunity exists for structured devices.

WHY STRUCTURED?

“Structured ASIC is a product to solve a bunch of problems, and in this case, the problems are structural and not likely to go away,” says Wawrzyniak. “Structured ASIC will only go away if someone figures a way to cut design time in half, cut NRE in half, and market windows widen greatly.”

Wawrzyniak says that the structured-ASIC market was \$200 million last year and predicts that it will grow to \$1.5 billion by 2008.

“IF YOU ARE LOOKING TO DEVELOP A CHIP THAT IS HIGH-COMPLEXITY BUT LOW-VOLUME, FPGA IS THE WAY TO GO.”

Structured ASICs have a much lower NRE and volume requirement than traditional ASICs and a much faster turnaround time—anywhere from 10 days to 14 weeks (Table 1).

“The whole idea of platform ASIC is not just the savings in mask charges; three-fourths of the design is reused, and that can save you \$5 million to \$7 million in engineering effort,” says Lewis. “You save on mask, but the bigger savings is on engineering.”

Structured-ASIC customers typically need buy only one or two commercial-EDA tools—typically a synthesis tool from Synplicity, Magma, or Synopsys—spending \$25,000 to \$50,000. Some vendors follow the FPGA-vendor-tool mod-

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el and offer customers OEM versions of design software for free.

Jordan Selburn, ASIC and FPGA analyst with research firm iSuppli, says users are employing structured ASICs in a range of applications, so vendors are keeping busy creating slices, which are application-specific platform layers, to speed customers through tapeout and products to market.

“I don’t know the exact number of slices LSI Logic has, but they are probably averaging one new slice per design,” says Selburn, who predicts that the structured-ASIC market will reach \$471 million by 2008, after posting what he estimates was revenue of \$86 million in 2004.

GUIDELINES FOR CHOOSING

For high-complexity designs, analysts say, structured ASICs cost five to 10 times less in volume than equivalent-gate-count FPGAs.

Judging solely on volume, a consensus of semiconductor-industry analysts and vendors say that FPGA is likely the most viable fabric for high-complexity designs to 20,000 units, and structured ASIC is the most viable option from 100,000 to 3 million units. Above that number, traditional ASIC becomes more reasonable in volume.

“If you are looking to develop a chip that is high-complexity but low-volume, FPGA is the way to go,” says Jerry Worchel, principal analyst, ASIC/ASSP and intellectual-property service at market-research company In-Stat. “If you need 1000 and 20,000 and the cost is within your budget constraints for the system,

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then an FPGA is a good way to go. You sure don’t want to buy 100,000 FPGAs if they are \$5 apiece, hence the structured-ASIC market.”

“From 2000 units to around 250,000 units is where platform ASIC makes sense,” says LSI’s Khalilollahi. “Beyond that, cell-based ASIC makes more sense. As we move to finer process geometries, platform will make sense at higher volumes.”

At what gate count structured makes more sense than FPGA and ASIC depends largely on who you ask.

Altera’s Bismuth says that FPGA is the right option for low- to medium-density designs to 1 million gates, unless volumes are really high. Structured ASIC, he says, is ideal for designs of greater than a million gates. “For density above 5 million gates, there is nothing else available; you have to go to an ASIC,” says Bismuth.

ASIC vendors, of course, believe the gate-count inflection point at which designers should consider structured ASIC over FPGA is much lower.

“If you have a small design around 50,000 FPGA gates, FPGAs are a good choice, because FPGA vendors have really come down in pricing,” says Khalilollahi. “But when you really get to 250,000 to 500,000 ASIC gates, that’s when the platform-ASIC proposition becomes valid.”

Bismuth notes that security is another consideration. Structured devices, he contends, typically have better security and encryption features than do SRAM-based FPGAs. Of course, FPGA vendors, most notably Actel, have FPGAs with high-security features.

Manpower and skills are other considerations. Analysts point out that many design groups lack the employees or the experience to design a full-blown ASIC, but, they say, a designer with the skills to perform FPGA synthesis likely has enough knowledge to synthesize a structured device. **EDN**

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