

leading edge

What's hot
in the
design
community

Edited by
Fran Granville



Dog-eat-blog world

"Here he is working all night on something read by five second cousins and a dog, and I'm willing to pay him."

—Barbara Quint,
editor of online
magazine *Searcher*,
of a blogging-addicted
writer who misses
deadlines as a result,
in *The New York Times*,
May 24, 2004

Smallest computer fits portable designs

By Warren Webb

MEASURING JUST 1.25×2.3×0.26 in., the Triton-XXS from Strategic Test Corp is a complete PXA255 computer targeting low-power, portable, embedded designs. The XXS includes a



Laying claim to the world's smallest PXA255 CPU module, the Triton-XXS low-power single-board computer targets use in portable, embedded designs.

400-MHz PXA255 CPU, 64 Mbytes of low-power SD-RAM, 32 Mbytes of flash, a built-in LCD controller, a PCMCIA interface, and two 100-pin surface-mount connectors.

Other board features include four high-speed serial interfaces, SPI, I²S, and AC'97 audio. A unique "programmable-core-power" feature for battery-operated devices allows you to vary the operating voltage from 0.9 to 1.5V to save power. The Triton-XXS is available immediately for \$286 (1000). Strategic Test provides free technical support and software updates, along with an optional development kit that includes the Linux kernel 2.6 or Windows CE.NET operating systems.

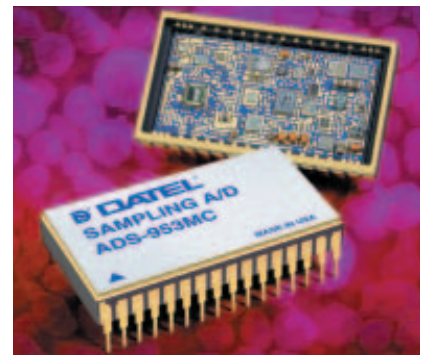
►Strategic Test Corp, 1-617-621-4010, www.strategic-test.com.

Watching high-speed ADCs? Don't blink

HOT ON THE HEELS OF *EDN's* most recent high-speed ADC survey, Datal has announced the ADS953, an 18-bit, 1M-sample/sec converter for high-end instrumentation, imaging, and communications systems (see "High-speed ADCs: preventing front-end collisions," *EDN*, May 13, 2004, pg 59). The device guarantees no-missing-codes performance over a -40 to +110°C operating range. The 953 accommodates a ±5V input range and features -80-dB THD (total harmonic distortion), -93-dB spurious-free dynamic range, and 91-dB SNR, all worst-case from 0 to 70°C at 50k samples/sec.

The 953's input span is ±5V; 15 pF or less shunts the input 500Ω impedance. The initial zero error is limited to ±15 mV with a maximum temperature coefficient of 0.2 mV/°C over the commercial range and 0.5 mV/°C over military temperatures. The ADS953 operates with ±15 and ±5V supplies and dissipates no more than 1.45W over temperature. Datal manufactures the 953 as a TDIP-32 hybrid priced at \$464 (100) and \$562 (100) for the commercial- and military-temperature ranges, respectively.—by Joshua Israelsohn

►Datal, 1-508-339-3000, www.datal.com.



The ADS953, an 18-bit, 1M-sample/sec converter, targets high-end instrumentation, imaging, and communications systems.

\$50 data-acquisition units connect to PCs via USB

DATAQ INSTRUMENTS has sold tens of thousands of its rock-bottom-priced, palm-sized (2.6×2.6×1.1-in.), eight-analog-input data-acquisition units. At the company's Web site, \$25 still gets you

the original RS-232C-connected DI-148R, which has a maximum acquisition rate of 2k samples/sec; six digital-I/O points in addition to the 610V-full-scale, 10-bit-resolution, single-ended analog inputs; and two eight-point screw-terminal blocks for the digital-I/O and analog-input points. However, with many new PCs having USB ports and no RS-232 port—unless you purchase an external USB-to-RS-232 adapter—Dataq officials thought it was time for a USB version. The otherwise-identical DI-148U costs \$50—a little more than the 148R, but the unit can acquire analog data at 28.8k samples/sec.

It is technically incorrect to refer to the DI-158 series as the DI-148's bigger sibling; the 158 case size is identical to that of the 148 series. However, the 12-bit-resolution 158-

series units offer programmable gain (×1, 2, 4, and 8 on one unit and ×1 to ×512 in 10 power-of-two steps on the two others) as well as a choice of USB or Ethernet interfaces. Dataq furnishes an ac adapter with the Ethernet units, whose maximum acquisition rate is 14k samples/sec; the 28.8k-sample/sec USB units receive their power from the



The USB-interfaced DI-148U provides eight 10-bit analog inputs and six digital-I/O points for just \$50.

bus. The DI-158 units, which incorporate channel-gain scan-list capabilities, sacrifice two digital-I/O points to add two digital-to-analog outputs. Prices range from \$99 to \$299.

The company's 5.43×4.12×1.5-in. DI-710 series, whose prices range from \$399 to \$799, provides more advanced capabilities, including 14-bit resolution, 16 user-configurable single-ended or eight differential analog inputs, and the ability to accept plug-in MMCs (multimedia cards) that store as much as 512 Mbytes. Some units can act as self-contained networked servers without a separate local host computer. Like the DI-158 series, the DI-710 units offer a choice of Ethernet or USB interfaces.

All units in all three series include the company's WinDaq software as well as an Active-X programming library. Units that can act as self-contained servers include additional software.

—by Dan Strassberg

►Dataq Instruments, 1-330-668-1444, www.dataq.com.

PICK A CARD, ANY CARD...AND READ IT

The proliferation of flash-media cards means that designing a reader for multiple formats can be a challenge. SMSC intends to change that situation with its USB2224 and USB2223 flash-media-card controllers, which interface between the USB host controller and the media card. The USB 2.0-compatible ICs handle all standard formats, including SmartMedia, xD Picture Card (USB2224 only), Memory Stick Pro, Memory Stick, High Speed Memory Stick, Secure Digital, Multi-MediaCard, NAND flash, Compact Flash I and II, and CF-form-factor ATA hard drives.

You can customize the ICs via more than 50 programmable settings, and a mask-programmed option is also available. The ICs perform 1-bit error correction in hardware to enhance efficiency. SMSC certifies the bus-powered devices, available in 128-pin TQFPs, for compliance with relevant standards. The devices allow a system to boot from flash media that support the bootable-BIOS function. Prices begin at \$4.45 (1000); the EVB-2224 development board is available for \$500.

—by Bill Schweber

►SMSC, 1-631-435-6000, www.smssc.com.

DILBERT By Scott Adams



►More than 57 million US citizens have received e-mails in the form of "phishing"—scams using phony e-mail messages and fraudulent Web sites—and phishing has accounted for \$1.2 billion annually in credit-card scams, according to a report from Gartner.

Graphics advancements span PCs to cell phones

NVIDIA'S TRAVAILS OF THE PAST two years are a reminder of the lesson of Aesop's classic fable *The Tortoise and the Hare*. Nvidia attempted to outleap its primary competitor, ATI Technologies (www.ati.com), to 0.13-micron technology with the GeForce FX 5800. But the initial revision of the process and, therefore, the chip based on it was excessively power-hungry. Nvidia's foundry

partner, TSMC (www.tsmc.com), also experienced production delays, causing Nvidia to miss the critical 2002 holiday-shopping season. ATI, in contrast, targeted the more mature 0.15-micron process for its Radeon 9700 graphics flagship, which smoothly ramped into high-volume production. Because ATI had the market to itself for many months, any potential lithography-driven cost disadvantage versus Nvidia went unrealized. And, again due to ATI's market dominance at the time, Microsoft (www.microsoft.com) settled on the Radeon 9700's 24-bit, floating-point shader architecture for initial revisions of the DirectX Version 9 API, leaving Nvidia's 32-bit approach in the 5xxx series at a performance disadvantage with DirectX Version 9-based applications.

Fortunately, Nvidia, unlike many other semiconductor companies, had sufficient money in the bank to help it ride out the rough times. It was also able to convince sufficient numbers of game de-

velopers to support 16-bit, floating-point partial precision, which Nvidia could speedily handle in hardware, in their DirectX 9 programs. With its latest graphics accelerator, Nvidia asserts that its past woes are behind it, due in part to its healthy relationship with a second 0.13-micron foundry partner, IBM (www.ibm.com). Nvidia squeezes 222 million transistors, some used to construct 16 parallel pixel pipelines, each with a matching texture unit, into the GeForce 6800. (The GeForce FX 5800, in contrast, contained four pixel pipelines, each with two corresponding texture units.) The GeForce 6800 also includes six vertex units, each of which can simultaneously process one vector and one scalar operation. It supports vertex fetches and branches and, therefore, displacement mapping, along with vertex instancing for high-efficiency model batching.

Nvidia hasn't backed down from its support for 32-bit, floating-point shader instructions, and the upcoming Di-

rectX Version 9.0c finally supports them at full precision. Although the GeForce 6800 significantly raises the industry bar on graphics performance, its video capabilities are also equally impressive. Nvidia moves away from the hard-wired MPEG-2 decoding pipeline in past chips to a more flexible video-processor approach. This approach is currently capable of hardware-accelerating MPEG-2 decoding and encoding, along with performance-boosting Windows Media Video 9 decoding at high resolutions and implementing advanced deinterlacing techniques. Support for WMV9 encoding, along with other video codecs, is ongoing.

The GeForce 6800 does have the potential for memory-bus bottlenecks. To use a historical analogy, the GeForce FX 5800's 128-bit external frame-buffer bus hampered its performance; the 256-bit interface in the follow-on GeForce FX 5900 relieved this restriction. Similarly, a 1.1-Gbps-per-pin, 256-bit DDR-3 SDRAM bus may still be insufficient to keep up with the GeForce 6800's 16-pipeline pace. Time will tell; \$499 Ultra boards running at a 400-MHz core frequency and with 256-Mbyte frame buffers are due on store shelves this month, along with Nvidia's first iteration of its Release 60 drivers. A less-than-\$300, non-Ultra variant of the GeForce 6800 with only 12 functional pixel pipelines and 128 Mbytes of DDR-1 memory appeared in May; the device reportedly runs at 325-MHz

core and 375-MHz memory speeds, although Nvidia does not officially confirm the specifications.

Although PCs may provide most of Nvidia's near-term revenues, the company also remains focused on cell-phone and PDA opportunities that last year's acquisition of MediaQ enabled it to pursue. Nvidia has, at least for the moment, shelved MediaQ's ARM-core-inclusive chips but is continuing the development of multimedia co-processors. The latest products include the GeForce 3000, targeting \$149 cell phones, and the higher end GeForce 4000 for fuller featured, \$199 phones. GeForce 3000 embeds 320 kbytes of SRAM, interfaces to 2 million-pixel camera modules, hardware-accelerates 2- and 3-D-graphics functions, and decodes CIF-resolution MPEG-4 Simple Profile and H.263 video streams at 30 frames/sec. GeForce 4000 doubles the amount of embedded memory over its lower end sibling and adds CIF-resolution, 30-frame/sec video-encoding capabilities, along with 3 million-pixel still-camera support. Nvidia has its work cut out for it; the market for handheld multimedia accelerators is quickly becoming crowded. Intel's (www.intel.com) 2700G, previously code-named Marathon, is a formidable foe, especially when the company bundles it with the latest generation PXA270 XScale processors.—by Brian Dipert
▶Nvidia, 1-408-486-2000, www.nvidia.com.

▶Sony was the third-largest handheld-system maker in 2003, shipping 1.4 million Clies into a worldwide market of about 10.7 million units, according to IDC. The Japanese market accounted for only 484,000 Clie shipments in 2003.

Behavioral-synthesis product uses SystemC models

SYSTEM DESIGNERS, especially those dealing with communication systems, use Matlab and Simulink or SystemC to specify algorithms to implement in hardware. However, the SystemC approach entails reimplementing the design in Verilog or VHDL to use logic synthesis for circuit implementation. Some EDA vendors have tried to introduce behavioral-synthesis tools that produce RTL (register-transfer-level) representations from algorithmic descriptions, but the results were not optimal, and designers did not adopt them. The problem with those tools is that they focused too much on circuit behavior instead of on algorithms. They also tried to extract the synthesis constraints from the model

source code, thus complicating both the model and the tool.

The SystemC hardware-description language uses C++ programming language and extends it to allow description of hardware primitives with the development of new classes. The introduction of SystemC gives EDA vendors a new opportunity to more easily translate algorithms expressed in software-programming language into RTL representations. Some tools are available to translate SystemC descriptions into Verilog or VHDL and thus allow direct synthesis without design recoding.

One such tool, Forte Design Systems' Cynthesizer, produces an RTL netlist directly from SystemC descriptions.

Although Forte calls the new product a behavioral-synthesis tool, the term "algorithm synthesis" more accurately describes the product. Using untimed SystemC models, the product builds a fully timed RTL-hardware implementation based on an external set of constraints. Designers can make trade-offs in area or performance without modifying the model, thus increasing the degree of reuse the model will provide.

Cynthesizer outputs standard RTL for a number of popular synthesis and simulation tools. The product includes automation of tasks such as operation scheduling, cycle timing, control and datapath blocks, resource allocation, and RTL generation. Cynthesizer is available on

both Linux and Solaris operating systems. Prices start at \$250,000 per year for a time-based license.

—by Gabe Moretti

► **Forte Design Systems**,
1-408-487-9340, www.forteds.com.

GEAR MOTOR IS SMALL, DOES IT ALL

Software or ICs cannot solve every design problem; you sometimes need a motor to move something, such as paper in a printer feed. One such device, the LB16-120-BB miniature brushless-dc gear motor from Nidec Copal USA, includes an integral speed control and 120-to-1 spur gear train, delivering 3.5 oz-in. of torque at 100 rpm. Load range



Get those small loads moving precisely, with the LB16-120-BB gear motor with speed control and 120-to-1 gear train.

is 0 to 6.9 oz-in. for the nominal 12V unit, and peak torque is 50 oz-in. at 0.8A, useful for fast-start and acceleration modes.

The unit weighs less than 1 oz and measures 1.3 in. long with a 0.63-in. outside diameter. Noise is just 45 dBA at 1 ft. The gear motor is available for \$25 (small quantities).

—by Bill Schweber

► **Nidec Copal USA Corp**,
1-310-782-6102, www.copal-usa.com.

Enhanced WiFi chips integrate USB, enable new applications

THE NEW Atheros AR5005UG and AR5005UX chip sets integrate a USB 2.0 interface for high-performance WLAN (wireless-LAN) applications beyond desktop applications, such as digital-video recorders, high-quality videoconferencing cameras, high-resolution scanners, and high-density external-storage devices.

The AR5005UG supports 802.11b/g, and the AR5005UX supports 802.11a/b/g, and they effectively wirelessly enable any device with a USB port. Both chip sets offer Atheros' Super G and Super AG technology, which use adaptive-bandwidth techniques to increase throughput to more than 60 Mbps on demand based on channel availability. The chip sets also offer the WME (wireless-media extensions) and quality-of-service capabilities that the IEEE 802.11e draft standard defines to facilitate the reliable wireless transfer of real-time voice, video, and data. Atheros' XR (extended-range) operation mode enables connections at greater distances from the access point at which signals are otherwise too weak to connect. Standard features without any performance reduction include WPA (WiFi Protected Access), WPA2, 802.11i Enhanced Security using AES (Advanced Encryption Standard), and CCS (Cisco-compatible extensions).

Currently available for sampling, the AR5005UX chip set sells for \$18 (10,000), and the AR5005UG chip set sells for \$16 (10,000). Reference modules for the chip sets measure 2.57×0.96 in. Atheros also announced that it has begun shipping versions of its line of WLAN chip sets that use a tin alloy as an alternative to lead solder, thus helping engineers meet international environmental guidelines.—by Nicholas Cravotta

► **Atheros Communications Inc**, 1-408-773-5200, www.atheros.com.

► **It costs \$10 million to \$20 million to produce a top-drawer computer game. The process usually takes 18 months to two years and requires about 100 workers.—The Boston Globe, May 31, 2004**

8-GHz RF-signal/spectrum analyzer offers open Windows XP interface, streams data to Matlab

FOLLOWING THE LEAD of digital-oscilloscope manufacturers, RF-instrument makers are introducing products that contain PC hardware. Many of the specifications of one such unit, Anritsu's Signature RF-signal analyzer, compete with those of high-quality swept-frequency spectrum analyzers. The product provides an open Windows XP operating environment and streams data directly from its measurement hardware to an analysis program that runs on the PC within the analyzer. Usually, the device works with The MathWorks' (www.mathworks.com) Matlab, but it can also work with the company's Simulink. This architecture thus enables data to flow in real time to customizable, top-tier math software, which displays complex calculated

results as quickly as the instrument acquires the underlying data.

These capabilities are particularly useful in applications such as the analysis of signal impairments caused by reflections from cars, airplanes, and other moving objects. When you use the same software with more conventional instrumentation, you can't even begin the analysis until you have acquired a complete data set and exported the file to a separate PC. With the built-in PC and high-speed links to the analysis software, the correlation with the external events is immediate and obvious; in the more conventional setup, you must not only wait to see the results, but also try to figure out what caused them.

The instrument's \$49,500 base price includes a DVD/

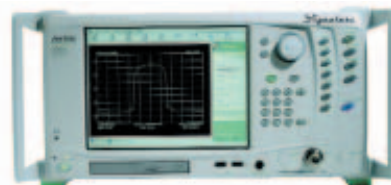
CD-R/W combination drive. Increasing the IF bandwidth to 30 MHz adds \$27,000. Without a separate computer or postprocessing, an \$8000 option allows measurements of EVM (error-vector magnitude), carrier leakage, and IQ (in-phase/quadrature) imbalance in signals that carry QAM (quadrature-amplitude modulation) and PSK (phase-shift keying). Matlab connectivity adds \$1000. You must separately purchase Matlab or Simulink from The MathWorks, however.

Anritsu says that, compared with similarly priced instruments, Signature offers superior sensitivity, intermodulation distortion, and dynamic range. Third-order intercept is 23 dBm, displayed average-noise level is less than -147 dBm, and typical amplitude

error is less than 0.65 dB over the entire frequency range.

—by Dan Strassberg

► **Anritsu Co**, 1-800-267-4878, www.us.anritsu.com.



The modular Signature RF-signal analyzer performs signal and spectrum analysis on bandwidths as great as 30 MHz in the range of 100 Hz to 8 GHz. The instrument incorporates a PC that implements an open Windows XP-based architecture that streams data in real time into Matlab software, which outputs and graphs the results of user-defined calculations as quickly as the instrument gathers the raw data.

EDA tool links to Simulink

ACCELCHIP (www.accelchip.com) and Catalytic Inc (www.catalyticinc.com) were the first two EDA companies to use The MathWorks' Matlab and Simulink models and designs as input to their products. Mentor Graphics (www.mentor.com) followed by providing a link from the Modelsim simulator to Matlab and Simulink, winning both companies the *EDN* Innovation award. Now, Synplicity has introduced a DSP-synthesis product that allows engineers to design the DSP and simulate it in Simulink and then convert the design to RTL and synthesize and optimize it for FPGA implementation.

When designing a circuit using a DSP device, some engineers prefer to use a standard device or core and develop the software that tailors the device functions to their applications, whereas other designers prefer to develop their own application-specific DSP. The first group usually works in C or C++ and is likely to have migrated to a SystemC development environment, and the second group uses Matlab and Simulink to design the device but then

manually reimplements the design in Verilog or VHDL.

Synplicity DSP joins the tools from AccelChip and Catalytic in providing a computer-aided translation from Simulink to an HDL (hardware-description language). Synplicity DSP optimizes the system-level design before HDL generation by using algorithms such as system-level retiming and automatic multichannel generation. The tool also uses a folding algorithm that allows users to trade off between performance and area. The Synplicity DSP software includes a set of functional blocks common to DSP design, such as FIR and IIR filtering, transforms, math functions, CORDIC (coordinate-rotation digital computer), signal operations, memories, and control logic. Although you may recognize Synplicity's FPGA synthesis, you can also use the product when targeting structured-ASIC or cell-based-ASIC devices. The product sells for \$39,000 for a perpetual license.—by Gabe Moretti

► **Synplicity**, 1-408-215-6000, www.synplicity.com.

► **The MathWorks**, 1-508-647-7000, www.mathworks.com.

► **Total voice-over-wireless-LAN-handset shipments totaled fewer than 60,000 units in 2003, according to InStat/MDR.**

Core stresses performance and power

TENSILICA'S XTENSA LX processor core drives down power consumption and increases computational and throughput performance. The Xtensa LX core incorporates fine-grained clock gating for every functional element, including user-defined extensions.

This level of clock gating helps reduce the core's power dissipation by 25% over the base Xtensa V core configuration.

The Xtensa LX core is the first implementation of the FLIX (flexible-length-instruction-extensions) architecture that supports modeless intermixing of 16-, 24-, 32-, or 64-bit instructions and better balances the performance and code-versus-size trade-offs when using a fixed-sized-instruction-length architecture. The FLIX architecture adds approximately 2000 gates of control logic to the core and supports

multiple, concurrent, independent, and compound operations per instruction cycle, and it is fully compatible with the 16- and 24-bit Xtensa instruction-set architecture.

The Xtensa LX implements LX-port and -queue interfaces and supports an optional second load/store unit to potentially increase the I/O throughput by several orders of magnitude. Port connections can be arbitrarily as wide as 1024×1024 bits, and they can directly connect two Xtensa LX cores or an Xtensa LX core to external RTL. The queue interfaces logically operate as traditional

processor registers, but the data is available without requiring a load or store before or after a computation. This approach allows queues to sustain data rates as high as one transfer per clock cycle. User-defined instruction extensions can perform multiple queue operations per cycle, including combining inputs from two input queues with local data and sending the computed values to two output queues.

You can configure the traditional five-stage pipeline with two additional pipeline stages to support memory access for instruction fetch and data load or store. This approach allows you to select the pipeline length based on the speed differences between high-clock frequencies coupled with large local memories, on the one hand, and slower, low-power memories, on the other. Each Xtensa LX processor configuration you

create includes custom software-development tools, an instruction-set simulator, a bus-functional model, and EDA scripts.

The Xtensa LX processor will be available early this summer. You can target each processor instance to any silicon-foundry technology, and licensing is on a per-processor basis plus royalties based on the volume of processors manufactured. Licensing fees for a single processor configuration start at \$550,000 for the Xtensa LX processor, and that fee includes the Vectra LX DSP engine. The Xtensa software-developer tool kit, which includes the Xtensa Explorer development environment, Xtensa C/C++ compiler, Xtensa instruction-set simulator, and Tensilica-instruction-set compiler, is priced separately.—by Robert Cravotta
►Tensilica, 1-408-986-8000, www.tensilica.com.

240A controller drives robotic vehicles

ROBOTEQ'S RECENTLY INTRODUCED dual-channel dc-motor controller directly drives as much as 120A on each channel at as much as 40V. The AX2850 targets designers of mobile robotic vehicles, including automatic guided vehicles, underwater remote-operated vehicles, mobile robots for exploration, hazardous-materials handling, and military-surveillance applications. The controller accepts commands from either standard remote-controlled radio for simple robot applications or a serial-port interface.

You can operate the controller's two channels independently or combine them to set the direction and rotation of a vehicle



Roboteq's AX2850 dc-motor controller delivers 120A per channel at as much as 40V to propel robotic-vehicle applications.

by coordinating the motion on each side. The AX2850 includes inputs for two quadrature encoders and four limit switches along with thermal protection, programmable acceleration, an input-command watchdog timer, and nonvolatile storage of configuration parameters.

The controller comes in an extruded aluminum case that also serves as a heat sink for its output-power stage. The AX2850 is available now for \$620 (one), complete with cable and PC-based configuration software.—by Warren Webb
►Roboteq Inc, 1-602-617-3931, www.roboteq.com.

►In the first quarter of this year, market share for Sony's Palm OS dropped more than 20%, according to Gartner, and Palm and Windows CE each accounted for 40% of the market.