

Figure 1 An analog SMPS control loop compares a scaled sample of the output voltage with a fixed reference and servos the PWM timing to force the two quantities to match.

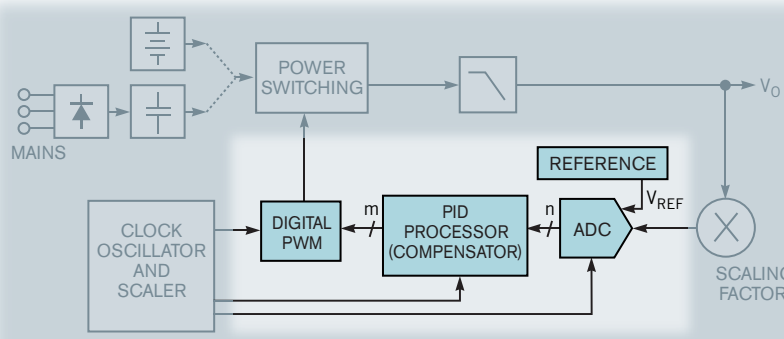


Figure 2 A digital SMPS control loop replaces the error amplifier with an ADC. The digital PWM requires a high-speed clock to provide the necessary edge-timing resolution.

BY JOSHUA ISRAELSOHN • TECHNICAL EDITOR

A BIT-O'-POWER: digitally controlled power conversion

IRONICALLY, PERHAPS, THE LAST SUBSYSTEM TO UNDERGO A SUBSTANTIVE SHIFT FROM AN ANALOG- TO A DIGITAL-CONTROL ARCHITECTURE IS THE MOST UNIVERSAL: THE POWER SUPPLY. BEWARE THE HYPE, HOWEVER. DIGITAL POWER CONTROL MAY BRING PERFORMANCE BENEFITS TO SOME APPLICATIONS, BUT UNTIL YOU BECOME FAMILIAR WITH THE INNER MACHINATIONS, THEIR SOPHISTICATION WILL EXACT A PRICE IN APPLICATION-DEVELOPMENT TIME.

Within reasonable limits of voltage and current ranges, disparate applications often put remarkably similar demands on power-management subsystems. This initially counterintuitive observation derives from the facts that many applications draw on common core technologies, exploit similar functional partitioning schemes, and operate dominantly on only a few different energy sources. Independently of what you design, declining operating voltages for major subsystems have marked the evolutionary track of many of the technologies you use. The supply tolerances that these technologies impose upon power subsystems have been in decline, too, in rough proportion to the supply voltages. Simultaneously, standing currents have been on the rise, and, disproportionately, dynamic currents have as well.

IN THE LOOP

The typical SMPS (switch-mode-power-supply) control loop modulates the timing of its power switches depending on the subsystem's output voltage (**Figure 1**). Working clockwise from the output, a scaling network samples the output voltage, multiplying it by $V_{O(\text{ideal})}/V_{\text{REF}}$. The term "error amplifier" is something of a misnomer. The device compares the scaling network's output with the reference voltage and produces a drive signal for the PWM sufficient to force the two input voltages to match. (Some literature describes the error amplifier as developing an output signal proportional to the difference between its two input signals, which is not the case as long as the loop is operating within its linear range.) A compensation network scales the amplifier's dc and low-frequency gain appropriately to the PWM's sensitivity and also provides a local high-frequency feedback path to ensure adequate phase margin for loop stability. This basic structure applies to both isolated and nonisolated supplies. You can provide isolation (not shown) either at the power entry or within the power-switching block.

Beyond the basic issues of voltage regulation, this architecture accommodates

AT A GLANCE

Recent arrivals of digital power controllers mark the beginning of what many believe is an important new trend in power control. Expect several competing parts to emerge over the coming quarters.

Digital power controllers allow you to exploit DSP-based filtering methods and build a range of supplies from a common core set of parts with model differentiation managed in software.

DPWM (digital-PWM) edge placement requires extremely high-speed clocks, which on-chip PLLs generally provide. Though the fastest signals stay on chip, use good high-frequency-layout practices to maintain switching-edge fidelity.

a variety of common ancillary functions with little additional complexity. For example, one additional resistor between the reference's output and the error amplifier's noninverting input provides a tracking option, which allows a regulator to follow another supply rail or voltage source. Here, an external voltage source can take control of the regulator's output target as long as it can adequately source (or sink as necessary) the reference current: $|V_{\text{TRACK}} - V_{\text{REF}}| \div R_{\text{R}}$. Few functions are implemented so simply, but the architecture accommodates such common features as overvoltage protection, undervoltage protection, overcurrent protection, and current reporting with moderate additional complexity and with little impact on the regulator's loop performance.

Outside the context of a switching regulator, servo circuits similar to this one date back to the days of vacuum tubes and are among the best studied, characterized, and documented control topologies in the literature (Reference 1). Considering the levels of performance that modern implementations provide, this loop is a remarkably simple and efficient structure, and, until recently, not easy to replace with a digital equivalent. Indeed, little more than a year ago, Astec Power Vice President Geof Potter stated, "Peripheral functions have long been within the scope of digital-control methods because

[the] necessary speed and complexity are not great. On the other hand, digital control of an active feedback loop, including a pulse-modulation process ... has been an elusive prize due to size, cost, and power consumption of components needed for practical operation. To successfully compete with a low-cost analog-control system, a digital equivalent requires data resolution and latency numbers that have been available only in large, expensive DSP and ADC products. To compound the difficulty, there are few, if any, integrated devices on the market ... that contain all the necessary functions to constitute a reasonable [digital] power 'controller'" (Reference 2).

BITS OF EMPOWERMENT

The motivation for such devices is multifold: Supplies for product variants within a family can use identical power-management circuits with model-specific tuning and optimization coded in software or by operational coefficients. Onboard self-test programs can reduce, enhance, or eliminate production testing of power-management functions, depending on your organization's design and test-method policies. A digital power-management section can automatically compensate or replace components subject to parametric variation over population, time, or temperature. Product and accessory identification and recognition schemes can fit into a digital-power-management design with little additional hardware and provide enhanced safety, product-tracking, and diagnostic information.

The digitally controlled loop replaces the error amplifier and its compensation network with an ADC and a control-law processor; the processor often implements a PI (proportional-integral) or PID (proportional-integral-derivative) compensator (Figure 2). The processor can access stored coefficients that determine the loop dynamics and can modify those coefficients to optimize operation during various normal operating modes, transient events, and faults. The processor's output drives the input to a DPWM (digital PWM), which in turn determines the switching-edge positions by calculating and timing as opposed to exploiting the analog loop's threshold-detection method.

The macroscopic similarities between the analog- and the digital-control-loop topologies mask the complexity of such a replacement. For example, both analog- and digital-control loops must compensate for the phase lags that the forward path imposes between the power-switch inputs and the filter output. The digital implementation must also contend with the additional phase lag due to analog-to-digital-conversion delays and computational latencies through the control-law processor.

In addition to operating as a discrete time circuit, the digital-control loop is a quantizer, whereas the analog-control loop operates in continuous time and amplitude. These distinctions impose structural requirements and performance limitations on the digital loop. These constraints have until recently made high loop bandwidths and tight output tolerances difficult to attain on a large mixed-signal IC. For example, the ADC determines the resolution of the output-voltage setting—the first line item on your output-voltage-error budget. You can calculate your minimum resolution from your nominal output voltage, V_{O} , and the setting resolution, ΔV_{O} :

$$\text{RESOLUTION} = \log_2 \frac{V_{\text{O}}}{\Delta V_{\text{O}}} = \frac{\ln \frac{V_{\text{O}}}{\Delta V_{\text{O}}}}{\ln(2)} \text{ (BITS)}.$$

To prevent limit-cycle oscillations in the output, quantizers that follow the ADC, including the DPWM, must exhibit a greater resolution than the ADC (Figure 3). This requirement ensures that a stable output value will exist for each possible ADC quantity. Referring to Figure 2,

$$m - n \geq 1.$$

The DPWM essentially translates bits of amplitude into bits of time. The power section's switching rate and the converter's amplitude resolution set the DPWM's minimum timing resolution: The DPWM must fit 2^m bits within the power section's switching interval. For example, in a controller that follows an 8-bit DAC with a 9-bit DPWM controlling a power section with a 1-MHz switching rate, the DPWM timing resolution is

$$\Delta t_{\text{DPWM}} = \frac{1}{f_{\text{SW}} 2^{\text{RES}_{\text{DPWM}}}} = \frac{1}{1 \text{ MHz} \times 2^9} = 1.953 \text{ nSEC.}$$

The reciprocal of the DPWM timing resolution gives the DPWM clock rate, which for this modest example is

$$f_{\text{CLK}} = \frac{1}{\Delta t_{\text{DPWM}}} = 512 \text{ MHz.}$$

As the voltage-setting resolution increases, the DPWM clock does likewise: one octave per bit. Because some emission is likely at both the system and the DPWM, consider the radiated-noise spectrum of a power supply that uses a digitally controlled loop in the context of your application's signal band before committing to the power-subsystem design. Also, be sure to observe good high-frequency-layout practices, particularly in the regions of the switch-drive and clock signals. Conduction of RF from the regulated dc output, V_o , is unlikely due to the output filter, but radiated RF emissions are still a layout concern (Reference 3).

POWER IN NUMBERS

The theoretical and technological-development work behind digital power controllers has been ongoing for some years, but this spring brought the announcement of ICs that implement the architecture from Texas Instruments and Silicon Laboratories. The Texas Instruments approach is a two-chip set with several options to accommodate a variety of SMPS topologies (Figure 4). ICs from the UCD9k and UCD7k families combine with your power-switching and filter sections to form a complete power subsystem.

The UCD7100 and 7201 single- and dual-channel, low-side MOSFET gate drivers feature microcontroller- and DSP-compatible inputs and can operate at switching rates as fast as 2 MHz. The drivers can typically source or sink 4A and feature maximum rise and fall times of 20 and 15 nsec, respectively, when driving 2.2-nF loads. The maximum input-to-output propagation delay is 35 nsec. Both drivers provide cycle-by-cycle current limiting, programmable limit thresholds, and logic-level limit-status flag outputs. The ICs can operate supplies

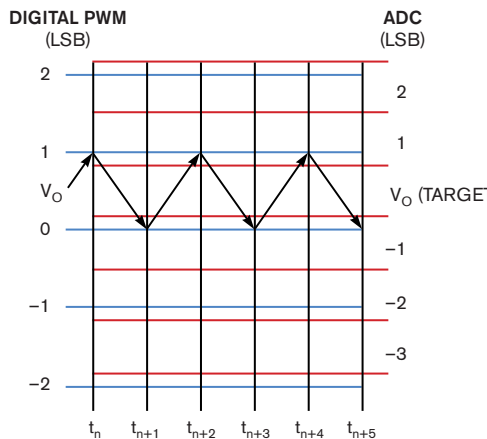


Figure 3 If the DPWM's resolution is coarser than that of the ADC that precedes it, limit-cycle oscillations can result.

in the range of 4.5 to 15V and include an on-chip 3.3V regulator rated for 10 mA, which you can use to power external circuits, such as a low-power microcontroller or ASIC. The 99-cent, single-channel and \$1.20, dual-channel drivers are available in QFN-14 and QFN-16 packages, respectively. Both parts are also available in HTSSOP-14 packages and are rated for operation at -40 to $+105^\circ\text{C}$.

TI also currently offers four other drivers in the UCD7k family. Various members include a synchronous-buck driver with current sensing, and single- and dual-channel, low-side drivers with 110V start-up capability. The dual-channel ICs are avail-

able with either independent or common current sensing. Members of the UCD7k-family drivers mate with a variety of processors, including the UCD9501 and its kin. The 9501, the first of the UCD9k family, comprises a 100-MHz, 32-bit Harvard DSP core; a clock- and timing-control block; a 12-bit, 6.25M-sample/sec ADC; extensive digital I/O, including PWM outputs; and memory.

The ADC features a 16-channel multiplexer and a sample-and-hold amplifier and operates over a 3V unipolar range. You can program the ADC to synchronize with the PWM outputs or initiate a conversion by either software command or hardware interrupt. A built-in sequencer can take as many as 16 samples with one command. You can program the

sequencer to take each sample from any of the 16 input channels. The converter's INL (integral nonlinearity) and DNL (differential nonlinearity) are typically 1.5 and 1 LSBs, respectively, at 6.25M samples/sec; the manufacturer provides no limit specs. Similarly, ac-converter specifications are available only as typical values: 76-dB SFDR (spurious-free dynamic range), 67-dB SNR, and 10.6-bit ENOB (effective number of bits), all at 100 kHz, suggest that the converter is largely noise-limited but at sufficiently low values for power-management applications. When the device is operating with a 100-MHz system clock, on-chip timers can set the

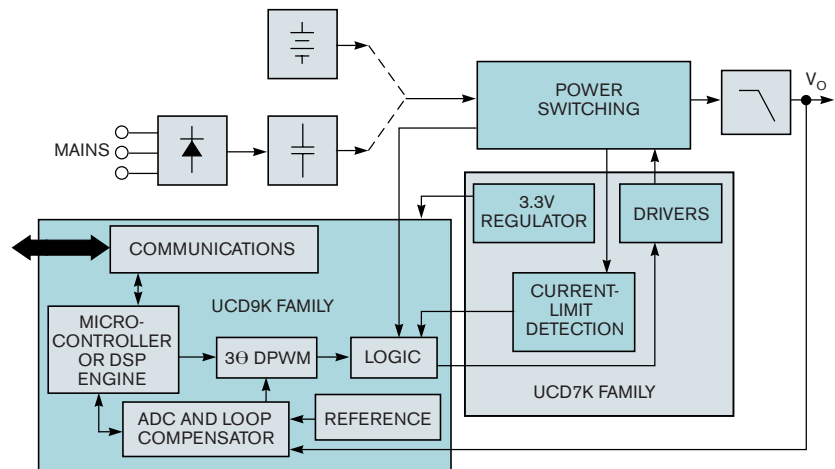


Figure 4 Texas Instruments' UCD9k and UCD7k ICs combine to form a digital power controller.

output edge positions of the three high-resolution PWM channels to a nominal granularity of 150 psec. At a 1-MHz power-switching rate, errors due to the PWM's finite-edge-placement resolution fall below the converter's noise floor.

TI offers the \$5.79 (1000) digital power controller in an LQFP-100 package with three temperature-range options extending to 125°C. The IC operates on 3.3 and 1.8V supplies and typically dissipates $\frac{1}{2}W$. Support tools include a \$495 eZdsp starter kit, a C/C++ compiler/assembler/linker, TI's Code Composer Studio IDE, evaluation modules, JTAG controllers, and TI's DSP/BIOS.

Silicon Labs takes a dual-processor approach that separates all of the communication and housekeeping activities from the primary task of loop control (Figure 5). At the block-diagram level, the Si8250 digital-power-controller family performs the functions of TI's UCD9k

family, though their internal architectures significantly differ. That fact leaves you to provide the driver and current sensing that the TI UCD7k family provides. However, a cursory search reveals some 15 reputable vendors of power-MOSFET drivers, so it is reasonable that Silicon Labs didn't reinvent the wheel when developing its first power-controller ICs.

One advantage of the Si8250 that is evident at first glance is its size: The dual-processor controller fits into QFN-28 and LQFP-32 packages. In exchange for the reduced pinout, the SiLabs part does without some of the ADC's multiplexer width—eight rather than 16 channels—and the 8250 family provides a somewhat more modest complement of digital-I/O facilities than does the UCD9k, which devotes more pins that function—35—than does the entirety of the 8250's package. (Ironically, perhaps, the Si8250 manages to fit in six PWM outputs—the busi-

ness end of these devices—compared with the UCD9k's three.) If you can do with the more modest facilities of the \$2.49 (1000) Si8250, another benefit in addition to its relatively reduced girth is a maximum dissipation of 69 mW.

The 8250 operates with an internal 25-MHz system clock. An internal PLL-based clock multiplier derives 50-, 100-, and 200-MHz clocks for the loop-control ADC, DPWM, and some peripherals. Programmable options include operation with an external clock with an on-chip, 3-bit programmable prescaler and an integrated 80-kHz, low-frequency clock, which is useful for certain low-power, nonoperational modes.

Silicon Labs provides a dedicated 10-MHz, 6-bit loop-control ADC and a separate 12-bit ADC with an eight-channel multiplexer for current, temperature, and other housekeeping measurements. The loop-control ADC meets 2- and 1-bit

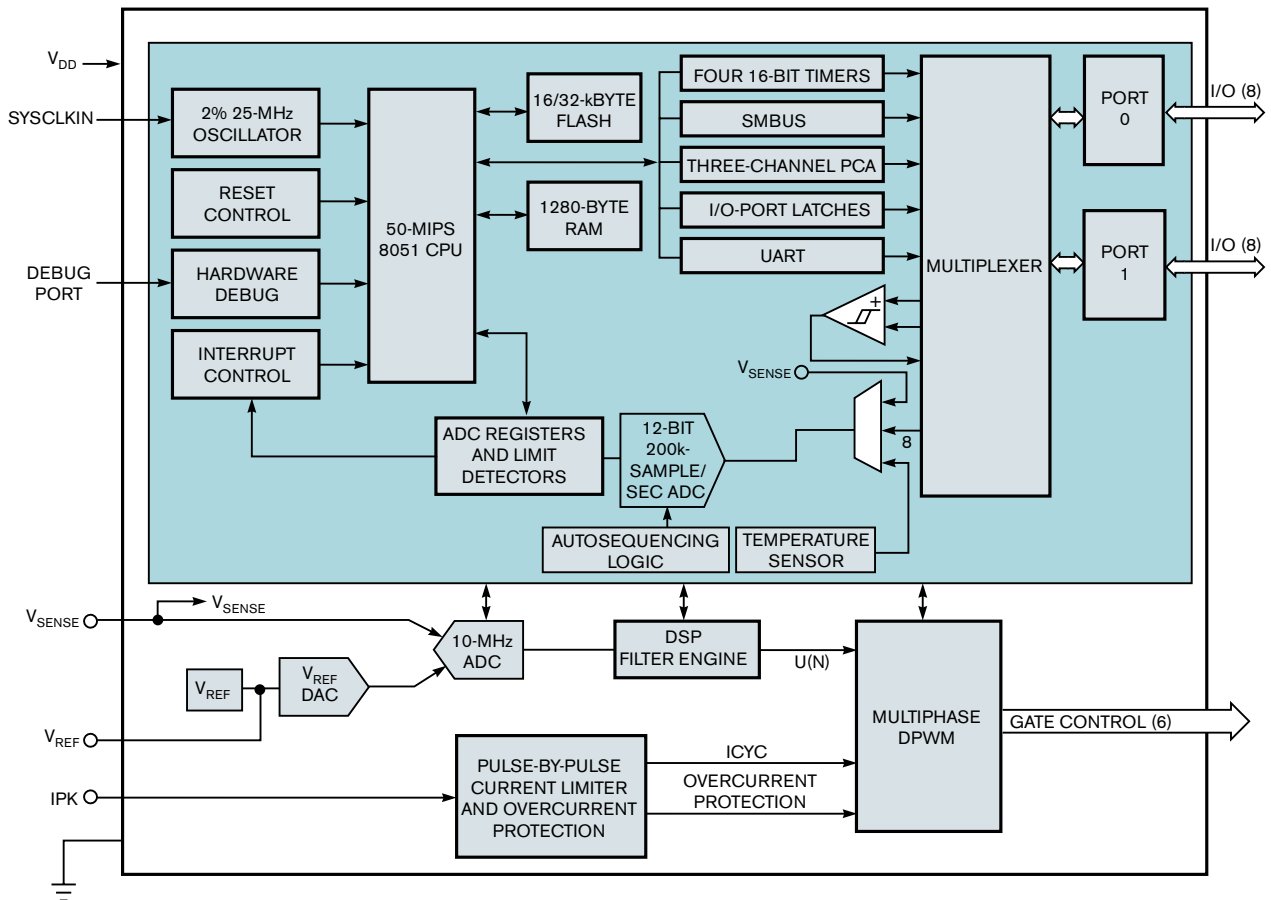


Figure 5 The Silicon Laboratories Si8250 commits a dedicated ADC and DSP-filter engine to loop control. A separate ADC and 8051 attend to such housekeeping duties as temperature measurement and system communications.

INL- and DNL-limit specs, respectively—a bit chubby for a 6-bit converter from a specsmanship perspective, perhaps, but adequate for many power-controller applications. A reference DAC allows you to program the LSB size from 2 to 20 mV for a dynamic range of 128 mV to 1.28V. As yet, SiLabs has neither specified the loop-control ADC's ac performance, nor announced an intention to do so.

One unusual "feature"—in the "it's-not-a-bug-it's-a-feature" sense of the word—of the Si8250's 300-page data sheet is that the specification table does not exist in a single section. Instead, the document tucks away pieces of the table at the end of each table segment's relative text. This approach distributes information critical to the part-selection process and early-design phases throughout the book-sized data sheet. In many cases, you'll find spec-table fragments under subparagraphs that you might otherwise hardly notice. Although this organization may be useful for those who assembled the data-sheet source materials, it can be cumbersome for users of the resultant document. You may, therefore, wish to have the data sheet in PDF form on a laptop for quick text searches, particularly if you are developing your first application using the 8250. Alternatively, you can arm yourself with a healthy supply of Post-it Notes.

Among the support tools for the Si8250 family is a \$199 IDK, which features a GUI-based design interface and timing design wizard. The tool set comprises a real-time firmware kernel with C source code, microcontroller-configuration software, and a USB debugging adapter. **EDN**

REFERENCES

- 1 Black, Harry, "Stabilized Feedback Amplifiers," *Bell System Technical Journal*, Volume 13, January 1934.
- 2 Potter, Geof, "An introduction to digi-



You can reach
Technical Editor
Joshua Israelsohn
at jisraelsohn@edn.com.

MORE AT EDN.COM

+ **This just in:** We did not receive information about Primarion's or Zilker Labs' power converters in time for *EDN's* print edition, but you can read about them and news about an upcoming related conference in the online version of this article at www.edn.com/072105df1.

+ **Politically correct power:** Power-semiconductor vendors ease OEM's efforts to comply with international power-factor-correction requirements. See www.edn.com/article/CA608153.

+ **Digitally controlled power-controller methods and challenges** are in some ways reminiscent of those that Class-D amplifiers face. Read **Class D Gen 3** at www.edn.com/article/CA408383 to make the comparison and note the differences.

tal control of switching power converters," Astec, April 2004.

3 Israelsohn, Joshua, Gary Levy, and Ron Gatzke, "A circuit board layout guide for RFICs," EOEM Design Expo, June 2005, www.eoemdesignexpo.com.

FOR MORE INFORMATION

DIGITAL POWER CONTROLLERS

Primarion
www.primarion.com

Silicon Laboratories
www.silabs.com

Texas Instruments
www.ti.com

Zilker Labs
www.zilkerlabs.com

POWER-MOSFET DRIVERS

Allegro
www.allegromicro.com

Fairchild Semiconductor
www.fairchildsemi.com

International Rectifier
www.irf.com

Intersil
www.intersil.com

Ixys
www.ixys.com

Linear Technology
www.linear.com

Maxim Integrated Products
www.maxim-ic.com

Micrel
www.micrel.com

Microchip
www.microchip.com

National Semiconductor
www.national.com

On Semiconductor
www.onsemi.com

Semtech
www.semtech.com

Siliconix
www.vishay.com

STMicroelectronics
www.st.com

Texas Instruments
www.ti.com