

PCI Express and USB 2.0 improve performance of PC-based measurements

ADVANCES IN PC AND SILICON TECHNOLOGIES ALLOW LOW-COST, PC-BASED PLUG-IN DEVICES TO ACCURATELY AND QUICKLY PERFORM MEASUREMENTS AND CONTROL.

As PC technology has evolved, the ability to use standard desktop and portable computers for sophisticated test, control, and design applications has improved dramatically. Economies of scale have made it more cost-effective to use the gigahertz-speed processing and gigabytes of memory on standard computers than for vendors to install processors and memory in measurement instruments. Meanwhile, test-and-control vendors have repurposed commercially available silicon technologies. For example, ADCs and DACs for electronic devices, such as cellular phones and DVD players, now also provide speed and accuracy for PC-based data-acquisition devices. These high-production commercial components are available at fractions of the cost and in much faster design cycles than it would take for instrumentation vendors to design their own components. With these advances in PC and silicon technologies, low-cost, PC-based plug-in devices can now perform measurements and control with accuracy and processing speed that traditional instruments lack.

As acquisition rates increase, a common bottleneck for these virtual instruments has been the ability to quickly and easily transfer data from the measurement device into PC memory. Traditional bus technologies, such as GPIB and RS232, often require instrumentation vendors to install local memory on the instrument to temporarily store data that cannot move to the PC fast enough because of bus-bandwidth limitations. As the PC industry over the past decade standardized the PCI bus, plug-in devices for this bus realized a 77-times increase in data bandwidth versus GPIB, and, in many cases, this increase reduced the requirement for deep onboard memory. Meanwhile, cabled-bus technologies, such as USB, became popular for test-and-measurement applications because of their portability and ease of use. As virtual instruments acquire more data at faster rates by using the lat-

est ADC and DAC technologies, systems using PCI and USB have again encountered the bus itself as the limiting factor in efficiently transferring data to PC memory. To address this increasing hunger for bandwidth, new technologies, including PCI Express and high-speed USB 2.0, are enabling designers to stream huge amounts of data from devices to the PC, ensuring backward compatibility, and improving ease of use.

PCI EXPRESS HAS ARRIVED

PC and peripheral vendors, including Intel, jointly developed PCI Express and last year began shipping it in standard desktop PCs. Most desktop machines from the leading suppliers include at least one PCI Express slot. PCI Express maintains software compatibility with traditional PCI but replaces the physical bus with a 2.5-Gbps serial bus. Data travels in packets through “lanes,” pairs of transmitting and receiving signals that enable 250-Mbyte/sec bandwidth per direction per lane. Designers can

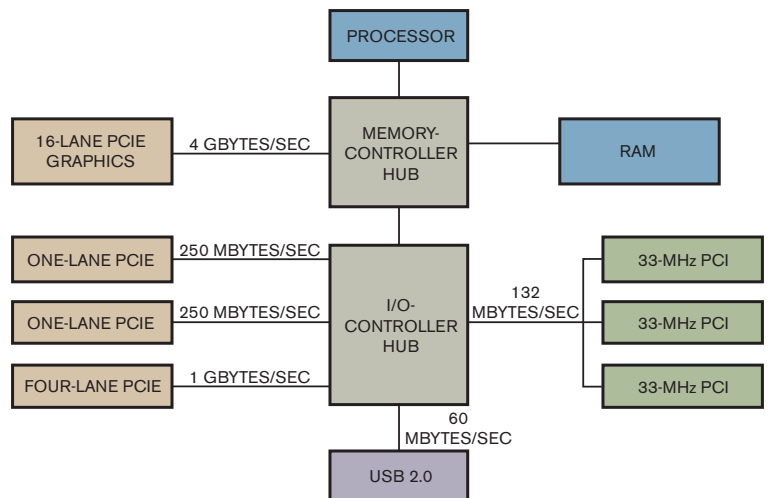


Figure 1 Each PCI Express slot has dedicated bandwidth to memory, unlike PCI, which shares bandwidth.

group multiple lanes of two, four, eight, 12, 16, and 32 to increase bandwidth to the slot. And, unlike PCI, which divides bandwidth between all devices on the bus, PCI Express provides dedicated bandwidth to each slot in the system.

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PCI Express incorporates an isochronous data-transfer mode, allowing a device to reserve a defined amount of bandwidth with deterministic latency. Data-acquisition applications also benefit from this feature, because PCI Express devices require less memory than traditional PCI for data-buffering purposes (**Figure 1**).

BANDWIDTH AND LATENCY

Applications such as data acquisition and waveform generation require guaranteed bandwidth and deterministic latency—the time for a system to send and another system to receive a signal, such as a configure or start command. Sufficient bandwidth ensures that data can transfer to memory fast enough without becoming lost or overwritten. Long latency is characteristic of buses such as Ethernet and is a primary reason that PC-based test-system vendors have not widely adopted this bus. The original PCI specification did not address these issues because high-speed-data-streaming applications on the PC were not prevalent at the time. As a result, data-acquisition devices that adopted the bus required onboard memory for data buffering to handle the varying bandwidths available during data transfers (see sidebar “Data-acquisition devices emerge”). Today, isochronous data transfers such as uncompressed streaming audio and video require the I/O subsystem of the PC to provide guaranteed bandwidth and deterministic latency to prevent data glitches. To address these needs,

PCI Express dramatically improves data bandwidth. The initial signaling frequency of 2.5 Gbps with a 16-lane slot provides as much as 30 times (60 times in two directions) the usable bandwidth of 32-bit, 33-MHz PCI, and, with advances in silicon technology, this signaling frequency should increase toward 10 Gbps—the practical limit for signals in copper. Because of the lane topology of PCI Express, data-acquisition-system vendors can implement a PCI Express connector with the number of lanes suitable to the requirements of the device. They can plug devices with smaller connectors into larger host connectors on the motherboard, improving hardware compatibility and flexibility (**Figure 2**).

SOFTWARE COMPATIBILITY IS PARAMOUNT

The PCI Express specification also ensures software compatibility. The configuration space and programmability of PCI Express devices remain unchanged from the traditional PCI

DATA-ACQUISITION DEVICES EMERGE

National Instruments recently released the industry's first PCI Express data-acquisition devices (**Figure A**). The new NI PCIe-6251 and 6259 devices combine the high-performance PCI Express bus with the technological advancements of National Instruments M Series devices to offer engineers and scientists fast analog and digital I/O with the dedicated per-slot bandwidth of PCI Express. The new devices feature as many as 32 analog channels with 16-bit, 1.25M-sample/sec speed, and 10-MHz digital I/O on as many as 32 lines. They use a one-lane PCI Express connector; one lane is the most common PCI Express lane width on currently shipping desktop PCs. These two

new data-acquisition devices complement the PCI Express image-acquisition and GPIB devices that the company released in 2004.

As with other NI M Series DAQ devices, the new NI PCIe-6251 and NI PCIe-6259 feature the NI-STC 2 system controller, the NI-PGIA 2 amplifier, and NI-MCal calibration technology for increased performance, accuracy, and I/O. The devices are part of the high-speed M Series family, offering as many as four analog-output channels at 16 bits at 2.8 MHz and 32 high-speed digital lines at 10 MHz. The devices also include 48 digital-I/O lines and two 32-bit counter/timers. The devices come with measurement software, including NI-DAQmx

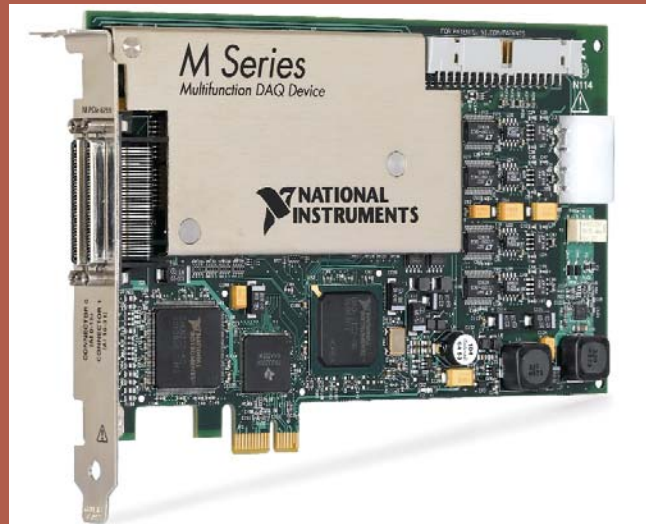


Figure A The NI PCIe devices offer fast analog and digital I/O with the dedicated per-slot bandwidth of PCI Express.

driver software and VI Logger Lite data-logging software. Because of the software compatibility that the PCI Express standard

provides, all examples and applications for PCI-based M Series devices are compatible with their new PCI Express counterparts.

methodology. All operating systems can boot without modification on a PCI Express architecture. At boot time, the operating system can discover all of the PCI Express devices present and then allocate system resources, such as memory, I/O space, and interrupts to create an optimal system environment. And, because the PCI Express physical layer is transparent to application software, programs written for PCI devices can run unchanged on PCI Express devices that have the same functions. This backward compatibility of PCI Express software with traditional PCI is critical in preserving the software investments of both vendors and users.

Similar to the improvements PCI Express offers plug-in devices, high-speed USB 2.0 has improvements in bandwidth and signal latency for externally cabled data-acquisition devices. USB has become the de facto standard for cabling peripheral devices to the PC, and data-acquisition devices are no exception. The plug-and-play and hot-pluggable features of the bus make it easy to use, enabling a host PC to automatically detect and configure a connected device. Users can dynamically load and unload drivers without powering down the device or PC during installation. USB 2.0 also provides power on the same cable that carries the data signal, often simplifying connectivity and portability by eliminating dedicated ac power cables.

The USB 2.0 specification made significant improvements in both bandwidth and latency versus USB 1.1. The 1.5-Mbyte/sec rate that USB 1.1 provided quickly became a limiting factor for large data transfers, such as those for high-speed data acquisition. High-speed USB 2.0 improved that rate by 40 times, enabling bandwidths as large as 60 Mbytes/sec. Like PCI Express, USB 2.0 provides isochronous transfers but also adds three data-

AS PC-BUS TECHNOLOGIES, SUCH AS PCI EXPRESS AND USB 2.0, CONTINUE TO IMPROVE DATA BANDWIDTH, PERFORMANCE, AND EASE OF USE, THE BENEFITS OF USING PC-BASED DEVICES FOR MEASUREMENTS AND CONTROL BECOME EVEN MORE DRAMATIC.

transfer modes that the manufacturer can enable. For example, the bulk-transfer mode provides data-reception confirmations to ensure error-free transfer for applications such as data acquisition in which data integrity is paramount.

The release of the USB 2.0 standard created low-speed, 1.5-Mbps; full-speed, 12-Mbps; and high-speed, 480-Mbps classes of USB devices. USB 2.0 is both forward- and backward-compatible with USB 1.1, and low-speed, full-speed, and high-speed devices can all coexist on a single USB port. In addition to bandwidth improvements, USB 2.0 also introduced ways to improve the efficiency of data transfers. Data frames—the time segments for packet transfers—decreased from 1 msec to eight 125- μ sec frames, and the number of data bytes transferred per frame sig-

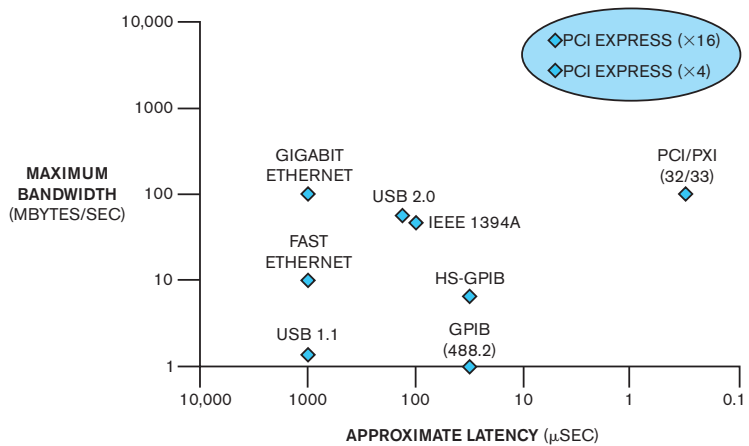


Figure 2 PCI Express dramatically improves data bandwidth.

nificantly increased. Because large data packets can consume large amounts of bandwidth, new handshaking commands ensure that the host is ready and able to receive the entire queued data packet. USB 2.0 also introduced split transactions, which prevent full- and low-speed devices from slowing the bus. With split transactions, the host can communicate with high-speed devices on the bus without waiting for slower devices to return communication.

WHAT'S AHEAD?

As PC-bus technologies, such as PCI Express and USB 2.0, continue to improve data bandwidth, performance, and ease of use, the benefits of using PC-based devices for measurements and control become even more dramatic. By virtue of being based on computer technology, virtual instruments will always improve as new communication, processing, and memory technologies come to market. As PCI Express and USB 2.0 continue in their adoption cycles, hybrid systems for several years will use these new technologies in addition to traditional PCI and USB 1.1 buses and devices. The software compatibilities of the new technologies as well as the physical compatibility between USB 1.1 and USB 2.0 will bridge these devices with their predecessors. But the benefits of these two new technologies are clear, and, as PC-based test-and-control systems continue to push bandwidth requirements, PCI Express and USB 2.0 will enable faster data transfers to PCs, which can fully use the ever-increasing processor speeds and memory depths. USB 2.0 has spurred a whirlwind of new, easy-to-use data-acquisition devices, and, with the release of PCI Express, the next generation of plug-in data-acquisition devices adopting the new bus standard is sure to follow. **EDN**

AUTHOR'S BIOGRAPHY

Brian Betts is data-acquisition-systems group manager at National Instruments. He has a bachelor's degree in mechanical engineering from Texas A&M University (College Station, TX). You can reach him at brian.betts@ni.com.