

The secrets of successful communications using LVDS

RELIABLE SINGLE- AND MIXED-TECHNOLOGY LVDS DESIGNS REQUIRE ATTENTION TO VOLTAGE LEVELS, NOISE MARGINS, AND DRIVE LEVELS.

Many choices now exist for LVDS (low-voltage differential-signaling) devices. Versions of these devices often coexist in the same system, which creates interoperability concerns. Among the available and practical versions, designers can choose from LVDS, bus-based LVDS, and M-LVDS (multipoint LVDS). Can these devices work in the same system? What issues should designers address when trying to mix these technologies in a system? What limitations do the combination of similar but different devices impose?

Each LVDS technology has strengths and limitations. When you compare them with single-ended signaling, LVDS technology's strengths include lower power, higher speed, and lower EMI. Technological limitations include the topologies they support, the number of nodes they allow, drive capability, and standard compliance. Standards minimize integration concerns; for example, the TIA/EIA-644A standard specifies the performance of LVDS devices for point-to-point and multidrop applications.

The TIA/EIA-899 standard for M-LVDS specifies requirements for multipoint devices. When developing a system from scratch, a homogeneous system is the best choice. The reality is, however, that systems often contain modules from various vendors, each complying with variants of the LVDS physical layers. The following guidelines will identify potential pitfalls and help designers to avoid them when integrating LVDS-I/O types. Examining M-LVDS devices demonstrates the range of I/O levels that this technology supports.

Table 1 highlights the key device parameters for the most common classes of LVDS devices. The TIA/EIA-644A standard and its predecessor, TIA/EIA-644, define the requirements for point-to-point (one driver, one receiver) and multidrop (one driver, multiple receivers) devices. Designers can connect as many as 32 receivers in a TIA/EIA-644A bus. Drive current is 3.5 mA, which is enough for single-termination applications but insufficient for double-terminated designs.

Bus-based LVDS increases the drive-current strength and preserves most of the features of the TIA/EIA-644A standard. These technologies share the same receiver common-mode range and receiver threshold as TIA/EIA-644A. They are driver enhancements of TIA/EIA-644A. M-LVDS provides a full complement of true multipoint features. Its drive capability of 11 mA supports double termination or

heavily loaded backplanes. The receiver threshold is half that of the other technologies, thus providing more sensitivity. The receiver's ground-potential offset, relative to the driver, is twice that of other technologies. M-LVDS provides a superset of features of the other bus-based LVDS technologies and complies with an industry standard.

TRANSMITTER AND RECEIVER SPECIFICATIONS

In the driver-parameter section in Table 1, the test load is the impedance that the test circuit uses for measuring and reporting data-sheet specifications. The output differential voltage, V_{OD} , is associated with this test load. The driver-output current is the derived load current that the device sources to achieve the indicated output-differential-voltage value. Designers can more meaningfully compare the technologies by normalizing driver strength, using a common test impedance. The normalized output-differential-voltage value assumes that each transmitter acts as an ideal current source and that this current source drives a 100Ω load. None of the technologies in the table truly respond like an ideal current source over a wide range of loads, but the assumption is fairly accurate for each technology and allows meaningful comparisons.

Table 1 also shows that all classes of signaling, except M-LVDS, have a receiver threshold of 100 mV. M-LVDS receivers are twice as sensitive as the other technologies, providing improved noise margin over the other LVDS receivers. Low-voltage-signaling technologies generally find use in short-distance data transmission. A ground-potential difference of ±1V

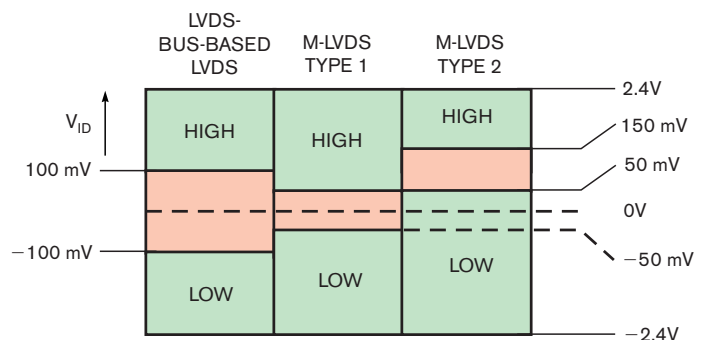


Figure 1 A comparison of receiver threshold voltages shows the differences among various technologies.

TABLE 1 COMPARISON OF MAJOR LVDS-FAMILY SPECS

| | LVDS TIA/EIA-644A | Bus-based LVDS Nonstandard | M-LVDS TIA/EIA-899 |
|--|---------------------------|-------------------------------|---------------------------|
| Driver parameters | | | |
| Test load (Ω) | 100 | 27 to 50 | 50 |
| Output differential voltage (V_{OD}) (mV) | 350 | 350 | 565 |
| Driver output current (I_{OD}) (mA) | 3.5 | 7 to 11.1 | 11.3 |
| V_{OD} normalized (100 Ω) | 350 mV | 700 mV to 1.11V | 1.13V |
| Steady-state-output common-mode voltage ($V_{OC(SS)}$) (V) | 1.2 | 1.2 to 1.3 | 1 |
| Receiver parameters | | | |
| Input threshold voltage ($V_{I(Th)}$) (mV) | 100 | 100 | 50 |
| Common-mode voltage (V_{ICM}) (V) | 0 to 2.4 | 0 to 2.4 | -1 to 3.4 |
| Voltage-potential difference (V_{GPD}) (V) | 1 | 1 | 2 |
| Fail-safe operation | Nonstandard | Nonstandard | Type 2-standard compliant |
| Supported architecture | | | |
| | Point-to-point, multidrop | Multipoint | True multipoint |

had been the required performance specification until the release of the M-LVDS standard. M-LVDS doubles the allowable ground shift between drivers and receivers and ensures that receiver dynamic range is wide enough to handle multipoint applications, in which enabling and disabling of drivers is common. Manufacturers incorporate various fail-safe operation into receivers, so designers must pay attention to the fail-safe each device incorporates. The M-LVDS standard clearly specifies fail-safe operation.

M-LVDS provides many additional features to support true multipoint operation. A common application of M-LVDS devices is in multislot backplanes. Such systems have numerous impedance mismatches due to transmission-path stubs at the backplane connectors and line cards. To minimize the reflection from these stubs, M-LVDS specifies a controlled rise time, setting a minimum allowable transition time of 1 nsec. This edge rate limits the maximum achievable signaling rate, but it places no real restriction on applications because multipoint signaling is generally limited to 200 to 400 Mbps.

M-LVDS bus drivers never drive voltages greater than 2.4V, even under conditions of driver contention. This voltage limitation, coupled with the specification for receivers to operate over a wide range, ensures that a homogeneous M-LVDS system will operate and that the receivers will always be able to determine the correct bus state.

LVDS and bus-based LVDS all require receiver operation over

a 0 to 2.4V range. This requirement effectively allows for a voltage-ground-potential difference of 1V. M-LVDS requires a range of -1V to +3.4V, which allows for a greater offset in ground potential. This increased common-mode range ensures that an M-LVDS receiver can accept LVDS, bus-based LVDS, and M-LVDS signals, thus positioning M-LVDS as a flexible receiver technology when designing mixed-use systems.

Another feature of M-LVDS, fail-safe operation, refers to the response of receivers under certain fault conditions or when drivers are inactive. Until TIA/EIA-899 emerged, many ways existed to accomplish fail-safe operation for LVDS technologies. Some of these techniques rely on external circuits to provide known outputs, whereas others are integrated approaches that force outputs to a known state. These methods are sometimes not interchangeable; thus, designers must heed how the data sheet specifies fail-safe operation. Bus-based LVDS technologies are enhanced driver specifications, and they address fail-safe operation in the same manner that LVDS does. In other words, no standard exists for fail-safe operation. Closely examine data sheets because this parameter can change from device to device.

The TIA/EIA-899 standard defines the fail-safe requirement, which must function over the full common-mode range of the driver. The standard identifies 50-mV-threshold Type 1 receivers and 100-mV-offset-threshold Type 2 receivers, which detect open-circuit and idle-bus conditions. Type 1 receivers are similar to LVDS receivers but with a more sensitive threshold range. Type 2 receivers provide standardized fail-safe operation by requiring an offset threshold. Type 2 receivers “see” signals lower than 50 mV as low, whereas they see those higher than 150 mV as high (Figure 1).

DRIVER CONTENTION

What happens when more than one driver is active on a bus at once, and how does each technology deal with driver contention? A designer hopes that, at a minimum, no damage occurs and that the bus voltage stays within some limit. Driver contention does not occur in point-to-point or multidrop systems; hence, TIA/EIA-644A does not cover it. The nonstandard, bus-based LVDS technologies also do not cover this issue. However, M-LVDS, a comprehensive, multipoint standard, addresses driver contention. M-LVDS drivers monitor the bus

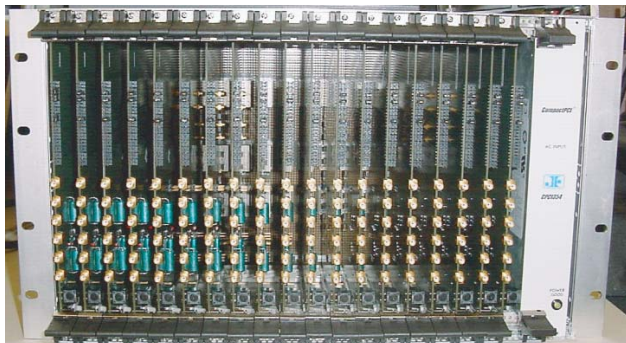


Figure 2 A full-scale hardware system confirms the results of analysis and predicted interoperability performance.

TABLE 2 COMPARISON OF OUTPUT-DIFFERENTIAL VOLTAGE IN LVDS TECHNOLOGIES

| Driver parameters | LVDS | Bus-based LVDS | M-LVDS |
|---|--------------|----------------|-------------|
| | TIA/EIA-644A | Nonstandard | TIA/EIA-899 |
| Test load (Ω) | 100 | 27 to 50 | 50 |
| Minimum output-differential voltage (mV) | 247 | 200 to 247 | 480 |
| Minimum output-differential voltage normalized to 100 Ω (mV) | 247 | 494 to 741 | 960 |
| Minimum output-differential voltage normalized to 40 Ω (mV) | 100 | 200 to 300 | 400 |

voltages and control the output current, such that the bus does not exceed 2.4V. TIA/EIA-899 also requires that disabled devices and receivers do not impact the bus in a manner that causes it to exceed the 2.4V limit. Considering these provisions, a homogeneous M-LVDS system does not see a bus voltage that exceeds 2.4V.

The driver's output voltage, receiver's threshold voltage, and receiver's common-mode voltage are important in addressing interoperability between classes of LVDS devices. Referring to **Table 1**, normalized-load-voltage technologies vary by a factor of almost three. This difference shows how mixing technologies in a point-to-point and multidrop system can become complex. Whether the receiver can handle these increased load-voltage levels depends on the receiver's common-mode-voltage range and maximum differential-input voltage. From the **table**, you can deduce that the M-LVDS receivers provide the widest common-mode-voltage range and that they can provide the greatest margin when interfacing to other drivers. This fact still does not provide the complete picture, though. Noise margin is a key concern to draw conclusions relating to interoperability.

Noise margin for differential-bus architectures is the minimum driver-differential-output voltage minus the maximum receiver-input threshold. The current-source assumption of **Table 1** generates the normalized voltages in **Table 2**, which provides the minimum differential-output voltage across data-sheet loads, normalized with 100 and 40 Ω test loads. The 40 Ω test-load value derives from realistic expectations for a multipoint-backplane system.

The standards fully define noise margin for standards-compliant devices. The TIA/EIA-644A standard provides for a minimum output-differential voltage of 247 mV and a maximum threshold voltage of 100 mV for a noise margin of 147 mV in a homogeneous system. The other bus-based-LVDS technologies do not comply with standards, so designers need to carefully study each bus-based-LVDS data sheet to calculate the

noise margin. For M-LVDS, the noise margin is 480–50 mV, or 430 mV. It is important to understand the load conditions. **Table 2** shows how output differential voltage can vary while the load changes. The **table** also raises questions concerning the noise margin that exists when the system uses mixed technologies.

M-LVDS DEMONSTRATION SYSTEM

Figure 2 shows a multipoint-M-LVDS demonstration system, illustrating the performance of M-LVDS in a realistic environment. The 21-card demonstration system has a 0.8-in. pitch between cards. The backplane traces have 130 Ω differential impedance. The connectors, devices, and stubs couple with tight card pitch to reduce the 130 Ω backplane impedance to an effective impedance of approximately 40 Ω . The demo uses 40 Ω for a multipoint backplane and 100 Ω for point-to-point comparison.

Table 3 provides calculated differential noise margin for a homogeneous system and various mixed technologies, using M-LVDS for normalization. Even though LVDS has less noise margin, it can drive any of the other technology receivers in a 100 Ω environment. Designers usually select LVDS for speed in a point-to-point system, and they choose M-LVDS if greater noise margin rather than speed is the relevant issue.

In a homogeneous system, M-LVDS provides the most noise margin for either a 40 or a 100 Ω architecture. This noise margin often provides a level of comfort for driving a signal through trace, connector, cable, and backplane, even in a point-to-point system. A true multipoint system creates loads that need more noise margin, which necessitates a technology such as M-LVDS. LVDS targets use in 100 Ω environments and thus is unsuitable for loads greater than those that the TIA/EIA-644A standard specifies.

The last area of concern for mixing technologies involves the receiver common mode. In most instances, the allowable ground-potential difference between driver and receiver for

TABLE 3 CALCULATED DIFFERENTIAL-NOISE MARGINS FOR SINGLE- AND MIXED-TECHNOLOGY

| Noise-margin parameters | Driver LVDS | Driver Bus-based LVDS | Driver M-LVDS | Driver LVDS | Driver Bus-based LVDS | Driver M-LVDS | Driver M-LVDS |
|--|---------------|-------------------------|-----------------|-----------------|-----------------------|---------------|-------------------------|
| | Receiver LVDS | Receiver Bus-based LVDS | Receiver M-LVDS | Receiver M-LVDS | Receiver M-LVDS | Receiver LVDS | Receiver Bus-based LVDS |
| Input threshold voltage (mV) | 100 | 100 | 50 | 50 | 50 | 100 | 100 |
| Differential voltage (V) | 247 | 200 to 247 | 480 | 247 | 200 to 247 | 480 | 480 |
| Minimum output-differential voltage normalized to a 100 Ω load (mV) | 247 | 494 to 741 | 960 | 247 | 494 to 741 | 960 | 960 |
| Minimum output-differential voltage normalized to a 40 Ω load (mV) | 100 | 200 to 300 | 400 | 100 | 200 to 300 | 400 | 400 |
| Noise margin with a 100 Ω load (mV) | 147 | 394 to 641 | 910 | 197 | 444 to 691 | 860 | 860 |
| Noise margin with a 40 Ω load (mV) | 0 | 100 to 200 | 350 | 50 | 150 to 250 | 300 | 300 |

LVDS and nonstandard-bus-based technologies is $\pm 1V$. Although this value is approximately correct, the designer needs to understand the allowable effects that the receiver can withstand under extremes of specification limits. For LVDS, the driver has a common-mode-output range of 1.125 to 1.375V, with 1.2V as the typical value. LVDS receivers accept an input of 0 to 2.4V, which means that the receiver can have a ground shift that can be approximately 1V. This shift value may actually be less if the driver provides the maximum output differential voltage—such as 450 mV at 1.375—at the high end of the common-mode range. This requirement means that the allowed ground shift is only 800 mV. Some vendors offer receivers, such as the SN65LVDS33D, with larger input ranges—in this case, -4 to $+5V$. The TIA/EIA-899 specification for M-LVDS requires an input-voltage range of -1 to $+3.4V$.

LVDS is an appropriate technology for point-to-point- and multipoint-system technologies. LVDS and M-LVDS interfaces are based on standards, whereas the other bus-based-LVDS technologies are not. LVDS technologies offer speed improvements, lower power, and better EMI than older, single-ended- bus technologies. A homogeneous system is the best design option, but the interface technologies are sometimes mixed. In such cases, designers should never exceed the data-sheet limits, must take noise margins into account, and must understand the common-mode range of the application. M-LVDS provides a new type of LVDS that can either increase the noise margin over other options or provide a true multipoint approach when a design requires it. Fail-safe operation, driver contention, and compliance are all available with M-LVDS implementations. Each technology has its place, and interoperability is possible if designers take the appropriate steps.**EDN**

MORE AT EDN.COM 

 We encourage your comments! Go to www.edn.com/ms4146 and click on Feedback Loop to post a comment on this article.

AUTHORS' BIOGRAPHIES

Jim Dietz is systems-engineering manager at Texas Instruments, where he provides strategic-marketing and applications support for TI's high-speed-interconnect portfolio. He has a master's degree in systems engineering from Texas Tech University (Lubbock, TX), a master's degree in international management studies from the University of Texas—Dallas, and a bachelor's degree in electrical engineering from Clarkson University (Potsdam, NY).

Richard Hubbard is a new-product-development/characterization manager at Texas Instruments, where he manages LVDS/M-LVDS/CML (current-mode logic)/LVPECL (low-voltage positive-emitter-coupled-logic)-device development, including buffers, translators, crosspoint switches, and serializers/deserializers. He has a master's degree in business administration from the University of Texas—Austin and bachelor's degrees in electrical engineering and liberal studies from the University of Central Florida (Orlando, FL). His other interests include raising his five-year-old son, painting, reading, bowling, and pursuing higher education opportunities.