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designideas

READERS SOLVE DESIGN PROBLEMS

LC oscillator has stable amplitude

Julius Foit, Czech Technical University, Prague, Czech Republic

Many applications call for wide-range-tunable LC oscillators that can deliver a nearly constant-frequency, nearly harmonic-free output even when the circuit's output load changes. From a design viewpoint, eliminating either inductive or capacitive LC circuit taps and transformer couplings within the frequency-determining circuit simplifies fabrication and production, as does the option of grounding one side of the tuned LC circuit. These requirements suggest a circuit that can automatically and efficiently internally adjust loop gain, the basic criterion for oscillation. In addition, the circuit must provide sufficient gain to oscillate with low-impedance LC circuits and regulate the oscillation's amplitude to improve frequency stability and minimize THD (total harmonic distortion).

Designers have exploited many circuit topologies—some highly complex—in their attempts to achieve these design goals, but certain active devices' basic properties can help designers obtain acceptable behavior from a simple oscillator circuit. **Figure 1** shows a basic LC-oscillator arrangement. The amplifier operates as a noninverting voltage-controlled current source. The LC circuit converts the amplifier's output current, I_{OUT}, to voltage, V_{IN}, and applies it as input to the amplifier. **Equation 1** shows the formal condition for oscillation:

$$A_O = \frac{I_{OUT}R_D}{V_{IN}} \geq 1. \qquad (1)$$

In this **equation**, A_O is the overall voltage amplification and R_D is the LC circuit's dynamic resistance at its resonant frequency. In practical circuits, the value of R_D depends on the LC circuit's properties and thus can fall anywhere within a wide range. Also, **Equation 1** assumes an ideal amplifier—that is, one having characteristics that are independent of frequency.

Figure 1 and **Equation 1** yield a simple insight into the basic design problem: If the operation over a wide frequency range demands the use of several LC circuits with widely varying values of R_D, the amplifier's properties must be adjustable over a wide range. You can adjust the amplification to fulfill the gain-limitation condition for the worst-case LC circuit and then rely on device nonlinearities to reduce amplification under overdrive conditions. However, a heavily overdriven amplifier's input- and output-differential resistances can drop to a fraction of their optimum, high-resistance values. Second, large amounts of nonlinear distortion can impair frequency stability. Moreover, these effects depend

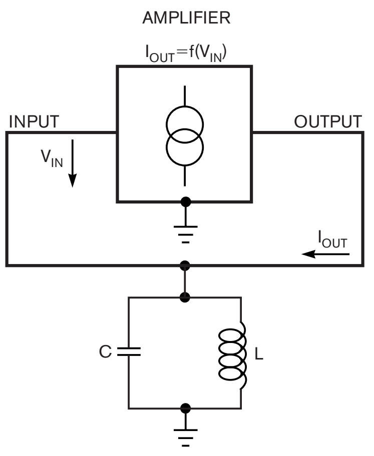

Figure 1 A parallel LC circuit and an amplifying voltage-to-current converter form a basic oscillator.

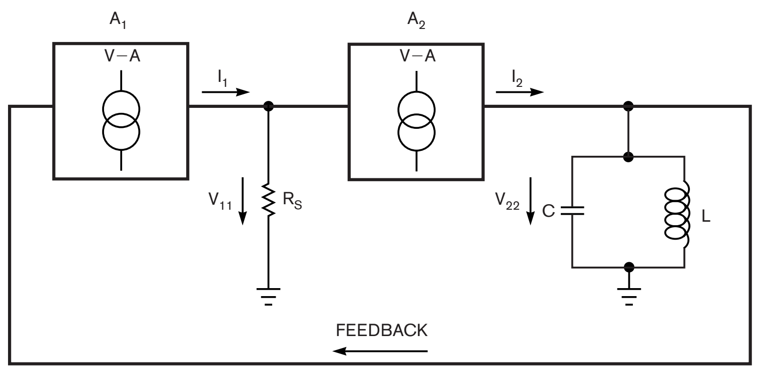

Figure 2 Adding a second voltage-to-current converter isolates the tuned circuit.

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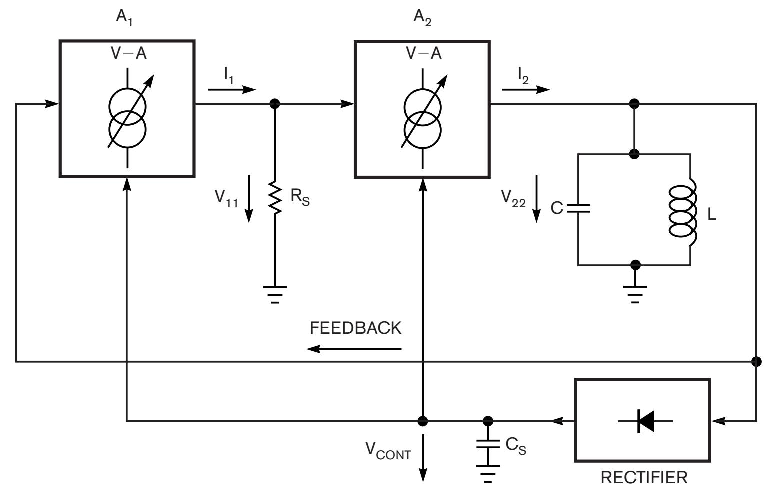


Figure 3 Rectifying a portion of the signal provides a gain-control voltage for the amplifiers.

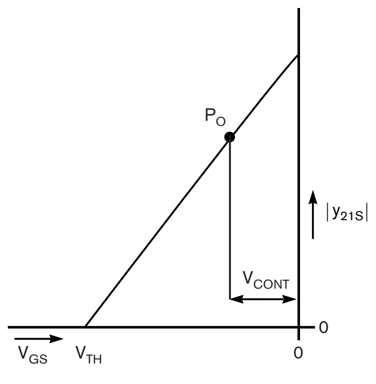


Figure 4 Control characteristics of an idealized JFET exhibit linear variation of forward transconductance versus gate-to-source voltage.

heavily on the amplifier's power-supply voltage, causing frequency stability to deteriorate if the supply voltage varies with load.

Various oscillator circuits use different designs within the amplifier block in **Figure 1**. The popular common-emitter or common-source transistor stage presents two important drawbacks: First, it's an inverting amplifier, and, second, its output does not behave as a good current source, especially when heavily overdriven. Attempts to avoid these problems include transformer coupling or providing impedance-matching taps on the LC circuit, both of which complicate the design and only partially solve the problems.

As **Figure 2** shows, another oscillator topology features two cascaded noninverting amplifiers, A_1 and A_2, as voltage-to-current converters (voltage-controlled current sources). In the circuit, coupling resistor R_S converts amplifier A_1's output current, I_{IN}, to voltage V_{IN}, and drives the second stage, A_2. The tuned circuit's dynamic resistance converts A_2's output current to output voltage, V_{22}, which feeds back to A_1's input to complete the positive-feedback loop. The overall loop amplification, A_{TOTAL}, appears in **Equation 2**:

$$A_{TOTAL} = A_1 \times A_2 = R_S R_D |y_{21S1}| \times |y_{21S2}|. \qquad (2)$$

In this **equation**, $R_D = Q\omega L$ is the dynamic resistance of the LC circuit at resonance at the ω frequency, Q is the quality factor of the LC circuit, A_1 and A_2 are the equivalent voltage amplifications of both amplifier stages, and $|y_{21S1}|$ and $|y_{21S2}|$ are the real parts of differential-forward-transfer admittances of both amplifying stages. For self-sustained oscillations, the basic condition $A_{TOTAL}>1$ in **Equation 1** must apply for all values of the LC circuit's dynamic resistance, R_D. In theory, this condition presents no problem; however, in practice, a situation arises in which the circuit must operate as an LC oscillator with a broad range of tuning inductances and capacitances; a wide range of tuned-circuit quality-factor Q, which the inductor primarily determines; a constant-amplitude output at any combination of conditions A and B; and the best possible frequency stability versus supply voltage and load.

Most LC oscillator circuits cannot simultaneously fulfill all of these requirements. Some oscillator circuits can sequentially fulfill some requirements, but none can fulfill all of them without complicating the circuit beyond reasonable limits. **Figure 3** shows a circuit deriving an external dc control signal from V_{22} to control the voltage-to-current-conversion coefficients—that is, amplification factors—of A_1 and A_2. Applying amplification control to both stages considerably increases the control's effectiveness. In addition to the original positive feedback for starting and sustaining oscillation, you can add an indirect negative-feedback path to the oscillator circuit to limit V_{22}'s amplitude. To meet the original design goals, amplifier blocks A_1 and A_2 should exhibit voltage-controlled input-versus-output characteristics, should possess linear-control amplification characteristics (**Figure 4**), should not invert the signal's phase, and should draw nearly no input current. Also, to emulate a current source, A_2 should present the highest possible differential internal output resistance.

The best active devices for both amplifier stages are the selected N-channel, medium-grade BF245Bs JFETs with a drain current of 5 mA at a gate-to-source voltage of 0V and a drain-to-source voltage of 15V. **Figure 5** shows the final circuit, in which Q_2 operates as a common-drain amplifier, A_2, and Q_1 operates as a common-gate amplifier, A_1.

The gate-source junction of Q_1 rectifies the ac voltage, V_{22}, across the tuned circuit. Coupling capacitor C_4

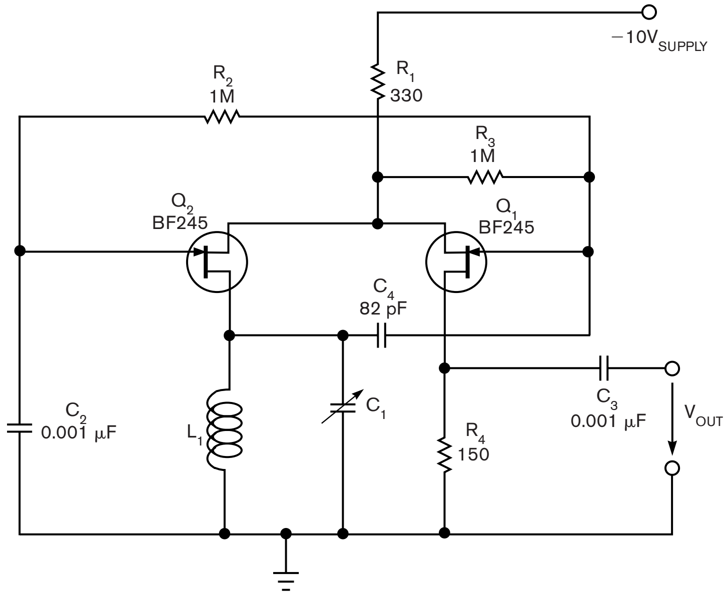
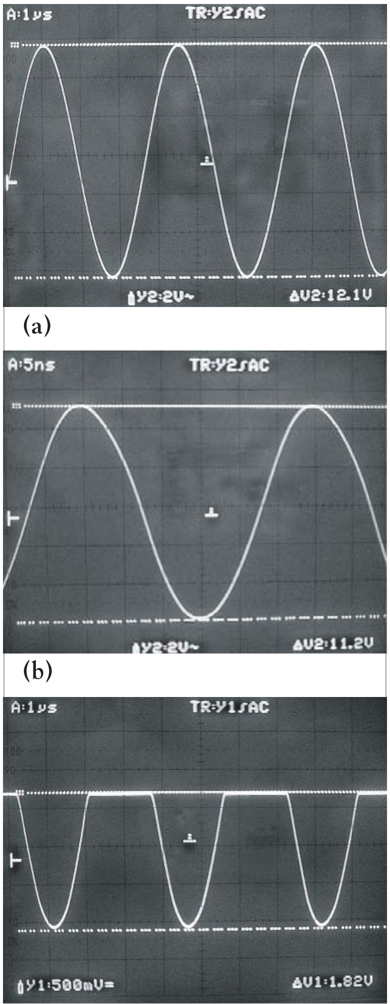


Figure 5 The completed oscillator circuit features a minimal component count.



(a)

(b)

(c)

Figure 6 A clean sine wave (V_{22} in Figure 3) appears across the tuned circuit at 280 kHz for values of 147 µH and 2200 pF for L_1 and C_1, respectively (a). The sine wave with respective values of 56 µH and 60 pF differ (b). The output waveform at 280 kHz, for values of 147 µH for L_1 and 2200 pF for C_1, exhibits a flat top (c).

in **Figure 5** doubles as dc-voltage-smoothing capacitor C_S in **Figure 3** because its bottom electrode connects to ground through the low dc resistance of tuning coil L. The dc-control voltage drives the gate of Q_2 through resistor R_2. Capacitor C_2 connects Q_2's gate to ground for ac signals, and Q_2 operates in common-gate connection because Q_1's source drives Q_2's source. To minimize frequency variations due to changing loads, a relatively low-value resistor, R_4, in series with Q_1's drain, isolates the output from the circuit's frequency-determining components. In addition, one lead each of L and C connects to ground.

The waveforms in **Figure 6a** and **6b** show no substantial change in the voltage across the tuned circuit even for widely different values of L and C. The voltage across the tuned circuit remains constant within 3% over a supply-voltage range of 8 to 30V. The same or better amplitude stability holds for the output voltage (**Figure 6c**), even at frequencies as low as 5 kHz and as high as 50 MHz with no adjustment of any passive-component values, except for L and C. Reducing the value of R_4 yields a smaller output voltage, further diminishing the effects of load variations on the operating frequency.

The dc level of the top, flat part of V_{OUT} rests at ground potential, and the waveform goes negative due to the negative power-supply voltage. Because of automatic-gain-control action, the waveshape remains remarkably consistent, regardless of frequency, exhibiting slightly rounded corners, mostly due to stray capacitances, at frequencies higher than 25 MHz. Only the LC circuit's ungrounded end provides a perfect sine wave. Other voltage and current waveforms exhibit cutoff distortion because both transistors operate roughly in Class B mode, shifting toward Class C at increasing power-supply voltages. You can extract a sine wave directly from the LC circuit, but variations in load impedance will influence the operating frequency.

On the other hand, the negative dc feedback controlling the gain of both transistors prevents even relatively large-load-impedance variations across the tuned circuit from greatly affecting the generated amplitude until the LC circuit's Q factor drops very low. At the expense of added complexity and a larger component count, you can include a buffer stage and extract a true sine wave from the LC circuit, but, in the circuit's original application as a radar-marker generator, the constant output amplitude ranked as of greater importance than the waveshape.EDN

(continued on pg 100)

Use a system's real-time clock to "hide" a code sequence

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Although the concept of a totally accessible system represents an ideal situation for users, designers now must limit access to—and conceal code sequences for—software routines for calibration, diagnostics, memory erasure, system reset, and more. In a system that includes a computer-compatible interface, such as an RS-232, a GPIB, or an infrared-I/O port, the system's software can detect unique input patterns and execute the "secret" code sequences. But if a system lacks a data port, any attempt to implement a secret-access feature in a publicly accessible user interface makes it transparent to the user, even if the feature includes password protection. This Design Idea offers an efficient way to activate a code sequence without making the customer aware that such a feature exists and without requiring any hardware modifications.

If a system includes an RTC (real-time clock), you can define a date and time stamp that invokes the hidden code. The date acts as a password, and, if you choose a date far in the past, a casual user would be unlikely to stumble across it. To implement the routine, you can modify the system software by inserting a date- and time-check routine at the location in which the hidden code executes. Under normal conditions, the program skips the hidden code and executes the routine only if the system's date matches the one that the routine specifies.

For example, the following pseudocode illustrates the use of Aug 12, 1980, as a system "password":

```
Check_date:
  if (Read_RTC(year)==1980 and
  Read_RTC(month)==8 and
  Read_RTC(day)==12)
                    run_hidden_sequence();
  Continue_the_Code();
```

After completing the procedure, you must remember to reset the system's clock to the current date and time. Otherwise, the system executes the special code for the remainder of the day until the clock rolls over to the next day. **EDN**

Shunt regulator eases power-supply-start-up woes

Michael O'Loughlin, Texas Instruments, Nashua, NH

The popular and multiply sourced TL431 three-terminal shunt regulator offers designers considerable versatility in its applications. **Figure 1a** illustrates the TL431's internal circuitry, which comprises a precision voltage reference, an operational amplifier, and a shunt transistor (**Reference 1**). In a typical voltage-regulator application, two external resistors, R_A and R_B, determine the shunt-regulated output voltage at the lower end of load resistor R_S (**Figure 1b**). By way of illustration, the TL431 and a few external active and passive components can serve as a low-power auxiliary power supply for an SMPS (switched-mode-power-supply) PWM (pulse-width-modulated) controller. In some power-supply designs, an auxiliary winding on the step-down transformer supplies power to the PWM controller. Under light output loads, the auxiliary winding may supply inadequate power to the PWM controller. For example, the converter circuit in **Figure 2** derives power for PWM controller IC_1 through an auxiliary bias winding, W_{AUX}, which is part of transformer T_1. Resistor R_T and capacitor C_{HOLD} form a trickle-charge circuit that supplies start-up power to IC_1. To conserve energy, resistor R_T supplies just enough current to trickle-charge C_{HOLD} to voltage V_{AUX}. Once the circuit starts, it

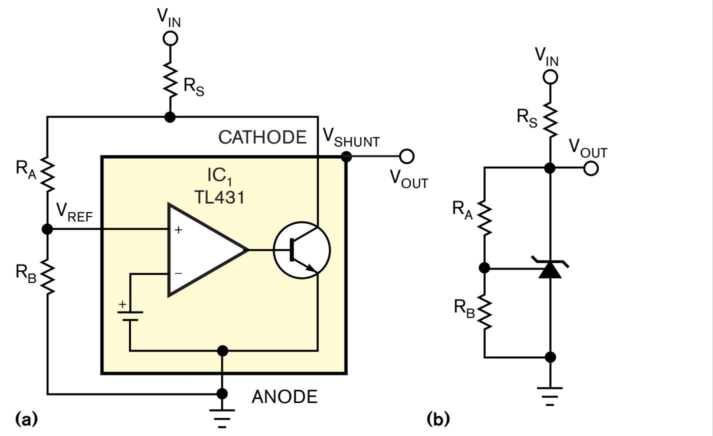

Figure 1 An uncomplicated block diagram (a) conceals the TL431's internal complexity, but you need only three external resistors to use the TL431 in a basic shunt-regulator circuit (b).

operates as you would expect and delivers output power to the load, and the auxiliary winding and its components power the PWM controller.

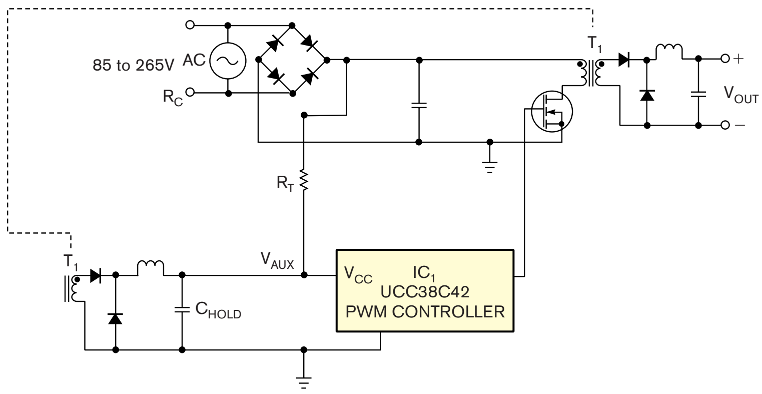

Figure 2 An auxiliary winding supplies power to the supply's PWM controller.

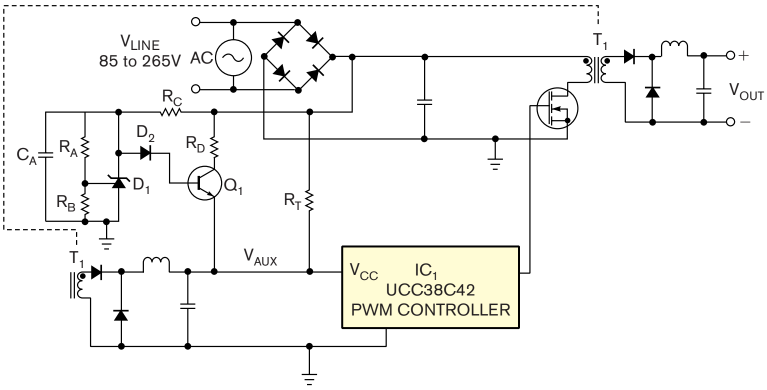

Figure 3 In this improved design, pulse-width-controller IC_1 derives its power from R_T for start-up, auxiliary winding W_{AUX} for normal operation, and shunt-regulator circuit IC_2 and Q_1 for low-load operation.

However, removing the output load reduces the energy supplied to the auxiliary bias winding, depleting the charge on C_{HOLD} and causing IC_1 to turn off, which in turn upsets output-voltage regulation and causes the power supply to operate erratically. A low-power bias-supply circuit supplies light-load start-up power and then switches off to conserve power whenever the auxiliary winding can supply enough energy to PWM controller IC_1 (**Figure 3**). In this circuit, a series-pass regulator turns on under light-load conditions and turns off when the bias winding can supply the energy to the PWM controller, thus conserving energy under load and improving converter efficiency.

Resistors R_A through R_D, shunt regulator IC_1, diode D_1, and transistor Q_1 form the low-load series-pass-regulated bias supply. You select these components to produce a voltage at Q_1's emitter that falls between IC_1's turn-off voltage and the nominal voltage produced by rectifying the auxiliary bias winding's output, V_{AUX_NOM}. In effect, the voltage at IC_1's V_{CC} pin follows in wired-OR fashion whichever is higher: V_{AUX_NOM} or the voltage at transistor Q_1's emitter. When the auxiliary bias winding and its components deliver sufficient power, Q_1's emitter sees a reverse bias, and Q_1 shuts off to conserve energy. Conversely, Q_1 supplies power when V_{AUX} decreases below V_{AUX_NOM} due to a light output load. Note that the circuit still must include trickle-charge resistor R_T because most PWM controllers incorporate undervoltage lockout, the ability to start at a higher than nominal supply voltage.

To design the series-pass regulator, select resistor R_C to supply sufficient operating current to IC_2, and select resistor R_D to maintain Q_1's collector voltage and current within its safe operating area. Select resistors R_A and R_B to set the series regulator's output voltage above IC_1's start-up voltage and below the nominal voltage supplied by the auxiliary winding's rectified output. Choose bypass capacitor C_A to minimize ripple voltage across IC_2.

You can use the following **equation** to adjust the voltage divider formed by resistors R_A and R_B:

$$\frac{V_{REF}}{R_B}=\frac{V_{AUX\_NOM}-V_{DI}-V_{BE(Q_1)}-V_{REF}-1V}{R_A}.$$

The voltage at Q_1's emitter must fall below the nominal auxiliary voltage, which the auxiliary bias winding supplies. V_{REF} represents shunt regulator IC_2's internal nominal reference voltage of 2.495V, and V_{D1} and $V_{BE(Q1)}$ represent D_1's voltage drop and Q_1's forward base-emitter voltage, respectively. **EDN**

REFERENCE

1. O'Loughlin, Michael, "Shunt regulator serves as inexpensive op amp in power supplies," *EDN*, Sept 15, 2005, pg 96, www.edn.com/article/CA6255051.