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## Are cell-based ASICs going away?

I can't count the number of conference sessions I've attended at which a speaker shows a market graph of ASIC-design starts. This chart, which is seemingly in every PowerPoint deck, shows a peak in these starts over the past few years with a dramatic drop in starts taking place in the next few years. I don't buy these projections.

Cost drives the pessimistic projection of ASICs in the future. A few years ago, everyone started talking about the cost of mask sets, and they are expensive. More recently, it's been the cost and time associated with verification that people often cite as the dominant cost component. In any event, the costs associated with 90-nm and finer geometry ASICs mean that only high-volume products justify the investment.

But what is high volume—especially in the age of 90-nm chips and 300-mm wafers? Smaller dice and larger wafers change the definition. All of a sudden, the demand for a product such as a communication chip for a router or switch, which many consider a high-volume product, can't fill a single tub of wafers per year. Outside PC processors, graphics processors, cell-phone basebands, and memory, not many ICs qualify as high volume on state-of-the-art process lines.

I recently attended the SOC (system-on-chip) conference presented by Savant. The “death-of-the-ASIC” chart appeared in several presentations, and the projected ASIC replacement was generally the structured or the platform ASIC. Such products combine preverified layers of a chip design with a minimal amount of mask processing for customization. Presumably, the result is something almost as dense as a cell-based ASIC with much lower NRE (nonrecurring-engineering) cost.

At the conference, Fujitsu, LSI

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Logic, Altera, eASIC, and others each spun its ASIC-replacement story. Most, however, failed to address the problem of volume production on state-of-the-art lines. Only eASIC has an answer for the volume issue. CEO Ronnie Vasishtha points out that, because the eASIC FlexASIC products require only the top via layer be customized, the company can manufacture multiple designs on one wafer. Vasishtha claims that the company's Direct-Write eBeam technology, which handles the top layer, is cost-effective even for mid-volume chips and that, as volumes grow, a design can move to a mask layer to handle the interconnect.

Although eASIC has an interesting technology, I'm still not sure that I see it as an ASIC replacement. My guess is

that it's less silicon-efficient than other structured-ASIC choices. In fact, eASIC may win more business as an IP (intellectual-property) provider of configurable-logic blocks to other IC vendors than as a fabless semiconductor company. The company's greatest success story to date came through a customizable IP block that it sold to STMicroelectronics, which used the eASIC IP to make a cell-based SOC design customizable.

At the end of the day, all of the analyst projections for declining ASIC starts and all of the structured-ASIC players rely on a common theory. Presumably, the move toward SOCs—more specifically, more functions integrated on a single die—requires that mainstream ASIC designs—or structured-ASIC designs replacing cell-based ASICs—must move down the Moore's Law curve to 90-nm and finer geometries. But do they? Clearly, examples exist of SOCs at the 180-nm node. I recently visited with Fujitsu, and the company's most recent high-profile product launch is an SOC for WiMax applications. Fujitsu produces that chip in a 180-nm process, although the company is eyeing 90 nm for the next-generation chip.

In the past, almost all chip designs moved through process reductions to lower cost through smaller dice while realizing performance gains and reductions in power. Today, only truly high-volume ICs, extremely large dice, or both realize a cost benefit from a 90-nm process and 300-nm wafers. Most ASIC designs today are at 180-nm and less dense geometries. These less dense ASICs have driven the recent peak in ASIC design starts. I believe that most ASIC designs will stay at these relatively low-cost geometries unless performance mandates a different choice. The payoff is in both affordability of the design upfront and fewer problems with static power consumption due to current leakage. That potential payoff may yet make those ASIC-design-start graphs look vastly different. **EDN**