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CMOS inverters convert RF to digital signal

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Applications ranging from frequency counting and synthesis to sensor signal conditioning require conversion of RF signals to digital-logic levels. In such situations, designers typically use a high-speed voltage comparator to perform the RF-to-digital conversion. Due to their high gain, voltage comparators typically exhibit good sensitivity but also present some drawbacks. High-speed comparators are expensive, difficult to find off the shelf, and prone to rapid obsolescence.

For frequencies as high as 180 MHz, the circuit in **Figure 1** offers an attractive approach. The IC in the design, a 74LVCU04 very-high-speed CMOS hex inverter, is available off the shelf and from many sources. Furthermore, many applications may already include three unused inverters. A single inverter, IC_{1A}, operating as a linear preamplifier, forms the converter's input

stage. Biasing resistor R₃ forces the inverter into its linear region by equalizing its input and output voltages at one-half of the power-supply voltage, V_{O1} = V_{I1} = (V_{DD}/2). Because the ac gain of a very-high-speed CMOS inverter is relatively low at RF (V_{O1}/V_{I1}) ≈ 7, additional gain stages follow the preamplifier. One self-evident approach—a cascade of additional inverters—presents poor stability at low frequencies and at dc when no RF source is present.

The circuit in **Figure 1** eliminates this drawback thanks to a topology based on a Schmitt trigger and amplifier circuit, IC_{1B} and IC_{1C}, that includes a frequency-dependent positive-feedback network comprising R₁, R₂, C_{D1}, and C_{D2}. Depending on the input frequency, the network exhibits two behaviors: At high frequencies, the decoupling-capacitor pair, C_{DC1} and C_{DC2}, short-circuits feedback resistor

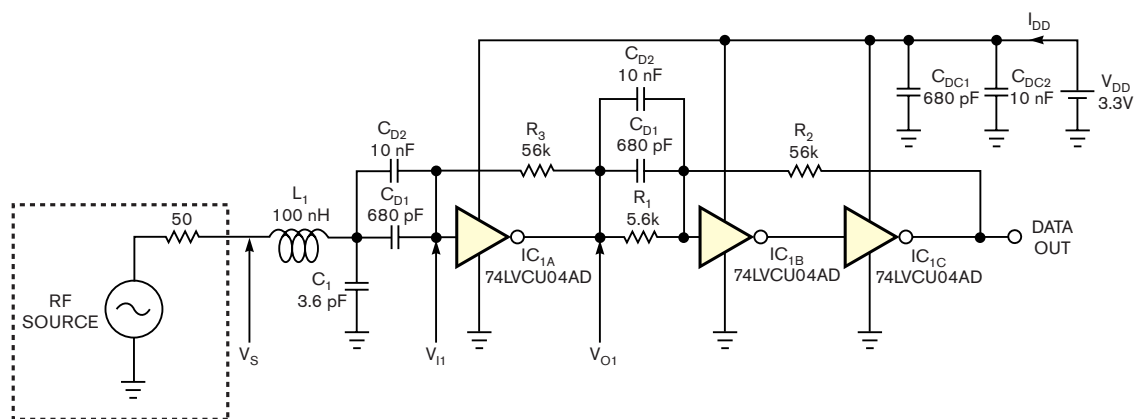
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R₁, canceling the time constant introduced by the positive-feedback network, R₁ and R₂, and the input capacitance of inverter IC_{1B}. Consequently, at high frequencies, the three cascaded, high-speed amplifiers that allow the best performance in input-signal bandwidth. At dc and low frequencies, the influence of coupling-capacitor pairs C_{D1} and C_{D2} is negligible, and inverters IC_{1B} and IC_{1C} and the positive-feedback network, R₁ and R₂, act as a Schmitt-trigger circuit. The choice of the high- and low-threshold voltages, V_{TH} and V_{TL}, at the Schmitt



NOTE:
ALL COMPONENTS ARE SURFACE-MOUNTED DEVICES.

Figure 1 Three high-speed CMOS inverters and a few passive components form an RF-to-logic converter.

trigger's input, V_{OI} , stems from a compromise between input sensitivity at V_S and ensuring unconditional stability of the comparator's output. **Equations 1** and **2** set the high and low threshold voltages, respectively:

$$V_{TH} = \frac{V_{DD}}{2} \left(1 + \frac{R_1}{R_2} \right) \approx 1.8V. \quad (1)$$

$$V_{TL} = \frac{V_{DD}}{2} \left(1 - \frac{R_1}{R_2} \right) \approx 1.5V. \quad (2)$$

To counteract a roll-off of sensitivity at higher frequencies, add a low-Q impedance-matching network comprising L_1 and C_1 at the comparator's input. Given the design objective of obtaining acceptable sensitivity at frequencies as high as 160 MHz, the network matches the 50Ω RF source and IC_{1A} 's input impedance, Z_{I1} , at 150 MHz. Unfortunately, manufacturers of digital ICs typically do not specify logic devices' input impedances. When designing the matching network, the first task involves using an Agilent (www.agilent.com) vector-network analyzer to measure the first inverter's input scattering parameter, S_{11} , at IC_{1A} 's input, V_{I1} . **Figure 2** shows a Smith-chart plot of the inverter's S_{11} parameter.

Knowing that

$$S_{11} = \frac{Z_{I1} - Z_C}{Z_{I1} + Z_C}, \quad (3)$$

with $Z_C = 50\Omega$, you can use the data in **Figure 2** to extract the first inverter's input impedance at the frequency of interest. At 150 MHz, this yields $Z_{I1} = 106.1\Omega - j116.7\Omega$ (at Marker 4 in **Figure 2**). To determine values for the matching network's components, you can use any of several software tools (**references 1** and **2**). If you are unfamiliar with Smith-chart computations, you can also proceed analytically with the following method:

1. Use series-to-parallel transformation formulas (**equations 4** and **5**) to transform the first inverter's input impedance into a parallel form:

$$R_p = \frac{R_S^2 + X_S^2}{R_S}. \quad (4)$$

$$X_p = \frac{R_S^2 + X_S^2}{X_S}. \quad (5)$$

Applying these formulas at 150 MHz yields: $R_p = 233\Omega$, and $X_p = -213\Omega$. (At 150 MHz, X_p represents an input capacitance, $C_p = 5$ pF)

2. Compute an initial version of the matching network to perform a match between the real part of the first invert-

er's input impedance, R_p , and the 50Ω RF source. Solving **equations 6** and **7** yields values for the matching network's elements (**Reference 3**):

$$L_1 = \frac{R_S}{\omega} \sqrt{\frac{R_p}{R_S} - 1}. \quad (6)$$

$$C_1 + C_p = \frac{1}{R_p \omega} \sqrt{\frac{R_p}{R_S} - 1}. \quad (7)$$

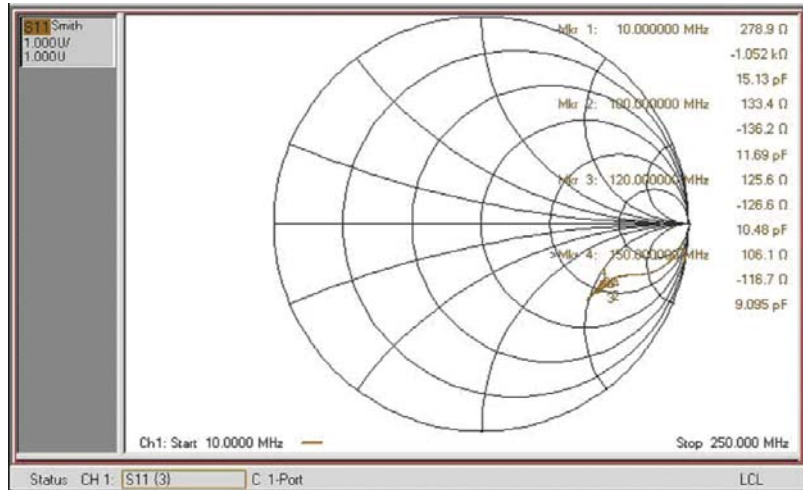


Figure 2 An Agilent N3382A vector-network analyzer obtained this S-parameter plot, which shows S_{11} measured at the first inverter's input for a source power level of -6 dBm.

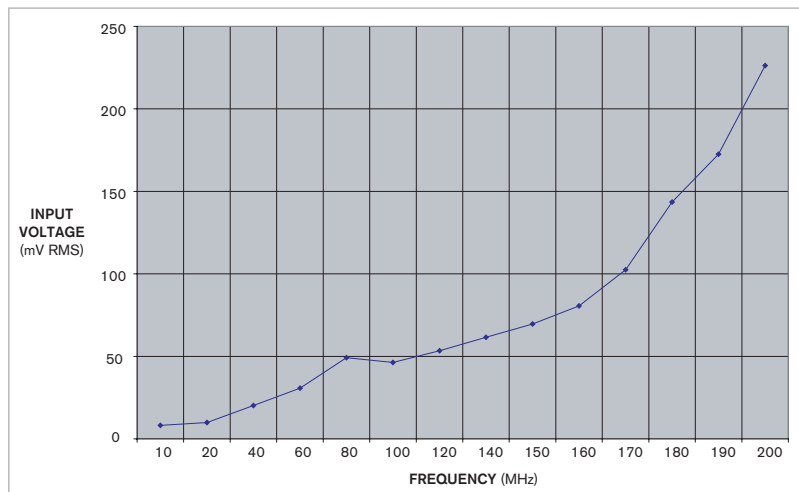


Figure 3 An input-level-versus-frequency plot of the RF-to-digital comparator measured from the RF source's reference plane to a clean logic output reveals less-than-100-mV sensitivity at 160 MHz and usable output to 200 MHz.

Applying these formulas at 150 MHz yields $L_1 \approx 100$ nH, and $C_1 + C_p \approx 8.7$ pF.

3. Subtract the inverter's input capacitance, $C_p = 5$ pF, from **Equation 7** to calculate a value for C_1 :

$$C_1 = \frac{1}{R_p \omega} \sqrt{\frac{R_p}{R_s} - 1} - C_p \approx 3.7 \text{ pF. (8)}$$

To build the circuit, use standard component values that fall closest to

the computed values: $L_1 = 100$ nH, and $C_1 = 3.6$ pF. As the plot of input frequency versus sensitivity in **Figure 3** shows, the circuit's increased sensitivity for 100- to 170-MHz frequencies clearly demonstrates the impedance-matching network's effectiveness. You can optimize the circuit's sensitivity in any other frequency band of interest by applying this method at the chosen frequency. The RF-to-digital-logic converter's power consumption does not change significantly for input signals of

10 to 180 MHz. Under worst-case conditions, the current drain does not exceed 58 mA for a supply voltage of 3.3V. **EDN**

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Instrumentation amplifier extends DSO

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To determine the specifications of a solar-generating plant, I needed to accurately measure the load current a product consumed. The product switched several internal devices on and off during an interval of several sec-

onds. An ammeter showed that the current transitions occurred too quickly for visual logging, and my managers had requested an oscilloscope photo of the current waveform's peaks. I rolled out our company's cart-mounted DSO (dig-

ital-storage oscilloscope), inserted a low-value resistor in series with the product's positive-power-supply input, and attempted to make a differential-voltage measurement (Channel A minus Channel B) across the current-sampling resistor.

Unfortunately, RF noise from a local FM-broadcast station swamped the small-load-induced fluctuations in the voltage developed across the sampling resistor, and increasing its resistance

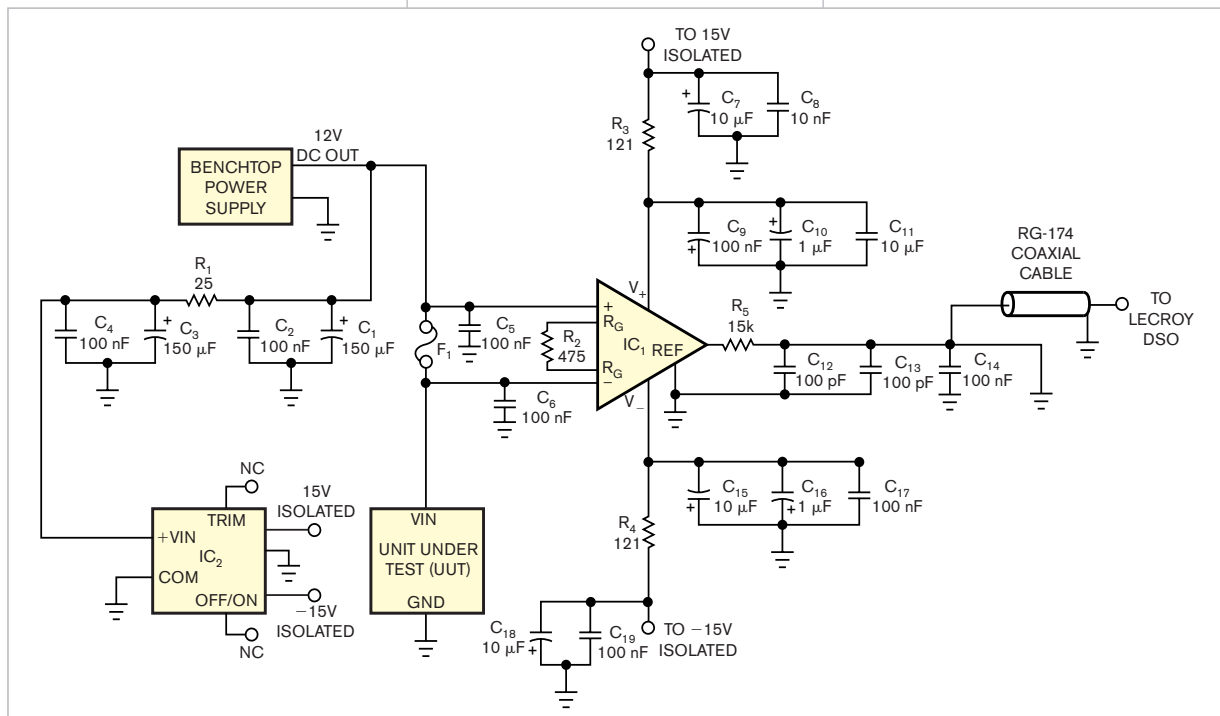


Figure 1 Improve your oscilloscope's performance in high-RF-noise environments by adding an instrumentation-amplifier front end. For best results, package the circuitry in a metal enclosure.

introduced an unwanted voltage drop on the product's power-supply rail. Finally, the 12V supply rail introduced a voltage offset that limited the oscilloscope's ability to accurately resolve the small differential signal that I was attempting to measure. I disconnected the oscilloscope's ac ground to "float" the scope with respect to the sampling resistor, but the RF noise visible on the trace increased significantly. I briefly considered using an older analog (non-storage) scope, but the DSO's storage feature would allow me to capture and print the waveforms required for my report.

In frustration, I scoured the workbench for stray parts and assembled a circuit that solved the problem. By chance, the parts collection included an instrumentation amplifier, IC₁, which does an excellent job of extract-

ing small signals from high-frequency background noise. The amplifier's inherently slow response attenuates RF noise but doesn't affect amplification of lower frequency signals. Adding RC lowpass filters to the amplifier's inputs and output further attenuates lower frequency noise induced by nearby switched-mode power supplies and digital logic or microprocessors.

Normally, I avoid using noise-emitting dc/dc converters as power supplies for analog circuits. However, in this case, IC₂, a dc/dc converter, provided an expedient and technically sound approach (Figure 1). In general, dc/dc converters produce more noise as their load currents increase, but, in this circuit, the sole load comprises the instrumentation amplifier that draws only a few milliamperes. Adding a few filtering components

provided additional noise suppression.

Under normal operation, the current that the product draws fluctuates from approximately 300 to 800 mA. To minimize the voltage drop induced in the power-supply loop, I used a 5×20-mm, 10A, 250V fuse, F₁, as a current-sampling resistor. Voltage drop across the fuse is approximately 1 mV per 100 mA of current, and operating the fuse at a small fraction of its nominal rating avoids introducing nonlinearities in the measurement.

With a 475Ω gain-setting resistor, R₂, the instrumentation amplifier, an Analog Devices (www.analog.com) AD620, provides a gain of 105V/V and delivers an output of approximately 1V, which corresponds to 1A of current flowing through the shunt. Capacitors C₁₂ and C₁₃ provide low-impedance paths for high-frequency noise. EDN

Virtual instrument determines magnetic core's B-H-loop characteristics

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To design an inductive component that contains a magnetic-core material, an engineer must accurately measure the material's characteristics. A magnetic core's dynamic hysteresis loop, or "B-H curve," contains valuable information about core losses and other magnetic parameters. Unfortunately, commercially available magnetic-loop-analysis instruments are expensive and thus impractical for small-scale research labs and manufacturers. This Design Idea describes a virtual instrument that uses a desktop or notebook computer with an analog data-acquisition card and National Instruments' (www.ni.com) LabView software (Version 7.1 or above). In operation, the software extracts B-H-loop information, core losses, and other magnetic parameters at a reasonable cost per measurement.

Figure 1 shows the test fixture for a magnetic-core-based device. The device, T₁, comprises a sample of core material and two windings with equal

numbers of turns. A precision current-sensing resistor, R₁, samples the excitation current that induces a magnetic field in the core. The voltage drop across R₁ is proportional to the excitation current and the magnetic field, H. A network comprising resistor R₂ and capacitor C₁ integrates the voltage induced in the secondary winding. The voltage across C₁ is directly proportional to the flux density, B, in the core. In practice, R₂'s value should be much larger than capacitor C₁'s impedance at the operating frequency. (Textbook

descriptions of the circuit suggest a ratio of 100-to-1.)

Components' tolerances and characteristics affect measurement accuracy. Use a noninductive, 1Ω, 1%-tolerance resistor of appropriate wattage rating for R₁, and select a low-leakage, low-dielectric-absorption, polyester- or polypropylene-film capacitor with tight tolerance for C₁. To acquire and view the data, you can use a dedicated virtual instrument using a National Instruments PCI-6024E data-acquisition card and LabView. The software features NI's Express VI (virtual-instrument) technology that greatly simplifies the creation of user-designed data-acquisition and -manipulation features. This application uses only two

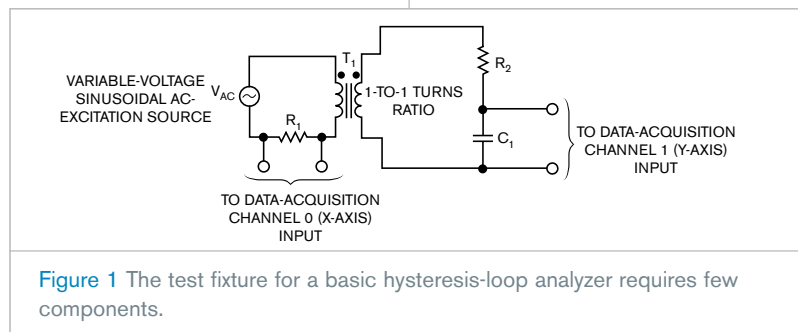


Figure 1 The test fixture for a basic hysteresis-loop analyzer requires few components.

data-acquisition analog-input channels: Channel 0 acquires magnetic-field readings (H) for display on an x-y chart's x axis in units of ampere-turns per meter, and Channel 1 captures flux density (B) in tesla units for the y-axis display.

At low frequencies, the core's hysteresis losses predominate, whereas eddy-current losses become more apparent at higher frequencies. A wattmeter-style algorithm calculates core losses, but you can easily substitute your own mathematical expression into the VI block diagram's formula node. LabView also can save the data and export results in Microsoft's (www.microsoft.com) Excel-spreadsheet format or into other programs for further analysis.

You can use another of the data-acquisition card's eight differential analog-input channels to determine inductance. To do so, measure the voltage across the device's primary winding and calculate its rms value. The ratio of the voltage to the rms current as measured through R_1 determines the magnitude of the winding's scalar impedance, X_L . Then, you can calculate the inductance from the following equation: $L = X_L / 2\pi f$, where f denotes

the frequency of the applied excitation voltage.

Figure 2 shows a hysteresis curve for a 3B7-mixture ferrite-pot core prepared with 100-turn primary and secondary windings and measured at 60 Hz. For comparison, **Figure 3** displays the 60-Hz hysteresis curve for a 100W power transformer wound on a toroidal core composed of grain-oriented steel. The toroidal core's wider loop indicates greater hysteresis, a characteristic that saturable-core power inverters exploit. To apply 60-Hz excitation, you can drive the device's primary winding from a stepdown (isolation) transformer powered by an adjustable-output auto-transformer, such as a GenRad (www.ietlabs.com) Variac. While observing the B-H curve display, gradually increase the primary voltage until the flattening of the hysteresis loop's upper and lower portions indicates core saturation. No calibration is necessary if you use precision. However, when evaluating core materials, you may need to experiment with different numbers of turns to obtain the windings' ampere-turns value for optimum results.

For tests at 60 Hz, use a 267-k Ω , 1%-tolerance resistor for R_2 and a 1- μ F polyester-dielectric capacitor for C_1 in

the integrator network. Depending on the number of turns and the current necessary to obtain a usable output voltage, a few volts of ac excitation is usually sufficient to run the test. For core measurements at higher frequencies, use a signal generator connected to a power amplifier and alter the RC integrator's component values for proper operation at the frequency of interest. Although the application does not use an analog output from the data-acquisition card, this output can serve as a sinusoidal-signal source for the power amplifier.

Review the electrical specifications of the card you plan to use and avoid exceeding the card's peak-to-peak differential- and common-mode input voltages. If the excitation voltage approaches or exceeds the card's ratings, add a 10-to-1 resistive-voltage divider to limit the applied voltage and compensate for the attenuator's losses by adding a factor-of-10 gain multiplier in the software.

You can download a copy of the VI that this Design Idea describes from www.circuitmentor.com/services.htm. You can also obtain a trial version of LabView from NI's Web site at www.ni.com. **EDN**

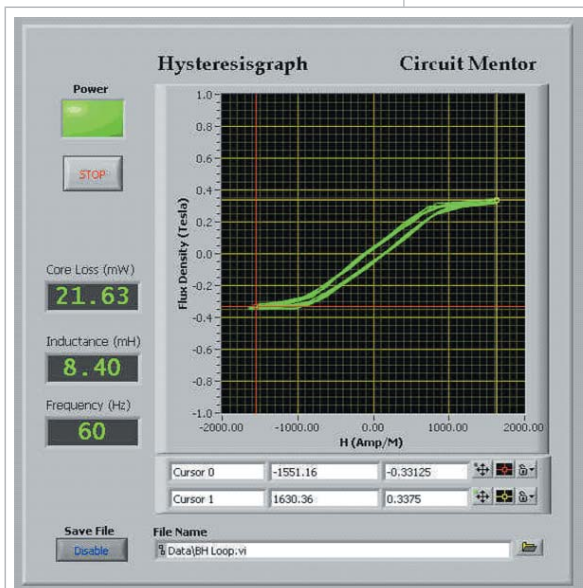


Figure 2 The virtual instrument's display shows a 3B7-mixture ferrite-pot core's B-H loop.

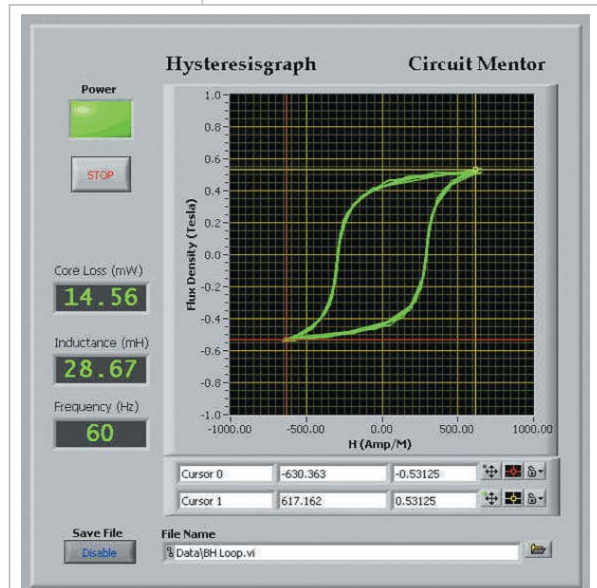


Figure 3 This grain-oriented-steel toroidal core's B-H loop exhibits saturation at a lower excitation value than the core in Figure 2.