

CO-DESIGN

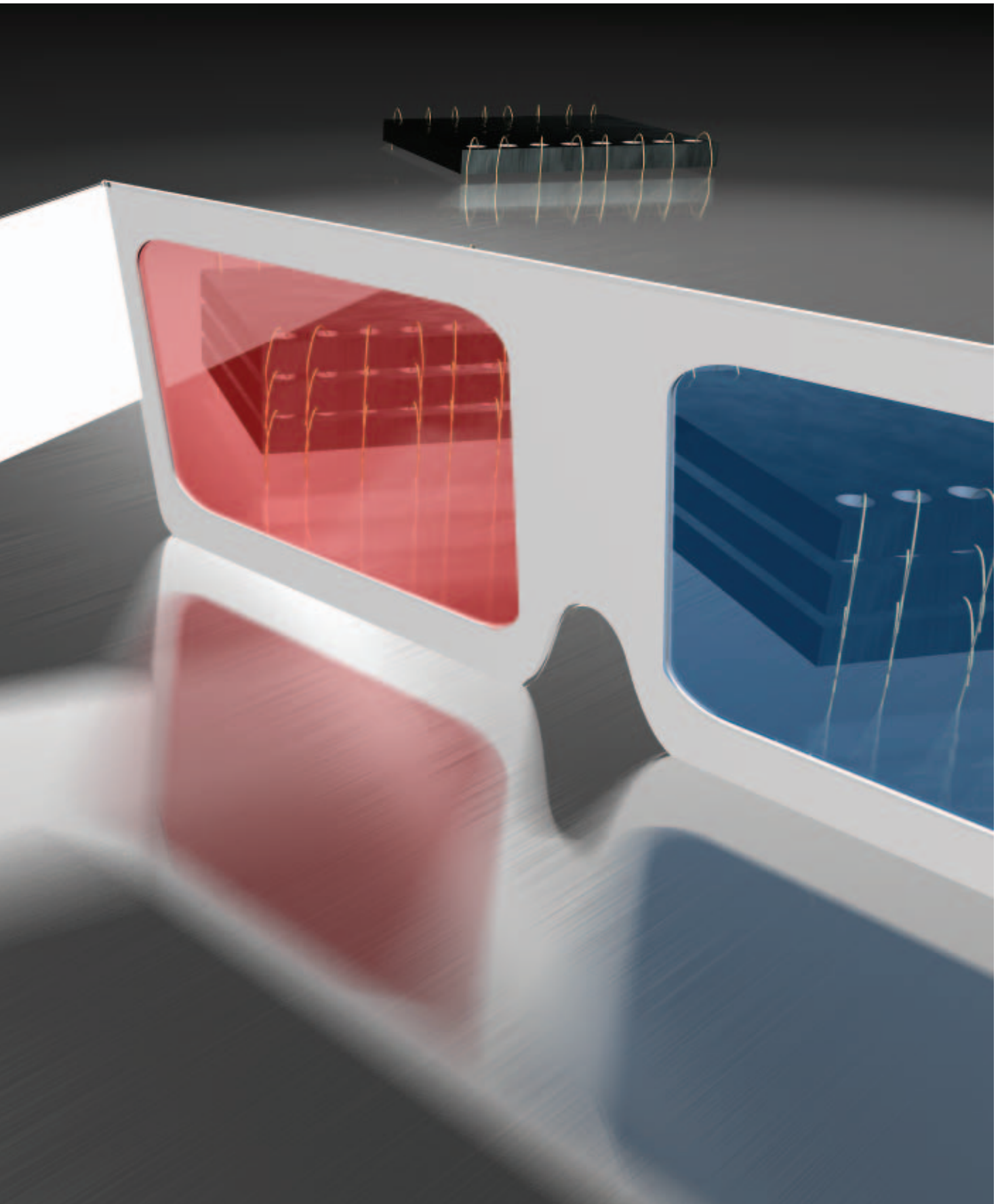
EDA VENDORS ARE HELPING IC AND PACKAGE DESIGNERS MORE EFFECTIVELY WORK TOGETHER.

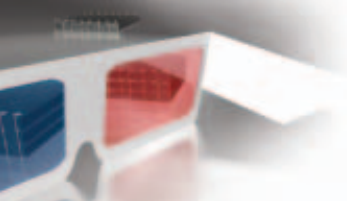
Traditionally, separate groups designed ICs and packages, but cost, time-to-market issues, and ever-growing package complexity—especially as SIPs (systems in packages), multichip modules, and stacked die become more common—are now forcing IC and package designers to work together more closely. Luckily, a few EDA players, such as Cadence Design Systems, Synopsys, Magma Design Automation, Ansoft Corp, EEsof, Optimal Technology, and Rio Design Automation are now making concerted efforts to develop tools to help IC designers and package designers collaborate more effectively.

THE TRADITIONAL FLOW BREAKS DOWN

A decade ago, IC-design teams would create the IC design and, during the place-and-route phase of the process, pull up an Excel spreadsheet to outline the I/O-ball or -pin requirements and assignments. They would then throw the spreadsheet over the wall to the package-design group. Package designers would use mechanical CAD tools, such as AutoCAD or proprietary tools, to create the package based on that specification and later adjust the system as test silicon became available.







AT A GLANCE

▣ A decade ago, designers developed packages mainly with mechanical CAD tools.

▣ Early EDA-package-design tools were warmed-over pc-board-design tools.

▣ TSMC's reference flow 5.0 demanded that vendors offer IC-package co-design tools for 90-nm designs.

▣ SIPs (systems in packages) are becoming alternatives to SOCs (systems on chips) and are especially popular with companies addressing fast-moving markets.

▣ EDA vendors are watching SIP progress to determine whether an opportunity to develop specialized SIP-design tools exists.

Groups usually indicated to each other that changes were necessary by reworking the numbers on the spreadsheet.

The process wasn't the smoothest, but it wasn't too painful. However, as transistor counts and I/O increased, working from a spreadsheet became impractical. Additionally, many of today's designs incorporate high-speed RF and use serial interconnect instead of parallel buses, which means that designers have to deal with blistering signal speeds and thus signal-integrity, power, and thermal issues requiring more thorough circuit and EM

(electromagnetic)-simulation and analysis among the IC, package, and pc board.

To better deal with these emerging issues, many companies started employing signal-integrity specialists, responsible for analyzing signals through the die, package, and board. Traditionally, companies have hired one or a few of these signal-integrity gurus to work across several design groups. These experts typically use 3-D field solvers, EM simulation, and pc-board signal-integrity tools to trace signals across the IC, package, and board.

To further sidestep some of these nasty effects, package designers adopted more advanced package materials, including moving from wire-bond to flip-chip packaging and even employing fan- or liquid-cooled packages. Of course, increasing the complexity of the package also increases its cost. Some analysts suggest that the package can have a higher per-unit cost than the die itself. Even conventional packages are growing in complexity, but that complexity jumps exponentially with designs that employ SIPs.

Despite the popular belief that a SIP is a poor man's SOC, SIPs are becoming useful in certain niches and popular with vendors addressing fast-moving markets and designers who simply don't want to deal with mixing technologies, such as analog and digital, on a single die. Flash-vendor M-Systems is a good example of a vendor that migrated from an SOC architecture to an SIP (see sidebar "M isn't for 'monolithic' at M-Systems"). But implementing an SIP or even an advanced single-die package and its extra design challenges, especially in extraction

and analysis, increases the necessity for IC and package designers to collaborate more closely (see sidebar "A tale of two methodologies").

Jaime Metcalfe, vice president of SIP marketing in Cadence's Allegro systems division, says the old throw-the-die-over-the-wall method doesn't work any longer, even in engagements with packaging-design companies. In fact, he says, it is becoming more common for customers to demand that IC designers and ASIC houses design to specific pinout configurations, so that the design will fit into the pc board. This situation holds especially true in the mobile-handset market. "The pc board is a major cost component of a cell phone," says Metcalfe. "By getting the pins optimized, cell-phone manufacturers are able to meet performance goals and reduce layers in the pc board. That [approach] cuts cost."

EVOLUTION OF TOOLS

EDA vendors have attacked IC and package co-design from two directions: upstream with IC-optimization tools and downstream with pc-board-systems tools. The industry's first step toward bringing together IC design and package design with an IC-centric approach occurred when vendors started integrating I/O-pinout-assignment software into IC-physical-implementation tools. Doing so, says Keith Felton, SIP-product-marketing-group director for the Allegro group at Cadence, eliminated the manual task of creating assignments in a spreadsheet.

"It is especially important with designs that have high-speed signals like

"M" ISN'T FOR "MONOLITHIC" AT M-SYSTEMS

When M-Systems many years ago introduced its MDOC (monolithic-disk-on-chip) hybrid boot-from-NAND device, a single die integrated the NAND core and NAND controller and software functions in an SOC (system on chip). Ariel Mashkovitz, vice president of the M-Systems

Mobile Division, says that M-Systems quickly found out that it is impractical to develop a new SOC for every NAND and NAND density, especially as NAND suppliers rapidly increase density grades in what has become a hot market.

Therefore, M-Systems went to an SIP (system-

in-package) model, which maintains the controller and related software on one IC and the NAND on another. The company can adjust the software in the controller to pair it up with a variety of NAND devices from disparate vendors and densities in a single package. This ability means

that M-Systems can quickly swap out a lower bit NAND if a higher density NAND emerges during a customer's product development. Today, the SIP model is such a force at M-Systems that the company renamed the product as "mobile," rather than "monolithic," disk on chip.



SERDES [serializers/deserializers],” says Felton. “You don’t want to end up putting so much skew in the die that it is impossible to rectify it in the package.”

IC-floorplanning tools from Cadence, Synopsys, and Magma have for a few years had I/O-pinout-assignment features, but Felton says that traditional floorplanning tools don’t go far enough, because they have only a rudimentary view of the package.

EDA vendors have also attacked the problem from the pc-board-fabric side. In the mid-1990s, Cadence created a variant of its pc-board tools for package designers. That tool, Advance Package Designer and, shortly after, tools from Avanti (which Synopsys has since acquired) brought commercial electrical design and analysis to package designers. Those tools had schematic entry and layout and autorouting for packages but lacked a useful link to IC design and even a link to simulation and analysis. Cadence and a growing field of players over the last three years have made even more significant strides in IC and package-co-design technology.

THE NEW GENERATION

An-Yu Kuo, chief technology officer at Optimal Corp, says that EDA-industry efforts to develop IC- and package-co-design tools sped up in 2004, when TSMC (Taiwan Semiconductor Manufacturing Co) issued its reference flow 5.0, which highlighted the need for an IC- and package-co-design flow (Reference 1). “Today, there are still no cohesive co-design tools, and, in the past, IC and package design were isolated islands,” says Kuo. “Three years ago, TSMC recognized the importance of IC and package co-design for nanometer flows, and the industry has since responded. The EDA industry has made great progress, but we’re not all the way there yet.”

Cadence, largely because it already had many of the point tools in the market, was the first to piece together a flow (Figure 1), and most package-design point-tool vendors tailor tools to fit the Cadence package-design flow. A year ago, Cadence enhanced its co-design offerings by releasing package- and pc-board-co-design capabilities with Allegro Package SI (signal-integrity) 620. That tool adds Opti-

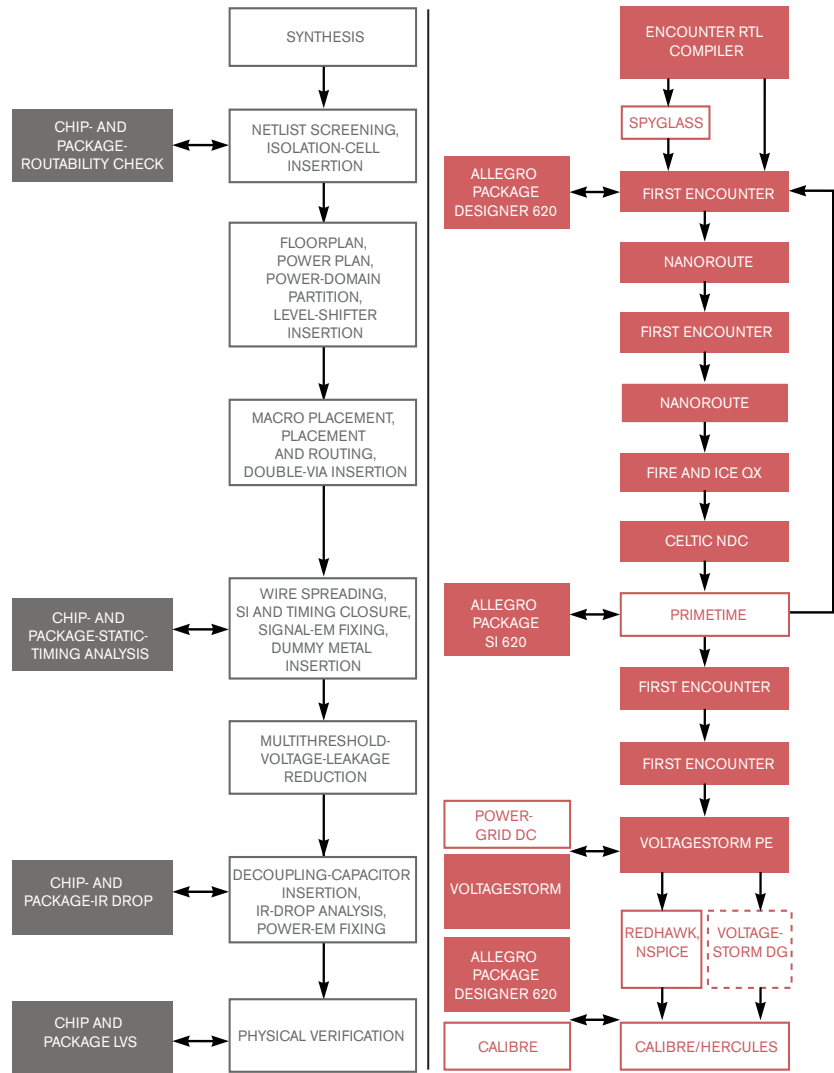


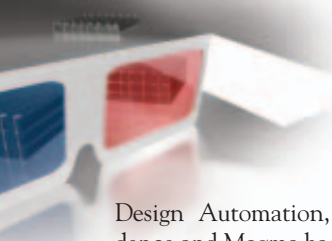
Figure 1 Cadence—an early innovator in package design, as well as in pc-board- and IC-design tools—has been able to respond to TSMC’s request for an IC- and package-co-design-tool flow.

mal Corp’s 3-D field-solver engine to the Allegro Package SI simulator. The 620 tool reads and writes package designs produced and designed by Allegro Package Designer as well as pc-board designs created with the Allegro pc-board-layout tool. It allows users to make trade-offs between their board layout and electrical effects.

“We wanted to help users analyze the electrical pathway from the die all the way through to the pc board and optimize to the final mask the quality level of the package substrate as well as the pc-board substrate,” says Felton.

Synopsys, too, has stepped up its efforts. The company gained the Xynetix package-design tool in its 2001 acquisition of Avanti, but, in September 2005, Synopsys took a step toward further automating the flow with JupiterIO. The tool is a concurrent die- and package-I/O-planning tool that includes I/O and bump placement, RDL (redistribution-layer) routing, and some package-route planning, as well. It accesses IC data through the Milkyway database and packaging data through standard interfaces.

The IC- and package-co-design market even has a start-up. By press time, Rio



Design Automation, which both Cadence and Magma back, will have introduced RioMagic. Like JupiterIO, the tool allows users to design the IC and package concurrently instead of sequentially (Figure 2). Kaushik Sheth, Rio's chief executive officer, says that the flow allows IC designers to make "packaging-aware" adjustments to their IC designs, and if changes in the board or packaging are required, the IC design can instantly reflect those changes. In the RioMagic flow, users build and work from a single golden I/O data model at the IC-floor-planning stage that the rest of the flow accesses through Si2's OpenAccess.

Joel McGrath, vice president of marketing at Rio, says that RioMagic analyzes

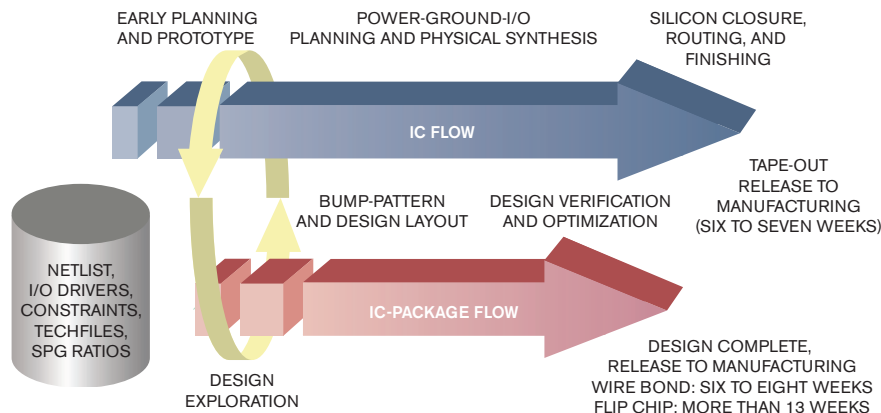


Figure 2 With Rio Design Automation's RioMagic, designers work from the same model and design ICs and packages concurrently, instead of sequentially.

A TALE OF TWO METHODOLOGIES

IC- and package-design challenges commonly confront today's ASIC vendors. LSI Logic and NEC run into similar problems regarding co-design but attack them using slightly different methods and tools.

LSI Logic uses an integrated team to ensure that designers take packaging concerns into account at the beginning of the process. Yogi Ranade, marketing manager at LSI Logic, says that a design team at LSI typically includes ASIC designers, a die and package signal-integrity specialist, a package designer/layout specialist, and a systems/methodology engineer. "They all talk upfront and do quick what-if scenarios," says Ranade. "Since they talk different languages, they use different tools."

Ranade says that, at LSI, a signal-integrity engineer typically uses Ansoft's Turbo Package Analyzer or an Optimal Technology 3-D

field solver. The package designer uses an APD (application-parameter-descriptor) tool from Cadence, and IC-design engineers use the usual ASIC tools.

Ranade says that, although current-generation commercial tools support standard formats and thus teams can transfer files back and forth, the cross-discipline design and analysis flow needs improvement.

"What would be neat is if in the packaging environment you could do a quick-turn, what-if signal-integrity analysis that would tell you that nicking down a trace would cause a discontinuity," says Ranade. "It would allow you to create better signal-integrity limits for the IC design. That what-if analysis doesn't happen as quickly as we'd like to see it."

Ranade says that anything that could help system-level engineers share

their pains with IC and package engineers would help further improve the methodology. "Today, on the silicon side, we have redistribution layers on top of the silicon where we route out to the wire-bond pads," says Ranade. "We are doing a lumped analysis in this area, but we think that EDA tools could help us more effectively route to wire-bond pads."

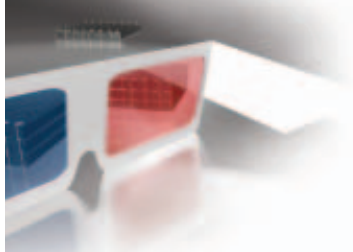
Han Park, a senior engineering manager at NEC Electronics America, says that NEC has a specialized packaging-design group that works closely with IC designers. Because the EDA industry has been slow to develop a tool flow, the group has developed its own design software and methodology.

"A couple of years ago, we found that you just can't design the package by itself any longer," says Park. "You really have to consider the silicon and the package together!"

Park notes that, with an early understanding of package problems, IC designers can place functions on their layout so problems don't occur during packaging. And if packaging designers know about silicon problems early, they can add functions or shielding, such as decoupling capacitors, to problem areas on the package.

The NEC tool incorporates RLC extraction, as well as signal- and power-integrity analysis. It currently supports flip-chip packaging, but company tool architects are developing a version for wire-bond design for deployment early this year.

Park doesn't believe NEC will offer the tool commercially, but he says that the company is constantly evaluating commercial offerings and would move to one if the EDA industry were to offer a flow superior to NEC's.



the signal integrity of I/O signals and the power integrity of the chip package. To do so, RioMagic builds electrical models that capture on-chip as well as package parasitics. To build the on-chip part of the model, RioMagic precharacterizes on-chip interconnects and stores them in look-up tables.

For the package part of the electrical model, RioMagic extracts the RLC and K and builds a detailed PEEC (partial-equivalent-electrical-circuit) model of the package. This PEEC model captures the entire package without incurring the cost of running a field solver. The tool also generates a simulation deck with primary drivers, drivers for coupled nets, a

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coupled-net parasitic network, and a pc-board-loading termination for each net. The tool analyzes this network and then calculates the response for the primary net switching and any coupling effects from adjacent nets.

RioMagic includes a synthesis engine that uses this model to help users assign I/O and immediately see whether it has an impact on the IC floorplan. When users move hard cores, which have fixed I/O, in their floorplan, RioMagic automatically resynthesizes the rest of the I/O conforming to the model.

RioMagic works from standard formats. The tool uses DEF (design-exchange format) for chip netlist data, IP (intellectual-property) libraries for I/O, standard-cell and hard macros in LEF (layout-exchange format), and I/O-driver models in IBIS (I/O-buffer-information specification).

More advanced designs, especially those employing SIPs as well as mixed

analog and digital or high-speed RF ICs, require more detailed extraction, EM analysis, and thermal analysis and simulation. Some research is even looking at incorporating antennas in SIPs. Luckily, many of the tried and true vendors, such as Ansoft, EEsos, Cadence, Synopsys, Flomerics, and Optimal, offer tools for leading-edge applications.

An SIP, for example, often incorporates a mixture of analog and digital ICs, usually side by side rather than stacked, to ensure shielding. In a two-IC SIP, designers need to perform parasitic extraction and signal- and power-integrity analysis individually on both device die and packages. Designers then have to analyze the SIP as a single unit in the context of the entire system.

The analysis can become even more complex if the die are stacked in wire bond or if the designs incorporate RF blocks with high-speed signals, which are susceptible to interference from the digital blocks. The amount of data extracted can be unwieldy, often forcing users to employ model-based techniques.

Both EEsos and Ansoft offer 2-D planar and 3-D EM simulators. Although RF tools typically evolve at a snail's pace, Ansoft recently introduced the Nexxim circuit simulator, which noted Massachusetts Institute of Technology professor Jacob White developed, to complement the company's flagship HFSS (high-frequency structured simulator). Nexxim uses the same circuit netlist and library models for transient and harmonic-balance analyses. Larry Williams, director of marketing at Ansoft, says that

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the tool offers increased runtimes, making it practical for use in IC, package, and pc-board design with a mixture of models. With this approach, designers need not reconcile differences between running analyses on different simulators, each running from separate netlists and device models.

“There are the challenges we’ve always

had for creating a model for electromagnetic, with extracting it so it is accessible to the design engineer,” says Williams. “But, once you have that model, what do you do with it in your circuit simulator? If you use a traditional parasitic extractor on chip, for example, you rapidly overwhelm your circuit simulator. Most folks say go to a fast Spice simulator, but often

you are making oversimplifications for the active devices. What is needed is a better circuit simulator. That’s why [Ansoft] developed Nexxim.”

Ansoft also offers the Turbo Package Analyzer, a package-modeling tool that employs boundary-element methods for high-pin-count BGA packaging.

Agilent’s EEs of group also offers Momentum, an advanced 3-D planar EM tool. The company recently released a 64-bit version of the tool to deal with the capacity issues that field solvers present.

Thanks largely to TSMC’s putting IC and package co-design on its reference flow for 90-nm design, the EDA industry is starting to ramp up its efforts in IC and package co-design. Although EDA companies are stepping up their game, they are far from conquering all the challenges in this area. Most vendors admit that, if SIP continues its growth, a greater need will emerge for IC integration and perhaps opportunities for EDA vendors to develop a subflow for SIP designs. It remains to be seen, however, which design group is responsible for the SIP: the IC-design group, the package-design group, or the system-design group. Perhaps SIP design will become so complex that it will require a new, specialized designer or design team. We’ll see. **EDN**

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