

The economics of structured- and standard-cell-ASIC designs

STRUCTURED ASICs OFFER COST AND PERFORMANCE THAT FALL BETWEEN FPGAs AND TRADITIONAL STANDARD-CELL ASICs. BUT THEIR INTRODUCTION HAS COMPLICATED THE CHOICE OF THE RIGHT SILICON.

Although structured ASICs promise a shorter schedule than standard-cell ASICs, this abbreviation comes at a price. Structured ASICs are more expensive on a per-unit basis, allow less customization, and offer lower performance than standard-cell ASICs. For various designs, customers often have to choose from standard-cell ASICs, structured ASICs, and FPGAs.

To select the right ASIC, you could use a three-step approach. The first step would be to look at the technical requirements and feasibility of the design for structured-ASIC and standard-cell-ASIC technologies. Next, you would perform a financial analysis. Finally, you would employ a financial model that looks at the total time value of money and the NPV (net present value) of the ASIC project.

BASIC ASIC PRICING

ASIC pricing is usually complex and depends strongly on the customer's projected volume. However, the fundamental cost aspects of an ASIC design do not change. You can break up the cost of any ASIC into two basic components: a fixed NRE (non-recurring-engineering) charge and unit pricing. ASIC vendors charge a fixed NRE to cover the expenses they incur for physical design—from handoff to tape-out. NRE charges include costs for IP (intellectual property), masks, package design, test development, debugging, and hardware. The design-engineering costs include engineering efforts, EDA tools, and hardware. The IP-licensing fee is a one-time cost you pay to the IP vendor for third-party IP. Some companies pass these charges on to their customers. In the case of FPGAs and structured ASICs, manufacturers do not customize the package, test cost, and die for each project; thus, they achieve a lower NRE cost but may require a trade-off in flexibility.

Meanwhile, the industry bases unit pricing or cost on volume shipments. Die size, packaging type, per-part royalty, and testing costs incurred on every part primarily drive unit cost. For standard-cell ASICs, the components of chip COG (cost of goods) may be transparent to the fabless-chip customer or the system house; manufacturers base the pricing of FPGAs and structured ASICs on the value of the parts.

Unit cost varies with the number of parts that customers order, and silicon vendors commonly offer volume discounts. Larger orders reduce the percentage of overhead in the chip cost per unit, which allows fabless-chip customers or system houses to

get reduced pricing for volume purchases. Additionally, unit cost may improve over time due to improved manufacturing efficiencies, yield enhancements, and better yield management.

Developing an ASIC from its architectural specifications breaks into three steps: architecture to RTL or netlist, RTL or netlist to tape-out, and tape-out to volume production or RTP (release to production, **Figure 1**). Development of the chip architecture and the associated RTL or netlist is primarily the ASIC customer's responsibility. ASIC vendors normally do not take ownership for developing the architecture or associated RTL of a design. The ASIC vendor takes either the RTL or a netlist as the customer deliverable and is responsible for producing the prototypes, testing the prototypes, and characterizing and qualifying the product for volume production. The ASIC vendor then delivers tested working parts to the customer.

ARCHITECTURE TO RTL OR NETLIST

Customers often provide RTL or a netlist to the ASIC vendor. Converting architectural specifications into RTL or a netlist primarily involves defining the microarchitecture, writing RTL code, developing a functional verification for the RTL description, and synthesizing the gate-level netlist. The schedule for this process varies with design complexity and can range from months to more than a year. More than 60% of this time involves functional verification. For complex SOC (system-on-chip) designs, functional verification can consume more than 70% of the total design schedule.

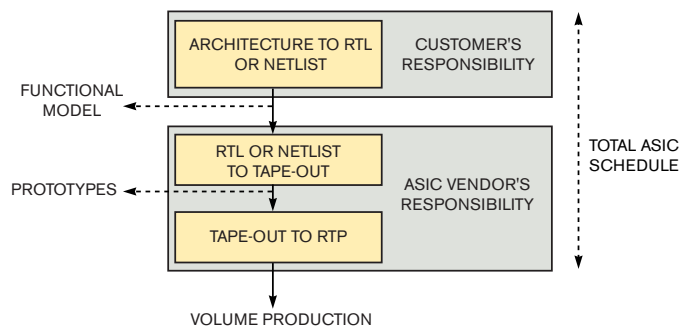


Figure 1 The development of an ASIC from its architectural specifications breaks down into three distinct steps.

RTL or netlist to tape-out constitutes the physical-design process. This process comprises synthesis, DFT (design for test), floorplanning, timing analysis, clock insertion, place and route, timing closure, reliability analysis, and physical-design verification. For FPGAs and structured ASICs, in which manufacturers lay out cells with built-in DFT, physical design implies routing the top metal layers, reliability analysis, and timing closure, which results in less time for physical design. A chip from a standard-cell implementation typically has better performance and a smaller die for the same level of complexity than an FPGA or a structured-ASIC implementation.

Once you tape out a design for a standard-cell ASIC, it takes about four to eight weeks to process a more-than-30-layer design and provide prototypes to the customer. For structured ASICs, the base wafer is processed; therefore, only the upper-level-metal and via layers require processing. Using a structured ASIC results in substantial time savings, with parts available for delivery in just a few weeks. After initial prototypes are available, they must undergo the RTP phase, requiring testing, qualification, and characterization, and designers must analyze and optimize the production process for maximum yield before the part enters full production.

The time it takes for a prototype to begin volume production varies from 12 to 26 weeks for a standard-cell ASIC. Structured ASICs require about six to eight weeks, because they need no detailed characterization, process qualification, and yield optimization. In parallel with the ASIC-RTP process, the customer must perform functional verification and develop and verify the software that will run on the silicon. This process may take longer than the RTP approach and could delay the volume-production shipment of parts.

In production, the time it takes to fill a customer's order is typically the same for standard-cell ASICs and structured ASICs for the same number of process layers, because the wafers require processing from scratch, and they also require packaging and testing. Therefore, neither process offers a great advantage over the other.

A NOTE ABOUT NPV

You calculate NPV (net present value) by discounting all the cash outflows at the hurdle rate of the customer's company. Companies internally set the hurdle rate, and it can vary substantially from project to project, depending on risk factors and prevailing interest rates.

in a minimum area, which results in a smaller die and, hence, a lower unit cost.

Going to a standard-cell ASIC can impact a schedule for as long as 18 months. The financial analysis accounts for the lost sales during this period as "lost-opportunity costs." The longer time is mainly due to the need for the detailed layout design,

COST STRUCTURE

Manufacturers custom-design each ASIC program for standard-cell ASICs, and the NRE charges are usually higher than for a structured ASIC or an FPGA. Custom design implies that every chip goes through physical design of all metal layers. This approach is time-consuming, and it results in longer schedules and higher costs for the engineering efforts and tools. The layout of the logic cells provides maximum performance

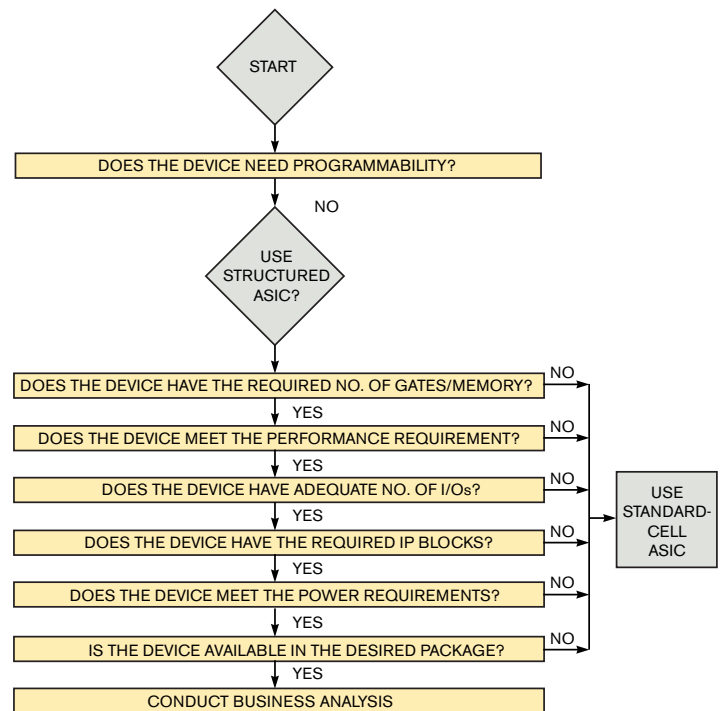


Figure 2 You can systematically carry out the technical feasibility of implementing the design in a standard-cell or structured ASIC by carefully identifying the needs and mapping those needs to the appropriate ASIC option.

complete manufacturing processes, and release to production.

The biggest advantage of standard-cell ASICs is that they offer the lowest unit cost, because their custom design results in a smaller die. Better package selection and testing also lower the unit cost. In a high-volume market, cost savings on a per-unit basis lead to significant market advantages. Additionally, you can use smaller packages and similarly sized structured ASICs, resulting in smaller pc-board form factors. Furthermore, customers get added flexibility and higher performance from both speed and power perspectives.

The lower unit cost compensates for the overall higher upfront NRE costs and the impact on the schedule. Therefore, you need to consider the total cost of the project over the life span of the ASIC. NRE cost with a structured ASIC is usually lower than with a standard-cell ASIC, mainly due to predesigned cell layout, fixed IP, standard packaging, and minimum routing at the top metal layers. Cell layout and cell-level routing are standard, so new designs require minimal effort. The manufacturing NRE cost is also lower, because the wafers are partially processed, and multiple customers share them. For a new design, only the top metal-layer masks require processing; hence, mask costs are lower. The packaging for each chip is standard, leading to economies of scale and reducing the package's NRE cost. The limitation of this platform, however, is that the design must fit the available prepackaged structured-ASIC IP, gates, and memory configurations.

Structured ASICs allow a quick turnaround from RTL to

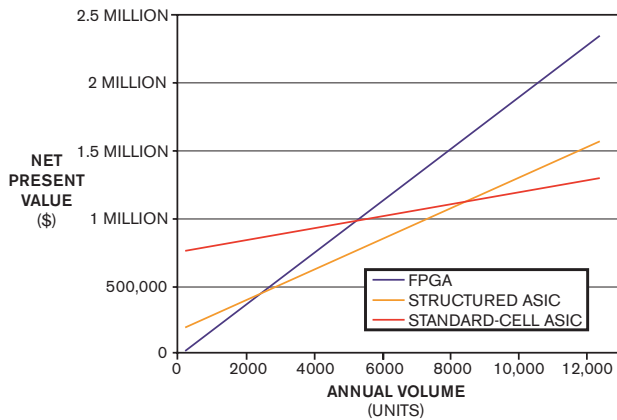


Figure 3 At volumes of less than 1500 parts per year, such as might be the case for an avionics-control chip, an FPGA may be your best bet.

parts. The physical-design-cycle time is low because only the top metal layers require routing, the package is standard, and the wafers are partially processed and stored as inventory. This approach allows a shorter turnaround time in both the design and the manufacturing phases.

Unit costs for a structured ASIC are higher than those for comparable standard-cell ASICs, primarily due to fixed-cell layout, which results in less cell usage, higher routing overheads, and increased use of silicon area for the design. A larger die directly impacts the unit cost. The use of suboptimal packaging further increases the unit cost. Generic packaging typically has a larger form factor and increases overall product and system costs. Test costs may also follow a similar cost increase over standard-cell ASICs.

Selecting the best silicon option for a given design is always a challenge. The best way to make this decision is to start with a technical-feasibility study to determine whether an FPGA, structured-ASIC, or standard-cell-ASIC platform meets the design requirements. If more than one silicon approach is technically feasible, a financial analysis can determine the optimal choice.

The best option is the one that offers the lowest cost or the highest returns. For a system manufacturer, the lowest cost for an ASIC is important because it is easy to determine and it directly affects the cost of the final product. You can attribute the highest returns from selling the final system to several factors, including market requirements, the ASIC platform, software, and market conditions. It often becomes difficult for a company that sells complete systems to gauge the returns from the ASIC.

TECHNICAL-FEASIBILITY STUDY

You can calculate the technical feasibility of implementing the design in a standard-cell or structured ASIC by carefully identifying the design needs and mapping those needs to the appropriate ASIC option (**Figure 2**). Often, a design needs complex IP, such as analog/mixed-signal blocks. Nonavailability of such IP may prevent the use of a structured ASIC. Alternatively, in some cases, the IP is available, but its performance is unacceptable for the design. For example, the CPU available in the structured ASIC may run at a maximum frequency of 250 MHz, even though the design calls for a CPU running at 400 MHz.

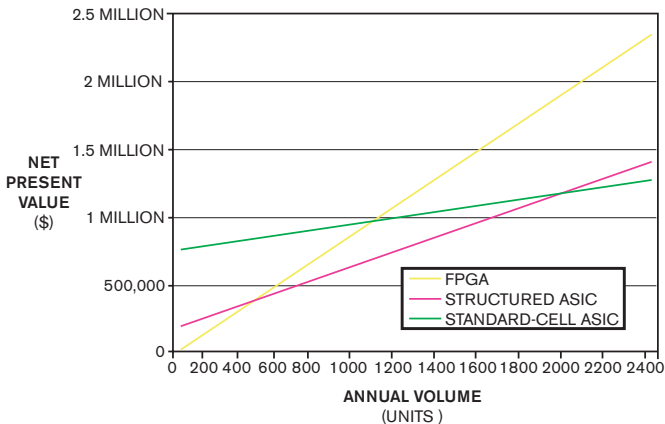


Figure 4 An NPV analysis shows that, even at volumes of 2200 parts per year, a standard-cell ASIC is the least costly alternative.

If the standard-cell ASIC is the only option available, then the decision is clear. Often, a combination of structured-ASIC and discrete components may also meet design requirements. Under such conditions, you must conduct a business analysis to identify the best option that offers the lowest cost.

BUSINESS ANALYSIS

If the design is feasible for an FPGA, structured ASIC, or standard-cell ASIC, then you should base your final decision on cost. You can do your financial analysis by calculating the NPV of all the options (see sidebar “A note about NPV”). The ASIC option with the lowest cost at the projected volume is your best choice. For NPV analysis, you must select a suitable discount rate.

The following case studies use a discount rate of 8.5% for NPV analysis. Varying the discount rate does not affect the final outcome of the analysis because the studies discount all the costs at a uniform rate. For a business analysis, you need to know the volume or number of ASICs needed per year, the projected life span of the ASIC, and the total NRE charges for that ASIC option.

The NRE figures in the case studies include only charges that projects incur after the netlist stage and before the initial prototypes. NRE charges you incur during architecture and RTL design are common for all types of ASICs; therefore, this comparative analysis does not take them into account. For the case studies, assume that you can implement the design in both a structured and a standard-cell ASIC. The goal of these studies is to determine the cost of all the possible ASIC options.

CASE STUDIES

In one case study, assume that an ASIC has 250,000 gates running at 200 MHz and requires implementation in a 250-pin BGA package. For a structured ASIC, the average NRE charges are \$200,000, and unit cost is around \$40. Standard-cell ASICs have an NRE cost of approximately \$800,000, and the unit cost is around \$12. For an FPGA, assume NRE costs of zero and unit costs of around \$80. Assume an ASIC life cycle of three to five years.

Conducting an NPV analysis for various volumes over a range of projected annual number of parts for five years gives you the total cost of the silicon option for each of the projected volumes. Because all the financial transactions in the procurement of the

ASIC are cash outflows, the numbers are positive for the NPV calculation. The analysis considers the ASIC option with the lowest NPV as the most suitable approach.

Table 1 on the Web version of this article at www.edn.com/ms4178 compares the total costs of FPGAs, structured ASICs, and standard-cell ASICs for the projected volume. **Figure 3** helps clarify the data in the **table** by depicting how the NPV of various ASIC options changes with volumes.

Figure 3 and **Table 1** show that, for volumes of less than 1500 parts per year, such as for an avionics-control chip—an FPGA may be your best bet. If the product has a demand of more than 2000 but less than 8500 parts per year, such as for a low-volume communication base station, a structured ASIC offers the lowest NPV and, hence, is the best option. If the annual demand increases to more than 8500 parts, a standard-cell ASIC is the right choice. In systems such as cell phones or LCD controllers, which have high annual volumes and are price-sensitive, a standard-cell ASIC is best.

You can run a similar analysis for ASICs with different unit costs and with different NRE charges, but the conclusion is the same. FPGAs are best for low volumes; at slightly higher volumes, structured ASICs offer the lowest cost; and at high volumes, a standard-cell ASIC is the ideal approach. Choosing an ASIC depends on having a good projection of the product's volume shipments and the unit cost of the ASIC.

In another case study, consider a complex system design with 5 million gates, 3 Mbits of internal memory, and a high-speed SERDES (serializer/deserializer) interface. Using a structured ASIC, the average NRE cost for such a chip is \$250,000, and unit cost is \$120. A standard-cell ASIC has an NRE cost of \$1 million and a unit cost of \$30. For an FPGA-based option using multiple FPGAs, the NRE cost is almost zero, and the total unit cost is around \$240.

Conducting an NPV analysis for the above case and plotting the NPV for various annual unit volumes for each option show that, even at volumes of 2200 parts per year, a standard-cell ASIC offers the least costly option (**Figure 4**). If you use the ASIC for enterprise routers or digital set-top boxes, which have large annual volumes, a standard-cell ASIC is the best approach. If the application of the ASIC is in industrial measuring or control devices, which have moderate or unpredictable volume shipments, a structured ASIC is a better choice.

These two examples show that, at higher design complexities, a standard-cell ASIC offers a less costly ASIC approach, even at lower volumes. The advantage of having a low unit cost outweighs the higher NRE costs associated with a standard-cell implementation. Both an FPGA and a structured ASIC may offer lower initial costs and shorter times to market at high overall costs.

In a third case study, a high-end ASIC may contain 12 million to 20 million gates and 10 to 20 Mbits of memory along with multiple SERDES interfaces and a high-speed DDR interface. You can implement this design in a 250- to 400-sq-mm die in a flip-chip package, but you cannot implement the same design in a single FPGA or structured ASIC. However, you can implement the entire design in multiple FPGAs or structured ASICs.

Assume that this ASIC costs about \$150 to \$320 per part with an NRE charge of approximately \$2 million to \$2.5 million. If you were to implement the same design in multiple structured ASICs, the NRE charges would be around \$750,000 with a unit

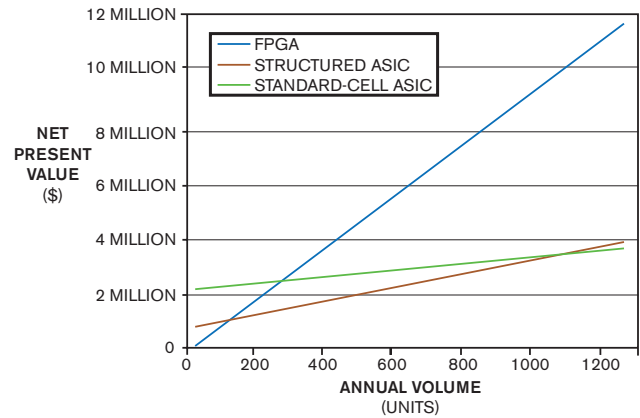


Figure 5 For high-end ASIC designs, a standard-cell ASIC makes economic sense only when volumes exceed 1200 per year.

cost of \$1000. You could implement the design with multiple FPGAs and other discrete chips; then, the total cost for each design would be approximately \$4000. A common industry perception is that, for high-end designs, standard-cell ASICs are expensive and need high volumes to justify their costs. NPV analyses bring out interesting results (**Figure 5** and also **Table 2** on the Web version of this article at www.edn.com/ms4178).

The NPV analysis clearly shows that, in the case of a high-end ASIC design, a standard-cell ASIC makes economic sense only when volumes exceed 1200 per year. At volumes lower than 1200, a structured ASIC may make economic sense. However, for annual volumes of less than 100, an FPGA is the best choice. Designers should implement high-end telecom devices, such as ISP (Internet-service-provider) routers, which have annual volumes of less than 100 units per year, in FPGAs or structured ASICs. On the other hand, if you expect the product to sell in large volumes, such as server chip sets, a standard-cell ASIC has the lowest cost.

Selecting an ASIC involves technical-feasibility and business analyses. Often, the technical-feasibility analysis can determine the type of ASIC. A structured ASIC has severe technical limitations compared with a standard-cell ASIC. If you can implement the design in both a structured ASIC and a standard-cell ASIC, you should perform an NPV analysis to determine the optimal ASIC. To conduct an NPV analysis, you need to know the NRE charges, unit cost, annual product volumes, and discount rate. The results show that, for a chip that you can technically design as a standard-cell ASIC or a structured ASIC, the application segment and the anticipated volume requirements primarily determine your choice. **EDN**

MORE AT EDN.COM

Go to www.edn.com/ms4178 and click on Feedback Loop to post a comment on this article.

AUTHOR'S BIOGRAPHY

Arun Kottolli is a technical solutions engineer at Open-Silicon (Sunnyvale, CA), where he is responsible for engineering-solutions management. He has a master's degree in electrical engineering from Texas A and M University (College Station, TX) and a master's degree in international management studies from University of Texas (Dallas).