



BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

## Scaling: a balanced view, part one

I've long maintained that, as long as semiconductor vendors use process descriptors to promote IC products, OEM designers need to know enough about those processes' capabilities to distinguish reasonable claims from hype (**Reference 1**). Leaving aside fond memories of IC processes that can support  $\pm 15$  and  $\pm 18$ V rails, analog IC designers began more than a decade ago to feel the pinch of process-imposed voltage scaling when the minimum feature size slipped below 700 nm and forced supply rails to do what was theretofore unthinkable: fall below 5V.

Since that time, claims about process scaling have all too often come down to the oversimplification, "good for digital, bad for analog." Although one cannot argue that scaling has been good for digital designers, the claim that it is bad for analog design depends upon certain assumptions that do not always hold. Additionally, many discussions about submicron and deep-submicron analog processes observe the effect that scaling has on parametric performance, whereas, in practice, performance is rarely a negotiable consequence of process selection. Instead, the application determines the minimum acceptable performance. So, the notion that scaling a process necessarily results in a degradation of, say, SNR, gains little traction if, to be competitive, a product must meet or exceed a specific minimum performance with respect to that parameter.

I mention this fact because Klaas Bult

of Broadcom Netherlands presented an insightful analysis on the effect of technology scaling on power dissipation in analog circuits at the ISSCC (International Solid State Circuits Conference) in February (**Reference 2**). The conference organizers have not yet widely distributed the work, so here begins a summary, which I will continue in the next installment of this column.

Bult observes that, within broad limits, "power can buy any performance"; as the *currency of the realm*, power dissipation thus appears in the denominator of a great many figures of merit. The key question, then, is: For a given level of performance, what effect does the voltage scaling have on power dissipation? The answer depends upon the performance parameters of interest. Using a single-transistor gain stage as the model minimum subcircuit, Bult observes, distortion, slew rate, settling, and bandwidth follow the bias current,

whereas matching, white noise, and  $1/f$  noise follow the load capacitance (**Figure 1**). The minimum subcircuit forms the basis of higher order subcircuits, such as differential pairs and gain cells with explicit feedback networks. From this scenario, Bult suggests an analysis that calculates the minimum dissipation that the subcircuit string requires to support a given level of performance with feature size as a parameter (**Figure 2**). Though the detailed analysis is not the sort of exercise OEM designers need to perform, an understanding of the concepts that the analysis draws upon can result in a clearer understanding of the implications that process scaling has on parameters of interest. The next installment of this column will continue with this thought. **EDN**

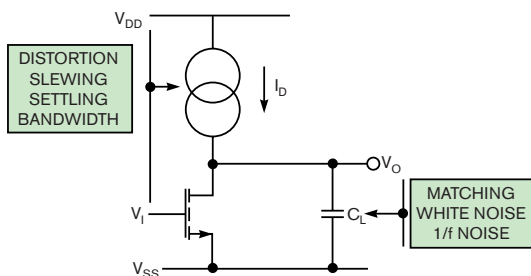
### REFERENCES

- 1 Israelsohn, Joshua, "Ripples in the process pool," *EDN*, Jan 24, 2002, pg 44, [www.edn.com/article/CA191157](http://www.edn.com/article/CA191157).
- 2 Bult, Klaas, "The effect of technology scaling on power dissipation in analog circuits," *ISSCC 2006*, Feb 5, 2006.

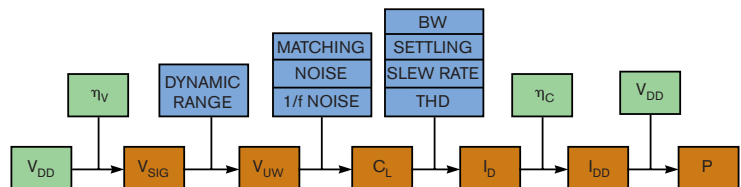
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**Figure 1** A single-transistor gain stage serves as Bult's model minimum subcircuit.



**Figure 2** Bult's analysis combines application requirements (blue) with terms that derive from the process scale (green) to generate calculated values (brown) resulting in a power estimate for the model subcircuit.