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CPLD automatically powers itself off

Rafael Camarota, Altera Corp, San Jose, CA

Most of today's CPLDs (complex programmable-logic devices) feature reduced-power operating modes, but, when the system is not in use, a complete shutdown that conserves battery power remains the ultimate power-reduction goal of many designers. **Figure 1** shows how you can add a few discrete components to a CPLD—in this example, an Altera EPM570-T100—to implement a battery-powered system's power-down circuit. An external P-channel MOSFET, Q_1, an International Rectifier (www.irf.com) IRLML6302 or equivalent, serves as a power-control switch for the CPLD, IC_1, and other components in the system. The CPLD and an array of switches control the MOSFET's gate, applying bias that switches on Q_1 whenever a user presses a switch. The CPLD includes an embedded timer that monitors switches and system activity. After a specified period of inactivity, the timer disables the MOSFET's gate drive, powering down the CPLD and other components connected to the MOSFET.

Q_1's source connects to the battery's positive terminal, and its drain connects to IC_1's $V_{CC(INT)}$, $V_{CC(IO1)}$, and $V_{CC(IO2)}$ power pins and other components that require power-down control. When power switches off, a 1-kΩ pullup resistor, R_3, keeps Q_1 off by maintaining its gate at a gate-to-source voltage of 0V. When you turn off IC_1, it presents a leakage path to ground through the CPLD's power-down pin. The EPM570-T100 includes hot-socket protection that limits the current available from any user-accessible device-I/O pin to less than 300 μA. Thus, even in the worst case, the voltage that the I/O pin develops across R_3 doesn't reach the FET's minimum gate-threshold turn-on voltage of 0.7V.

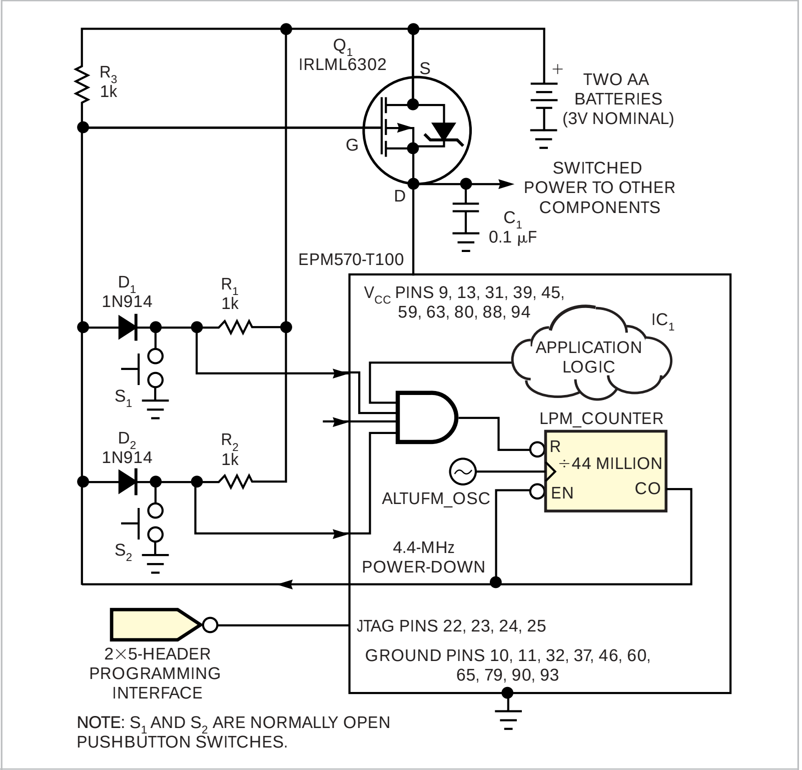

Figure 1 A few external components and internal logic blocks enable a CPLD circuit to switch itself off after a predetermined interval.

Pressing any switch creates a current path through the switch's contacts and its associated diode, which in turn develops approximately 2.3V of gate-source bias across R_3—more than enough to turn on Q_1 and to power up IC_1 in approximately 100 μsec. When you actuate the mechanical switches, they exhibit a minimum on-time of at least 3 msec, whereas a typical human operator's minimum press-and-release operation consumes at least 30 msec. During these relatively slow response times, the CPLD can turn on, resetting its internal circuitry and asserting its power-down pin to a logic zero that turns on Q_1 before the operator can release the switch.

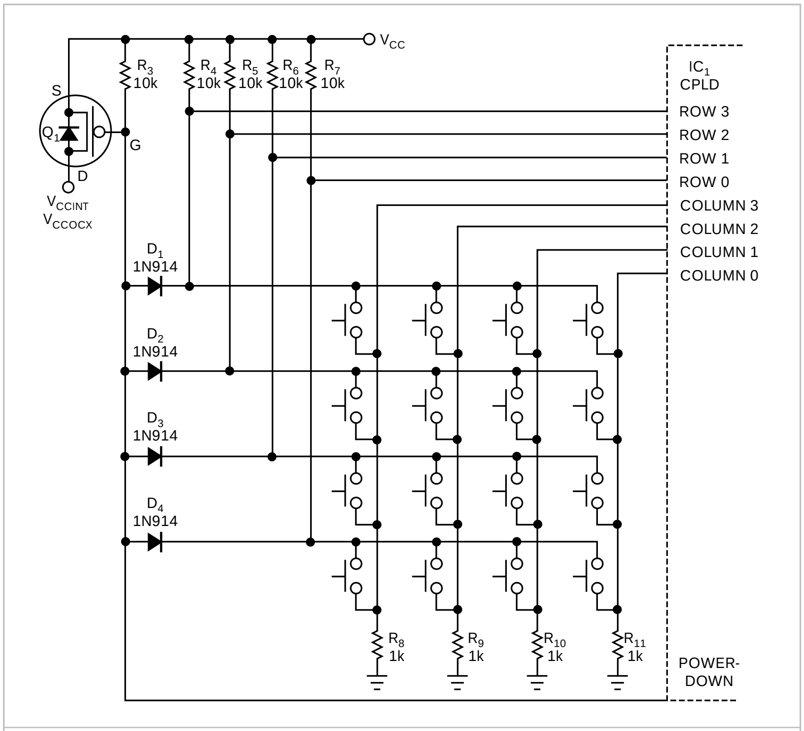

Figure 2 A keypad matrix expands the CPLD circuit's control capabilities and retains the circuit's automatic power-off function.

In addition to user-specified application logic (not shown), the CPLD's power-control logic adds a pair of standard parameterized, library-macro circuits that Altera's (www.altera.com) Quartus II development tools generate. An internal 4.4-MHz±25% oscillator, Altufm_osc, drives a modulo-44-million LPM (library-parameterized-module) counter. A logic-low signal that the CPLD's application logic produces or closing any switch resets the counter. When you reset the counter, its carry-out signal goes low and drives the external power-down pin. An inverted version of the carry-out signal re-enables the LPM counter once you remove the reset.

If you leave all switches open and the application logic becomes inactive, the counter counts to 44 million in approximately 10 sec, and the internal carry-out signal goes high, disabling the counter and holding the carry-out signal high. In turn, the power-down pin rises toward V_{CC}, turning off Q_1 when the voltage on the power-down pin reaches 2.3V. Removing power from the CPLD places the power-down pin in the tristate, or disconnected, mode, and R_3 keeps Q_1 off.

You can use JTAG-compliant commands to configure the EPM570-T100 with a download cable you connect to a manufacturer-defined 10-pin header. The process requires that you press an external switch before, during, and shortly after configuration to ensure that the CPLD receives power throughout the configuration process. You can set the inactivity time-out to any desired value by changing the counter's modulus. Although power, ground, and JTAG signals use specific device pins, you can assign any general-purpose CPLD I/O pins as inputs for switches and as the power-down output.

If your application requires a matrix of pushbutton switches, you can use only n diodes to configure an n×m switch matrix for efficient power-up detection (**Figure 2**). In this example, rows of switches connect to the MOSFET's gate through diodes D_1 through D_4. Resistors R_8 through R_{11} provide a ground path for each column of switches and carry current only during key closures, holding the column inputs low while waiting to minimize power-supply current drain.

When a user presses any switch, Q_1's gate goes low, turning on the CPLD. A fast CPLD-power-up routine allows the application to scan the switch matrix's rows and columns and determine which switch a user pressed before the user can release the switch. In this application, the row signals reset the LPM counter's inactivity timer.EDN

Amplifier removes common-mode noise on RGB differential-video-transmission line

Tamara Papalias and Mike Wong, Intersil Corp

Comprising four twisted pairs within a durable external sheath, Category 5 network cable offers a common and cost-effective choice for transmitting component-video signals. Three of the pairs can carry RGB video signals, and the fourth pair carries audio, synchronization, and other transmissions. Unfortunately, Category 5 cable lacks shielding, and thus it's somewhat vulnerable to common-mode coupling that induces equal voltages in each of the cable's conductors. As a first line of defense against common-mode problems, you can configure RGB signals as differential voltages, but any voltage difference between the ground references of the twisted-pairs' drivers and receivers results in a common-mode signal on each of the received lines.

Common-mode-noise voltages limit transmission quality of video signals. This Design Idea shows how you can use a single operational amplifier to minimize common-mode signals' effects on differential-component-video receivers. In **Figure 1**, the receiver circuits' ground terminals (in red) show that the ground-reference voltages of each of the RGB differential signals differ from those present at the drivers. To maintain signal quality and minimize reflections, each video-signal twisted-pair transmission line terminates in 100Ω. For example, resistors R_{35} and R_{37} terminate the R+ line, and R_{36} and R_{38} terminate the R− line. Meanwhile, the G and B termination circuits are identical. Any common-mode voltage on the R-signal pair appears at the junction of R_{37} and R_{38} and across R_{39}.

To create a common-mode cancellation voltage, operational amplifier IC_1 sums and inverts the signals on all three or four signal-line pairs. For example, adding the R+ and R− signals cancels their differential-voltage components and doubles the common-mode voltage that each line contributes. Capacitors C_1 and C_2 provide ac coupling for the circuit's input and output, respectively. The output from IC_1 applies a common-mode bias voltage through a matched pair of 30-kΩ resistors, R_{42} and R_{43}, to the R+ and R− receiver network. Close tolerances for R_{42} and R_{43} ensure that the differential voltages delivered at R_{OUT+} and R_{OUT-} closely balance with respect to the inputs' common-mode

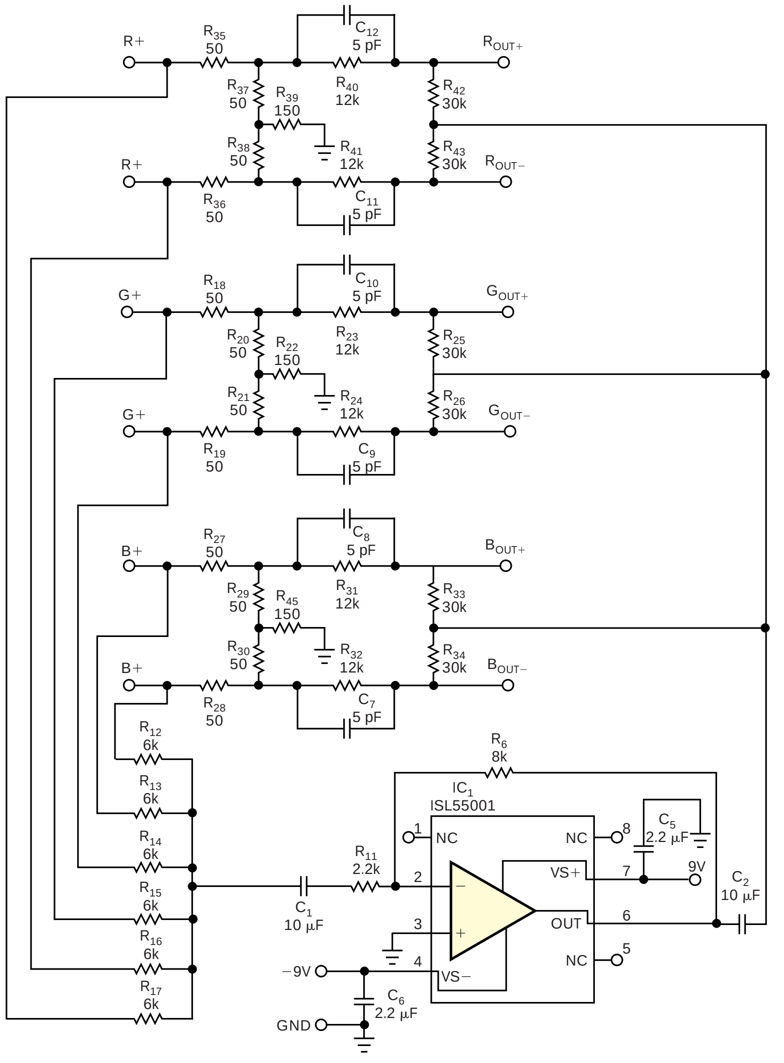

Figure 1 A common-mode-cleanup circuit reduces noise pickup on unshielded Category 5 differential-video signals.

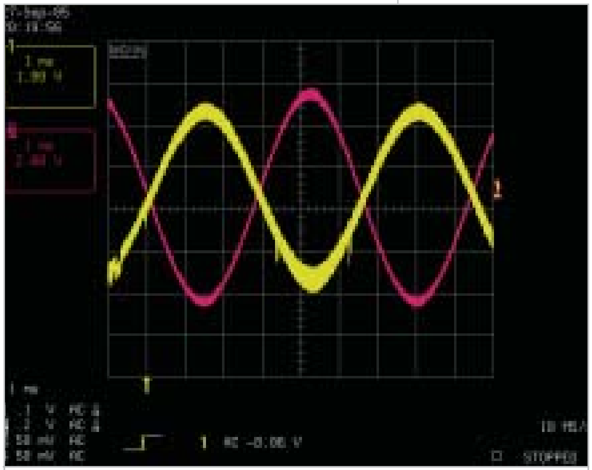

Figure 2 The common-mode signal (yellow trace) heavily influences the video signal (pink trace).

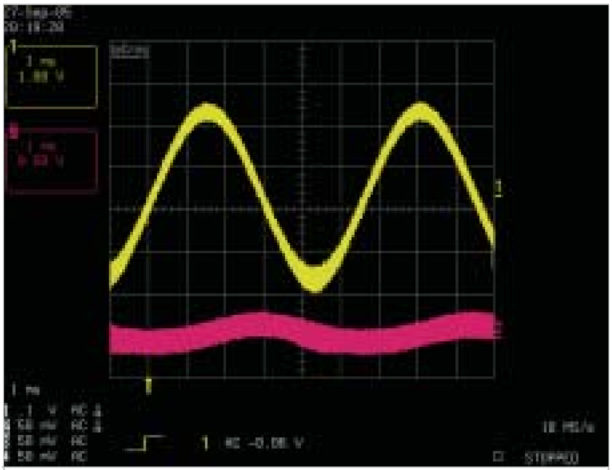

Figure 3 Adding the common-mode-reduction circuit in Figure 1 significantly reduces the amount of common-mode voltage on the video signal.

voltage. Capacitors C_{11} and C_{12} provide equalization to boost the differential-video signal's higher frequency components.

Before applying cancellation, the signals at the circuit's outputs R_{OUT+} and R_{OUT-} would appear as: $R_{OUT+}=V_{DIFF}/2+V_{CM}$, and $R_{OUT-}=-V_{DIFF}/2+V_{CM}$, where V_{DIFF} represents the desired differential signal, and V_{CM} exists with respect to the circuit's local ground. After applying cancellation, the output signals appear as: $R_{OUT+}=+V_{DIFF}/2+V_{CM}-V_{CMS}=+V_{DIFF}/2$, and $R_{OUT}-=-V_{DIFF}/2+V_{CM}-V_{CMS}=-V_{DIF}/2$, where V_{CMS} represents the summed and inverted common-mode voltage at IC_1's output.

Figure 2 shows a representative 1V peak received signal that's on the R+ line (yellow trace) and an accompanying 2V peak common-mode signal (pink trace). Figure 3 shows the circuit's common-mode-cancellation abilities. Although the differential signal (yellow) remains unchanged, the common-mode signal (pink) exhibits an 80%, 14-dB reduction. Any mismatch between the time delay and the summed analog signal, which the passive input network and IC_1, respectively, produce, prevents complete cancellation. Also, for best performance, the common-mode signal must not exceed IC_1's common-mode input-voltage rating. In addition, IC_1, an Intersil ISL55001, must exhibit unity-gain stability over a wide bandwidth and an excellent slew-rate response and, for best results, must operate at relatively high-power-supply voltages for good linearity. Use 10-μF, nonpolarized input- and output-coupling capacitors to accommodate extremely low-frequency common-mode voltages. Ensure adequate bypassing for IC_1's power-supply terminals for all frequencies of interest. EDN

Use a switching-regulator controller to generate fast pulses

Mitchell Lee, Linear Technology Corp

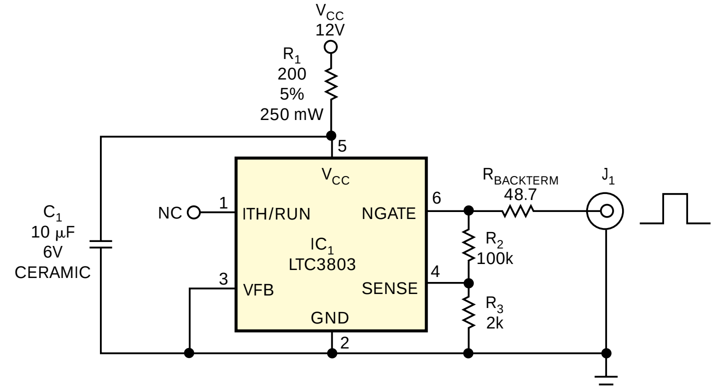

Figure 1 Switching-regulator-controller IC_1 delivers pulses with 1.5-nsec rise and fall times into a 50Ω load.

A source of pulses with fast-rising edges that approximate the step function can help you perform many useful laboratory measurements, including characterization of coaxial cables' rise times and location of cable faults using time-domain-reflectometry methods. For example, evaluating the rise time of a 10- to 20-ft-long RG-58/U cable requires edge-transition times of 1 to 2 nsec. Agilent's (www.agilent.com) HP8012B, a workhorse pulse generator that finds use in many electronics labs, can deliver pulses with rise times of 5 nsec that are adequate for many applications but not for cable characterization.

As an alternative, switching-regulator-controller ICs can deliver gate-drive pulses with rise and fall times of less than 2 nsec, making them ideal candidates for laboratory pulse-generation service. A simple implementation uses Linear Technology's (www.linear.com) LTC3803 constant-frequency flyback controller, IC_1 (Figure 1). The controller self-clocks at 200 kHz, and applying a sample of its output to its Sense pin causes the controller to operate at its minimum duty cycle and produce a 300-nsec-wide output pulse.

The LTC3803's output can deliver more than 180 mA into a 50Ω load, so use a low-series-inductance bypass capacitor that connects as directly as possible between IC_1's power and ground (pins 5 and 2). The decoupling components, C_1, a 10-μF ceramic capacitor, and R_1, a 200Ω resistor, minimize pulse-top aberrations without introducing amplitude droop. The circuit's output directly drives a 50Ω termination at amplitudes as high as 9V. For applications that require maximum pulse fidelity, use a back-termination resistor, $R_{BACKTERM}$, to suppress triple-transit echos and absorb reflections from the cable and any mismatch in the cable's far-end termination impedance. Back-termination also helps when driving passive filters, which expect to see a specific generator impedance. The LTC-3803's output impedance is approximately 1.5Ω, which affects the value of the back-termination resistor. The back-termination technique

(continued on pg 106)

works well with load impedances of at least 2 kΩ. At impedances higher than that value, parasitic impedances associated with the terminating resistor and IC_1 degrade bandwidth and pulse fidelity.

In a back-terminated, 50Ω system, the circuit delivers a 4.5V output pulse with symmetric rise and fall times of 1.5 nsec, pulse-top-amplitude aberrations of less than 10%, and amplitude droop of less than 5%. Directly driving a 50Ω load doesn't degrade the output's rise and fall times. For best pulse fidelity, use stripline techniques to route IC_1's output directly to the termination resistor and output connector J_1. Using a 100-mil-wide trace on a $^1/_{16}$-in., double-sided, glass-epoxy pc board approximates a 50Ω surge impedance.EDN

Shift registers and resistors deliver multiphase sine waves

Gary Steinbaugh, 4 E A Transform, Loveland, OH

Sine waves with fixed phase relationships find application in communications equipment, instrumentation, and power sources. Although you can use any of several traditional analog techniques to generate basic sine-wave signals, this Design Idea offers a simple method that uses only digital logic and fixed-value resistors (Figure 1a). A common clock pulse drives three of four sections of a pair of CD4015 4-bit shift registers that recirculate a pattern comprising 12 zeros and 12 ones—that is, 000000000000111111111111. Each of the registers' outputs drives a resistor, R_1 through R_{12}, that connects to a summing node. If all of the resistors were of equal value, their summed output would comprise a stepped linear triangular waveform at a repetition frequency one-twenty-fourth that of the clock frequency.

To produce a stepped sinusoidal output waveform, you replace the equal-value resistors with the weighted values in **Figure 1a**. If you use resistors of 1% tolerance, the output's amplitude will approximate that of a true sine wave to better than 1°. To produce a cleaner sine wave, a lowpass filter helps remove clock-pulse feedthrough and stepped-edge transients (**Figure 1b**). For many applications, a simple one-pole lowpass filter/buffer provides adequate filtering, but a more elaborate multipole filter further increases output purity.

You can add a second set of registers and resistors, R_{13} through R_{24}, to produce cosine and sine waves offset by a 90° phase shift—that is, two sine waves in quadrature (**Figure 2**). Register IC_{2A}'s inverted and recirculated output from Q4 generates the 000000000000111111111111 bit pattern that the first set of shift registers uses. IC_{1B}'s Q2 output produces the D input that you apply to the second set of shift registers—IC_{2B}, IC_{3A}, and IC_{3B}—which in turn generate a 90° phase-shifted version of the bit pattern to form a cosine wave. The cosine bit pattern requires no recirculation and simply propagates

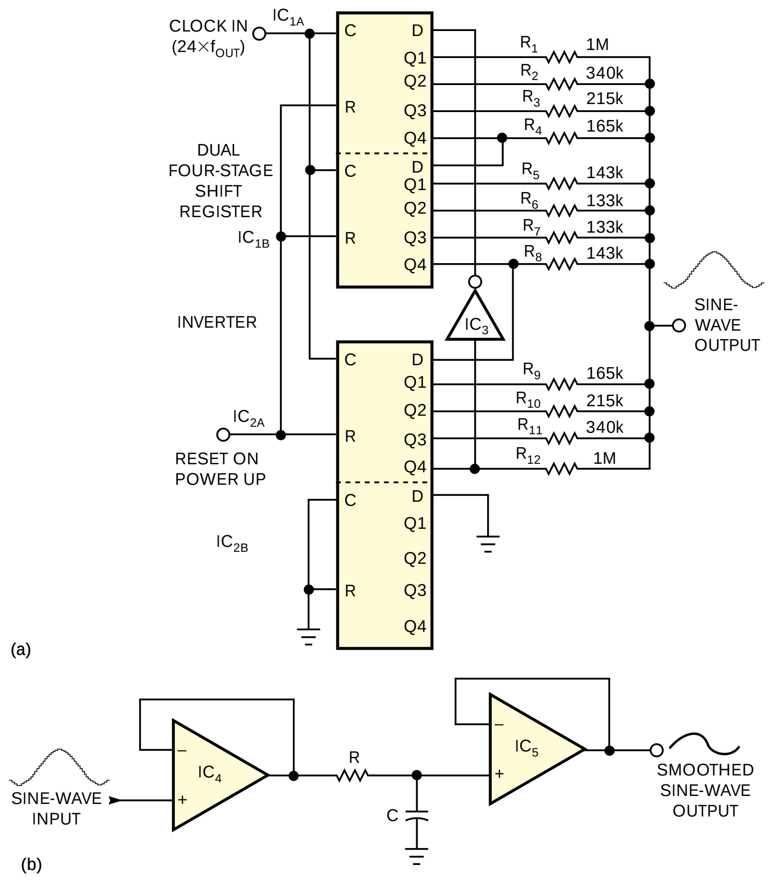

Figure 1 A pair of shift registers, an inverter, and a handful of precision resistors form a sine-wave generator (a). Two operational amplifiers form a resistance-capacitance lowpass filter that removes clock-signal artifacts from the output (b).

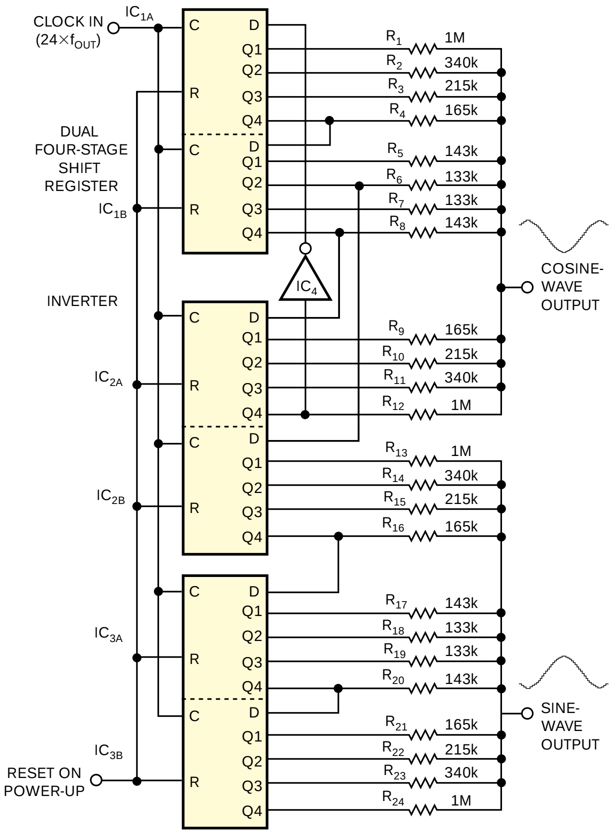

Figure 2 Add a second set of shift registers to generate a cosine wave.

through the second set of shift registers and "falls off the end." To adjust the second output's phase shift with respect to the first output from 15 to 180° in 15° increments, you can connect IC_{2B}'s D input to any one of IC_1's or IC_{2A}'s Q outputs.

Figure 3 illustrates a three-phase sine-wave-generator circuit. The Q4 output from IC_{1B} supplies the D input to the second set of shift registers, IC_{2A} and IC_{2B}, to produce the recirculated bit pattern. In similar fashion, the Q4 output from IC_{3A} supplies the D input to the third set of shift registers, IC_{4A}, to transfer a duplicate bit pattern that's phase-shifted by 240° with respect to the output from the first set of shift registers.

Register IC_{2B}'s D input connects to IC_{1B}'s Q4 output to produce a signal—Phase 2's output—that lags behind the Phase 1 output by 120°. In similar fashion, register IC_{4A}'s D input connects to IC_{3A}'s Q4 output to produce a signal—Phase 3's output—that lags behind Phase 2's output by 120°, or 240° with respect to Phase 1.

You can expand the basic circuit to accommodate additional signal phases. The weighted resistors' values are adequate for low-frequency sine waves and 4000-series CMOS-logic devices. However, you can scale the resistors' values to accommodate other output frequencies and logic families. EDN

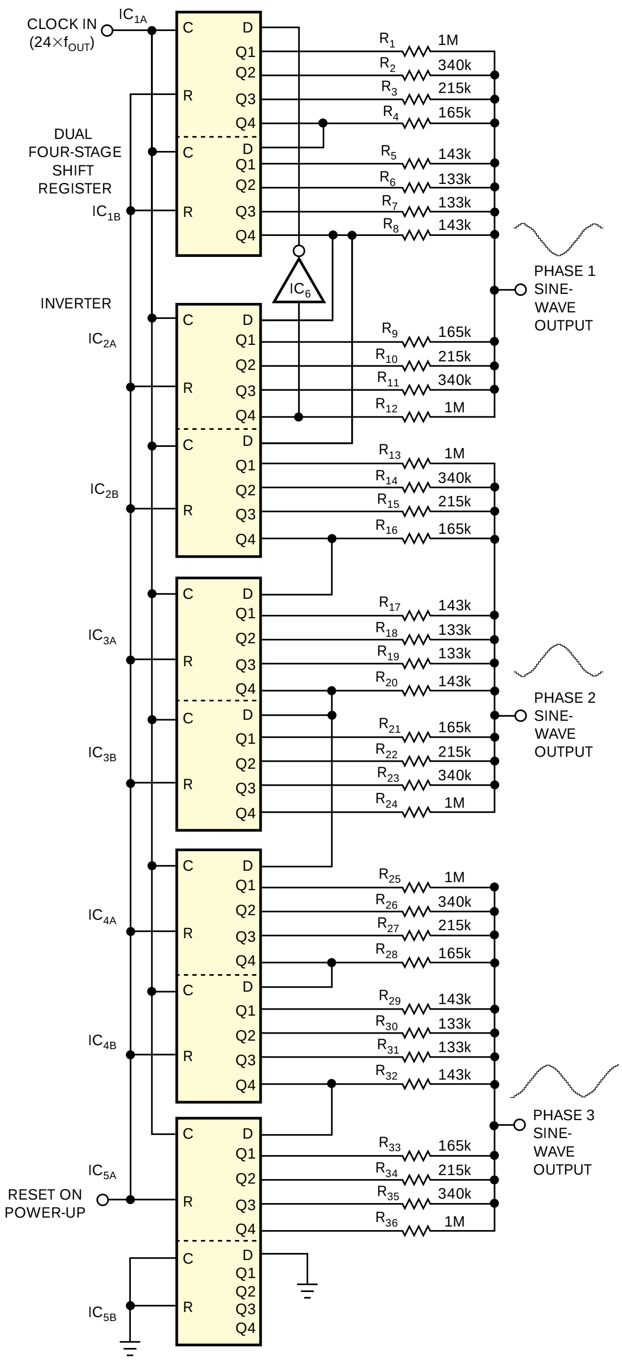

Figure 3 Adding a third set of shift registers yields a three-phase sine-wave output.