



BY BONNIE BAKER

Charge your SAR-converter inputs

It is tempting to drive a SAR (successive-approximation register) ADC with just an amplifier. As an added benefit, you might try to configure the amplifier circuit in a gain or antialiasing-filter stage. These enhancements seem reasonable as you try to optimize your device use. However, did you think about whether you would compromise the effectiveness of your op-amp/converter pair (Figure 1)?

If you need good, accurate performance at dc as well as ac, regardless of your throughput rate, the analog-input stage of the SAR ADC requires special attention. The model of the input stage of most modern ADCs is a resistor/capacitor pair with two switches and a voltage source (Figure 2). The resistance, R_{SW} , in the converter's input is the closed-switch resistance. This switch

closes during the acquisition time of the conversion process and opens during the conversion time. The converter uses capacitance, C_{SH} , which is the total of the distributed on-chip capacitance, for the input-signal-sampling process.

First and foremost, you need to give sample capacitor C_{SH} enough charging time to reach at least $1/2$ LSB of the final value. Theoretically, for a 12-bit con-

verter, enough time would be more than eight times $R_{SW} \times C_{SH}$. Given error margins and component variations, you should use multiples of 10 to 15. The SAR converter needs an op amp with a gain of $\pm 1V/V$, along with an R_{IN} - C_{IN} external resistor/capacitor pair. During sampling, the ADC uses capacitor C_{IN} for signal stability. Resistor R_{IN} isolates the amplifier from the ADC's load capacitance. The op amp isolates the ADC from high-impedance loads and drives C_{IN} and C_{SH} , facilitating a quick charge time while the ADC is sampling.

Design this seemingly simple circuit with the following guidelines. C_{IN} is a silver mica or C0G dielectric-type capacitor. These types of capacitors provide stability to the voltage and frequency coefficient of C_{SH} . Capacitors such as X7R, Z5U, and others have significant voltage and frequency "memory" and might degrade the converter's total-harmonic-distortion performance. At a minimum, the value of C_{IN} is greater than 20 times C_{SH} . You determine the value of R_{IN} using the ADC internal resistor and capacitor values. The time constant of the final values of C_{IN} and R_{IN} is 70% of the C_{SH}/R_{SW} time constant, with a value of $50\Omega < R_{IN} < 2\text{ k}\Omega$. Finally, the op-amp circuit, with C_{IN} and R_{IN} installed, should be able to settle to your converter's resolution and still drive a step-response signal. You can prove this function with bench testing (Reference 1).

REFERENCE

1 Oljaca, Miro, and Bill Klein, "Optimizing the High Accuracy Measurement Circuit ...," PCIM conference proceedings, 2004.

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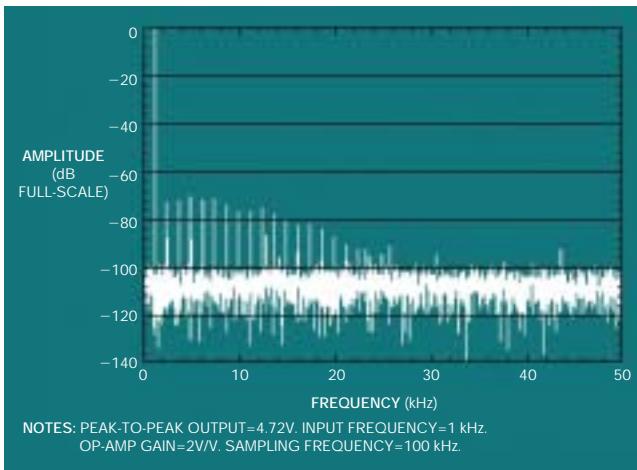


Figure 1 An improperly driven, 12-bit SAR ADC can produce unwanted noise and harmonic distortion. In this diagram, the SNR (signal-to-noise ratio) is 69.76 dB full-scale, and the THD (total harmonic distortion) is -63.34 dB full-scale for a converter that performs at an SNR of 71.82 dB full-scale and a THD of 78.82 dB full-scale.

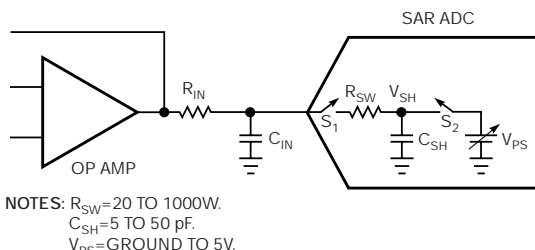


Figure 2 The input structure of a SAR converter initially has a sample-and-hold capacitor, C_{SW} , following a switch, S_1 , which controls the sampling time.