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## JFET cascode boosts current-source performance

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Many process-control sensors, such as thermistors and strain-gauge bridges, require accurate bias currents. By adding a single current-setting resistor,  $R_1$ , you can configure voltage-reference circuit IC<sub>1</sub> to produce a constant and accurate current source (Figure 1). However, the source's errors depend on the accuracy of both  $R_1$  and IC<sub>1</sub> and affect measurement accuracy and resolution. Although you can specify high-precision resistors whose accuracy exceeds that of most commonly available voltage-reference ICs, the voltage reference's error dominates this current source's accuracy. Although the manufacturer minimizes the voltage reference's temperature sensitivity and output-voltage error, sensitivity to power-supply variations can affect its accuracy, especial-

ly in process-control applications that must operate over a wide range of supply voltages.

A cascode-connected pair of JFETs,  $Q_1$  and  $Q_2$ , form a constant-current source that minimizes the reference circuit's sensitivity to supply-voltage fluctuations and extends IC<sub>1</sub>'s operating voltage beyond its 5.5V maximum rating. In addition,  $Q_1$  and  $Q_2$  effectively increase the current source's equivalent resistance from a few megohms almost into the gigohm range. In the circuit's Norton model, equivalent resistance represents the parallel resistance across an ideal current source.

An N-channel JFET operates as a depletion-mode device at its maximum saturated drain current when its gate-to-source bias voltage is 0V. In

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contrast to a depletion-mode MOSFET that requires a gate-bias voltage to conduct, the JFET operates in a default on-state and requires gate-bias voltage to cut off conduction. As its gate-to-source voltage becomes more negative with respect to the source, a JFET's drain current goes to zero at the pinch-off voltage. The JFET's drain current varies approximately with its gate bias:  $I_D \approx I_{DSS} \times (1 + V_{GS}/V_p)^2$ , where  $I_D$  is drain current,  $I_{DSS}$  is the sat-

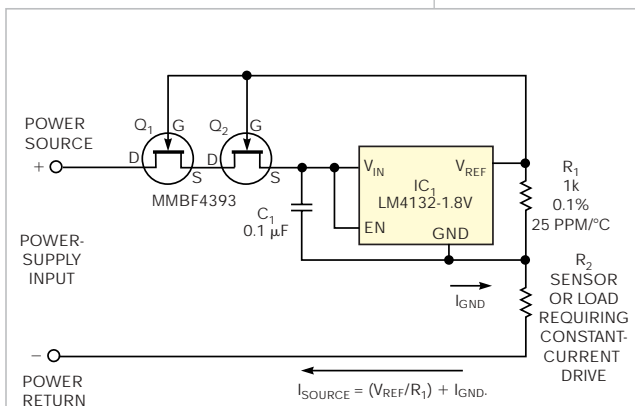


Figure 1 A pair of cascode-connected JFETs reduces the effects of power-supply-voltage fluctuations on a current source's accuracy.

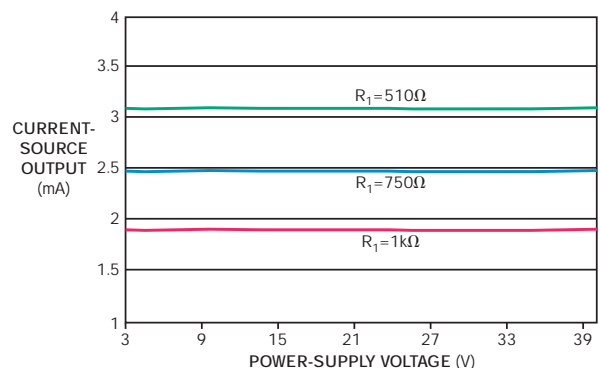


Figure 2 Setting  $R_1$  to values of 1 kΩ, 750Ω, and 510Ω delivers output currents of approximately 1.8, 2.5, and 3.6 mA that are insensitive to a wide range of power-supply voltages.

urated drain current,  $V_{GS}$  is the gate-to-source voltage, and  $V_p$  is the pinch-off voltage.

Assume that  $IC_1$ 's output voltage,  $V_{REF}$ , remains constant at 1.8V. Because the output voltage drives  $Q_2$ 's gate,  $IC_1$ 's input voltage,  $V_{IN}$ , equals  $V_{REF} - V_{GS(Q2)}$ , or  $1.8V - (-1.2V) = 3V$ . Thus,  $Q_2$ 's gate-to-source voltage rests at its nominal pinch-off voltage of 1.2V and varies in step with small changes in current source. As the power-supply voltage varies from 3V to more than 30V, then the input voltage remains almost constant, as you would expect, because  $V_{REF}$  also remains constant. The cascoded-FET configuration increases the current source's Norton equivalent resistance beyond that of the voltage reference and  $R_1$  alone. You

can use a single JFET, but stacking two JFETs further enhances the circuit's effective impedance. Note that  $IC_1$  doesn't degrade accuracy because the JFETs hold  $IC_1$ 's input voltage virtually constant, and  $IC_1$  effectively cancels initial gate-to-source-voltage variations and temperature effects that  $Q_1$  and  $Q_2$  introduce.

Negative feedback in the Kirchhoff-voltage loop that comprises  $V_{IN}$ ,  $V_{REF}$ , and  $V_{GS(Q2)}$  allows the drain current to reach an equilibrium bias point that satisfies  $Q_2$ 's transfer equation. Comprising the sum of  $(V_{REF}/R_1)$  plus  $IC_1$ 's internal "housekeeping" current,  $I_{GND}$ ,  $Q_2$ 's drain current remains constant. Adding  $Q_1$  reduces the effects of  $Q_2$ 's output impedance to insignificance. Adjusting the value of  $R_1$  varies the cir-

cuit's output current over a useful range of 200  $\mu A$  to 5 mA, with  $Q_2$ 's saturated-drain-current specification imposing an upper limit. If you select a JFET with higher saturated drain current, make sure not to exceed  $Q_1$ 's maximum power dissipation.

Note that the circuit's lower power-supply-voltage limit must exceed the circuit's compliance voltage, 3V, plus the voltage drop that the sensor introduces:  $I_{SOURCE} \times R_2$ . The circuit's upper power-supply voltage must not exceed  $I_{SOURCE} \times R_2 + 30V$ . For example, supplying a current of 2.5 mA to a 1-k $\Omega$  pressure-sensor bridge,  $R_2$ , limits the power-supply-voltage range to 5.5 to 32.5V. The circuit's output current varies less than 1  $\mu A$  over a wide range of power-supply voltages (Figure 2). EDN

## Microcontroller delivers voltage-multiplied dc power

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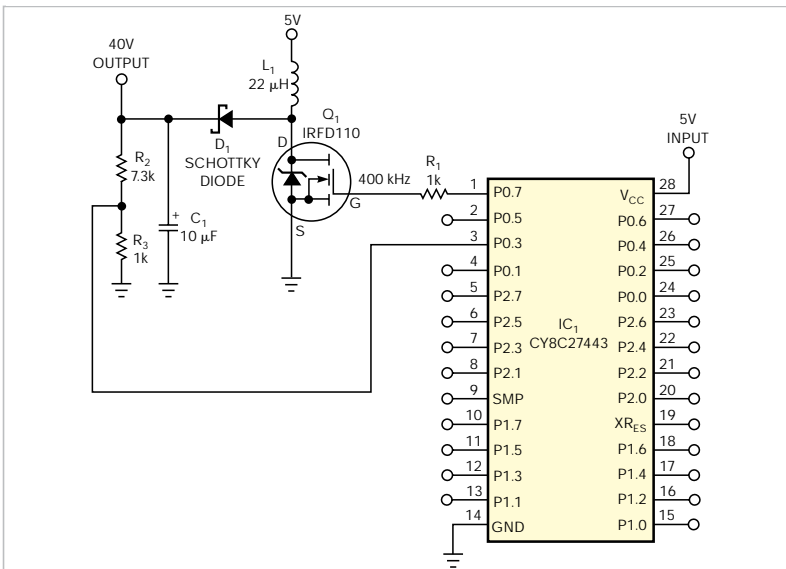


Figure 1 Use a pair of a PSOC microprocessor's internal blocks and a few external components to build a voltage-boost converter. Use a Schottky diode rated for a peak-inverse voltage of 100V for  $D_1$ . The PSOC's remaining pins are available for application support.

The combination of an external circuit and a low-voltage microcontroller occasionally requires a significantly higher power-supply voltage. You can use either an external boost converter to increase the logic supply or a buck converter to decrease an even higher voltage. However, you can alternatively use the microcontroller to create a higher voltage. For example, some of Cypress Semiconductor's (www.cypress.com) PSOC (programmable-system-on-chip) microcontrollers include a configurable comparator block that, with a PWM block, can form the heart of a simple inductor-based boost converter (Figure 1). A few external components implement a 40V power supply (Figure 2). When the feedback voltage you apply to Pin 3 (P0.3) exceeds the comparator's software-defined threshold voltage, the comparator shuts off the PWM stage. When the voltage drops below the threshold, the comparator re-enables the PWM block and thus regulates the output voltage. The voltage regulator uses only hardware blocks and

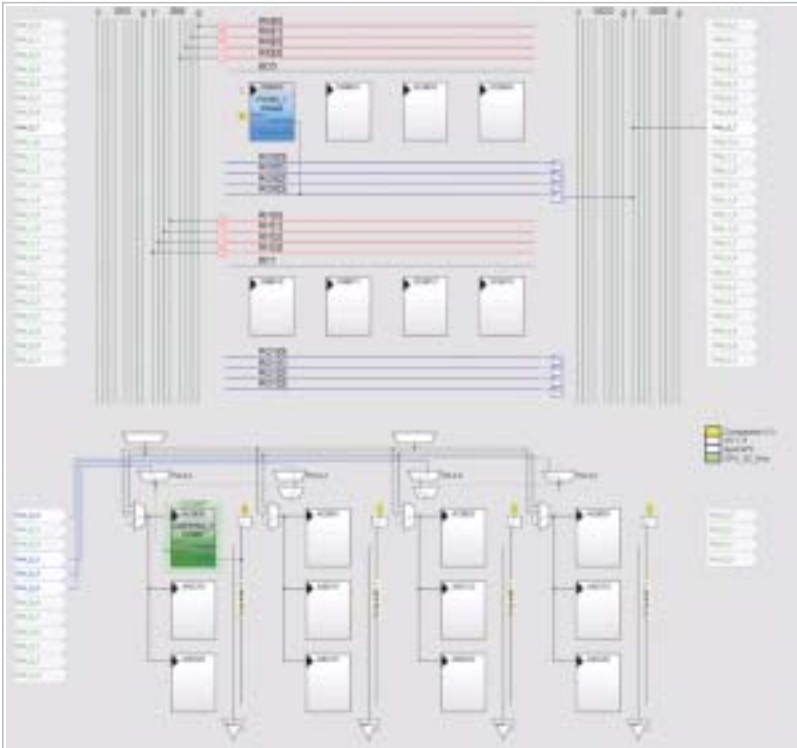


Figure 2 A pulse-width modulator (top) and a comparator (bottom) can operate independently of other PSOC functions. Unconnected pins are available for additional functions.

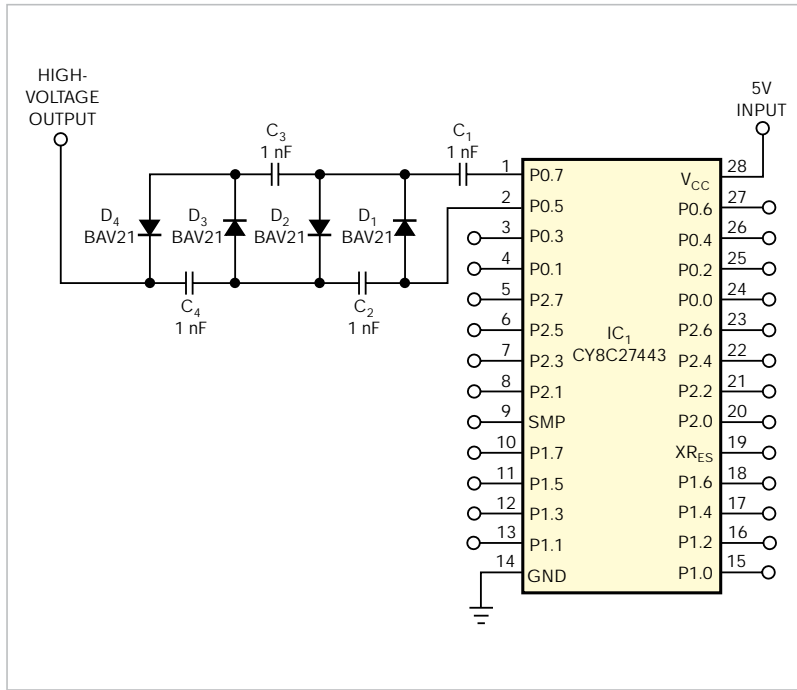


Figure 3 A few diodes and capacitors form a Villard Cascade voltage multiplier.

thus is immune to the effects of other activities taking place in the PSOC's CPU.

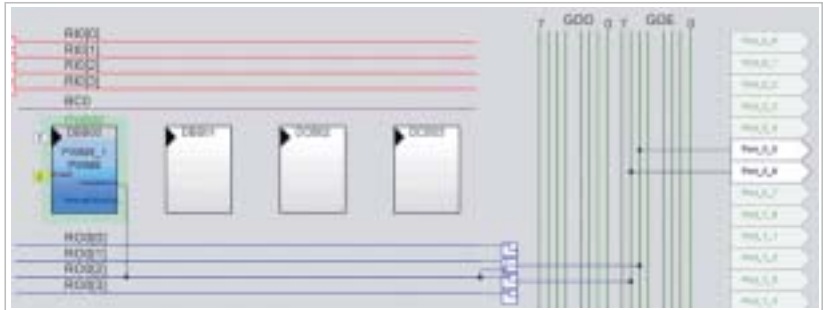
However, some microcontrollers lack a built-in comparator. For these devices, the Villard Cascade circuit offers a less expensive alternative to an external boost-voltage converter (Reference 1). Most engineers who are familiar with the Villard Cascade associate it with high-voltage applications and do not envision it as a low-voltage dc-supply technique. The circuit in Figure 3 requires an ac input source that you can easily simulate using a PSOC's internal PWM and inverter blocks. A square-wave output voltage appears on Pin 1, and an inverted version of the same square wave appears on Pin 2. The voltage difference between the two pins applies an ac square-wave voltage to the cascade.

Figure 4 shows how to configure a PSOC's internal blocks to drive the circuit in Figure 3. The PSOC's output multiplexer inverts the PWM's output and drives Port\_0\_5, and Port\_0\_6 receives the PWM's noninverted output signal. Again, the PSOC uses hardware blocks to drive a Villard Cascade voltage multiplier, and the circuit produces an output voltage without regard to CPU activity. For an input voltage,  $V_{IN}$ , a Villard Cascade of  $N$  stages delivers an output voltage of  $V_{IN} \times 2N$ . One stage comprises two diodes and two capacitors (Figure 5). However, the series-connected capacitors and diodes introduce voltage drops that limit the output current available from a Villard Cascade. In addition, the following equation imposes a practical limit that governs the cascade's output voltage:

$$\Delta V = \frac{I}{fC} \left( \frac{2}{3} N^3 + \frac{1}{2} N^2 - \frac{1}{6} N \right),$$

where  $\Delta V$  is the output-voltage drop,  $f$  is the input frequency,  $C$  is the capacitance,  $I$  is the output current, and  $N$  is the number of stages.

Both boost circuits can supply only modest amounts of current, especial-

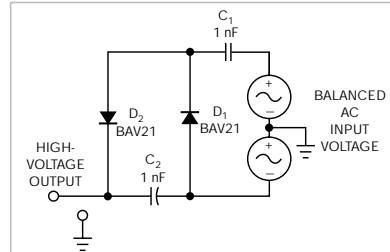


**Figure 4** To drive a Villard Cascade multiplier, a PWM block and an inverter block deliver a balanced ac voltage with respect to ground.

ly when they receive power from a 5 or 3.3V source. However, you can charge a high-value storage capacitor from the boost circuit's output and drive a load that presents a low duty cycle (for example, solenoid actuation).<sup>EDN</sup>

## REFERENCE

1 "Jochen's High Voltage Page," [www.kronjaeger.com/hv/hv/src/mul/](http://www.kronjaeger.com/hv/hv/src/mul/).



**Figure 5** An isolated multiplier stage eases analysis.

## Low-dropout linear regulators deliver constant currents

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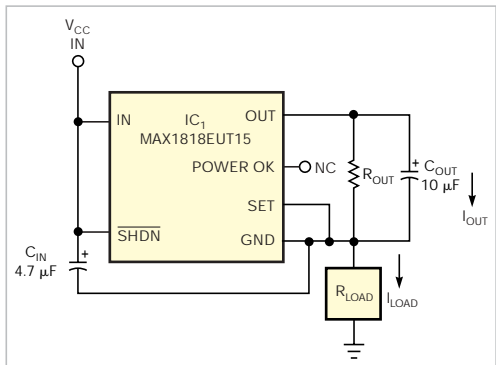
Linear voltage regulators offer a simple method of producing a constant current by connecting a fixed resistor between the regulator's output and ground nodes. The regulator's constant output voltage produces a constant current through the resistor. You can use the basic circuit as either a high-side or a low-side current source. The high-side current source uses a positive-output linear voltage regulator, IC<sub>1</sub>, a Maxim MAX1818, to provide a constant current of 25 mA to the load resistance (**Figure 1**). The design imposes two conditions: First, the voltage between IC<sub>1</sub>'s V<sub>CC</sub> and ground terminals must not exceed 5.5V. Second, the voltage between IC<sub>1</sub>'s input and ground terminals must meet or exceed 2.5V, the minimum voltage for proper operation. To satisfy these conditions, choose an output-resistance value that allows 2.5 to 5.5V between input and

ground and provides a fixed output of 1.5V across the output resistance at the desired load current.

For example, if you use the circuit to drive a constant current through a 100Ω maximum load resistance while applying 5V V<sub>CC</sub> between IC<sub>1</sub> and ground, the circuit functions properly when R<sub>OUT</sub> equals or exceeds 60Ω. This value allows a maximum programmable current of 1.5V/60Ω, or 25 mA. The voltage across IC<sub>1</sub> then equals the allowed minimum: 5V – (25 mA × 100Ω) = 2.5V. Available in six-pin SOT-23 packages, the MAX1818 can source as much as 500 mA.

The low-side current-source circuit draws a constant current of 2.5V divided by the output resistance through the load resistance (**Figure 2**). In this example, IC<sub>1</sub>, a MAX1735 linear negative-voltage regulator, provides a fixed output voltage of –2.5V. As in **Figure 1**, ensuring a voltage of 2.5 to 6.5V be-

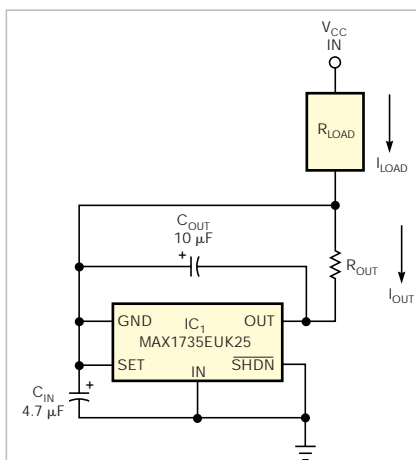
tween IC<sub>1</sub>'s ground and input terminals represents the only precaution for its proper operation. To satisfy that condition, choose an output-resistance value that allows 2.5 to 6.5V between ground



**Figure 1** This high-side constant-current source delivers load current of 2.5V divided by the output resistance, provided that you choose the output resistance to ensure that the voltage between the regulator's input and ground terminals is at least 2.5V.

and the input. When using the circuit to draw current through a maximum load of 100Ω with V<sub>CC</sub> at 5V, the output resistance should exceed 100Ω, which provides a maximum programmable current of 2.5V/100Ω=25 mA, which in turn produces a minimum recommended voltage across the device of 5V−(25 mA×100Ω)=2.5V. The MAX1735 can source as much as 200 mA and occupies a five-pin SOT-23 package.

In addition to the programmed load current, both configurations allow the regulator's quiescent current to flow through the load and introduce a source of error that varies with the voltage you apply between the regulator's input and ground connections. You can minimize the error by choosing a voltage regulator that draws low quiescent current or whose quiescent current remains constant through the operating range and allows you to compensate the error by adjusting the value of the output resist-



**Figure 2** As in Figure 1, this low-side constant-current source draws a load current of 2.5V divided by the output resistance, provided that you select the output resistance to make the voltage difference between IC<sub>1</sub>'s input and ground terminals at least 2.5V.

ance. Quiescent currents for the devices in **figures 1** and **2** typically average 130 μA and vary less than 40 μA for a regulator input-voltage range of 2.5 to 5V.<sup>EDN</sup>