# Build a precise dc floating-current source

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Although well-known to active-filter theorists and designers, GICs (generalized impedance converters) may be less familiar to analog generalists. Comprising a one-port active circuit typically comprising low-cost operational amplifiers, resistors, and capacitors, a GIC transforms capacitive reactance into inductive reactance and thus can substitute for an inductor in a filter that an RLC-transfer function describes. In addition, the flexibility of a GIC's input-impedance equation permits the design of virtual impedances that don't exist as physical components—for example, frequency-dependent resistance (**Reference 1**). The GIC, which its developers introduced 30 years ago, has seen its greatest application in ac-circuit and active-filter applications.

**Figure 1** shows a classic GIC circuit in which the input impedance, $Z_{IN}$, depends on the nature of impedances $Z_1$ through $Z_5$. The following equation describes the circuit's input impedance:

$$Z_{IN}=\frac{V_{IN}}{I_{IN}}=\frac{Z_1\times Z_3\times Z_5}{Z_2\times Z_4}.$$

For example, if $Z_1$, $Z_2$, $Z_3$, and $Z_5$ comprise resistors $R_1$, $R_2$, $R_3$, and $R_5$, and $Z_4$ comprises capacitor $C_4$, then the input impedance, $Z_{IN}$, appears as a virtual inductor of value $L_{IN}$:

$$L_{IN}=\frac{R_1\times R_3\times R_5\times C_4}{R_2}.$$

**Figure 2** shows the GIC circuit in its dc configuration. When you consider the GIC circuit in a purely dc environment, you can envision new applications. For example, you could replace impedances $Z_1$ through $Z_5$ with pure resistances $R_1$ through $R_5$. Instead of an ac input-voltage source, connect a precision temperature- and time-stable dc reference voltage to the input port. A simple circuit analysis using ideal op amps for $IC_1$ and $IC_2$ shows that the reference input voltage, $V_{REF}$, appears across resistor $R_5$, and, as the following equation shows, a constant current, $I_O$, flows through $R_5$.

$$I_O=\frac{V_{REF}}{R_5}.$$

However, op amp $IC_2$'s noninverting input diverts a small amount of current from the junction of $R_4$ and $R_5$, and $I_O$ thus also flows through $R_4$. Selecting

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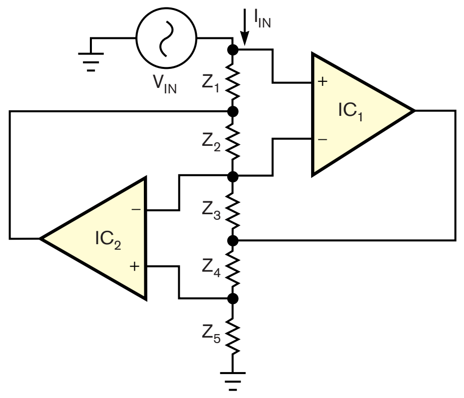

Figure 1 A classic generalized impedance converter provides a single-port impedance that appears at $V_{IN}$. The schematic omits power connections for clarity.

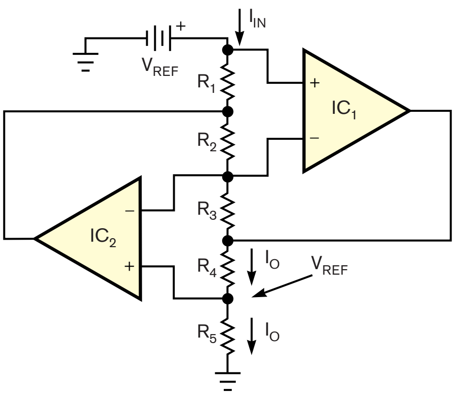

Figure 2 Replacing all of a GIC's impedances with resistors creates a constant-current source.

large values for $R_1$, $R_2$, and $R_3$ helps minimize current drawn from the reference voltage. For example, the circuit can supply 2 to 10 mA to $R_4$ and draw only a few tenths of a microampere from the reference source. Using tight-tolerance and low-drift components for $V_{REF}$ and $R_5$ ensures the stability of $I_O$. Applications include providing constant-current drive for Wheatstone-bridge and platinum-element sensors (**Reference 2**). In addition, you can replace $R_4$ with a series of resistive sensors as in an Anderson loop (**Reference 3**).**EDN**

## REFERENCES

1. Franco, S, *Design with Operational Amplifiers and Analog Integrated Circuits*, Third Edition, ISBN 0072-320842, WCB-McGraw-Hill, 2001.
2. Ramírez, Diego, S Casans, and C Reig, "Current loop generated from a generalized impedance converter: a new sensor signal conditioning circuit," *Review of Scientific Instruments, Volume 76, No. 1*, January 2005.
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# Frequency dithering enhances high-performance ADCs

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Since the late 1970s, designers have successfully improved the effective resolution and spurious performance of A/D converters by adding dither—uncorrelated noise—to a converter's input and then using DSP techniques to average out noise from the converted data. The most common dithering method adds random-amplitude noise to an A/D converter's input signal. Although this method works, the added noise includes large random peak values. To keep the A/D converter's input out of the saturation region, a designer must know both the peak signal and the peak dither levels. Even briefly saturating the A/D converter adds more nonlinearities than dither can remove.

Another approach adds a dithered-frequency, constant-amplitude signal. **Figure 1** shows one possible implementation featuring a Linear LTC1799 programmable oscillator, $IC_2$, that's operated in a VCO (voltage-controlled-oscillator) mode in which an applied voltage modulates the center frequency. You can set the LTC1799's center frequency at 1 kHz to 33 MHz, making it a suitable dither generator for many currently available A/D converters. Because the LTC1799's output comprises a square wave, its peak output amplitude is well-defined.

You can set the random-dither center frequency either below or above the signal frequency of interest. For conversion of a narrowband intermediate frequency, either location may work well. For an A/D converter that must operate to dc, the only useful location is above the signal frequency of interest. One approach places the dither frequency at one-half of the sampling or the Nyquist frequency. When you place it there, the random noise typically doesn't interfere with the desired signal, and any aliasing that occurs only folds the random frequency noise around itself and not into the desired signal band.

The circuit in **Figure 1** operates with a 20-MHz sampling A/D converter and generates random noise around a center frequency of 10 MHz. You can use any of a number of techniques to generate the random noise, including dig-

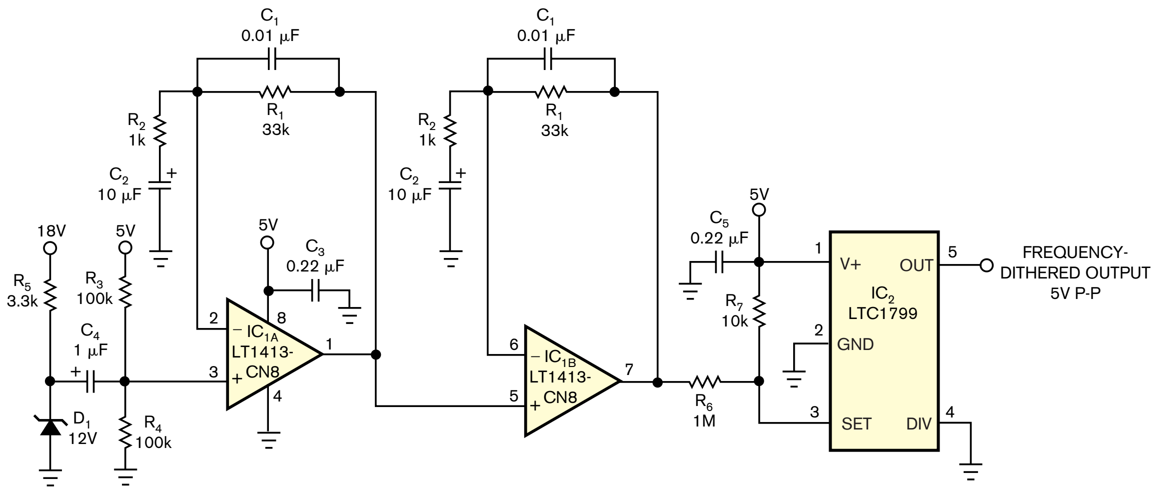

Figure 1 A zener diode, two stages of amplification, and an FM voltage-controlled oscillator form a constant-amplitude dither generator.

ital shift registers and semiconductor junctions biased into the breakdown range. In this design, a 12V zener diode, $D_1$, generates the noise, which a two-stage amplifier amplifies and frequency-shapes. If necessary, you can further shape the noise distribution by using more complex active-filter sections, $IC_{1A}$ and $IC_{1B}$. After filtering, the noise modulates the LTC1799. Make sure that the LTC1799's power-supply voltage is pure dc and free of ripple, because power-supply noise produces nonrandom AM sidebands.

**Figure 2** shows an amplitude-versus-frequency plot of the frequency-limited spectrum that the design in **Figure 1** produces. Depending on the circuit's configuration, you can apply the dither to the A/D converter using a small coupling capacitor or a more complex active summing circuit. Although zener-diode noise generators offer theoretical simplicity, they behave poorly in production environments because their noise outputs can vary greatly. Even among diodes from the same manufacturing batch, you can observe popcorn noise, unevenly distributed noise histograms, amplitude shifts, and frequency-weighted noise. In a high-volume application, well-specified noise diodes, such as those from Micronetics (www.micronetics.com), may prove more cost-effective than zener diodes.

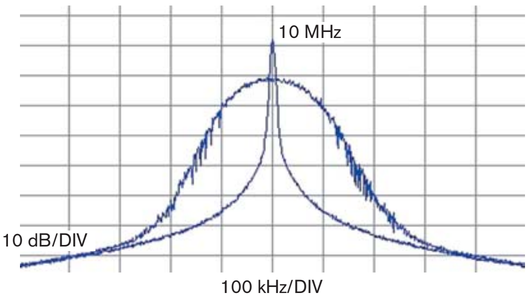

Figure 2 The broad bell-shaped curve shows a random-frequency-dithered spectrum superimposed onto the LTC1799's unmodulated, 10-MHz output.

Once you select a noise diode, you can select amplification-stage gains such that clipping of noise peaks isn't evident at the circuit's output. If your application requires it, you can alter the amplifiers' frequency responses to alter the noise spectrum. Finally, adjust the LTC1799's frequency-setting resistors, $R_6$ and $R_7$, so that the noise-spectrum display resembles that in **Figure 2**. Any clipping along the amplifier path tends to add peaks to the edges of the spectrum, which indicates amplitude clipping and reduction of the noise's random characteristics.

You can add a filter between the noise output and the A/D converter's summing input to limit inband noise or remove any periodic modulation that power-supply ripple introduces. In a modern, high-performance A/D converter, even a small amount of periodic noise can manifest itself as a −80-dBc (decibels-below-carrier) spurious response.**EDN**

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# Memory-termination IC balances charges on series capacitors

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As one of today's most interesting component families, high-value capacitors offer ratings ranging from tenths to tens of farads but suffer from relatively low working voltages. For example, Maxwell's (www.maxwell.com) PC10 ultracapacitor occupies an area about the size of a large postage stamp and the thickness of four stacked US 25-cent coins. The PC10 provides 10F capacitance, a 2.5A maximum discharge-current rating, and an 18Ω ESR (equivalent-series resistance). However, its rated working voltage is only 2.5V.

To accommodate a supply voltage greater than 2.5V, you can connect two capacitors in series, halving the available capacitance and doubling the overall voltage rating. However, due to differences in leakage current and capacitance, the voltage at the capacitor's common connection can vary, and your design must ensure that you do not exceed either capacitor's maximum voltage rating. If the series-connected capacitors' charge and discharge currents are relatively small, you can connect equal-valued charge-balancing resistors across both capacitors. But for farad-range capacitors that can deliver amperes of current, you need a more efficient approach.

The theoretical voltage across a capacitor comprises its initial voltage, $V_C(0)$, plus the integral of the capacitance, C, multiplied by the capacitor's current over time: $V_C(t)=V_C(0)+C\times\int I(t)dt$. In a two-capacitor divider, the current through both capacitors is

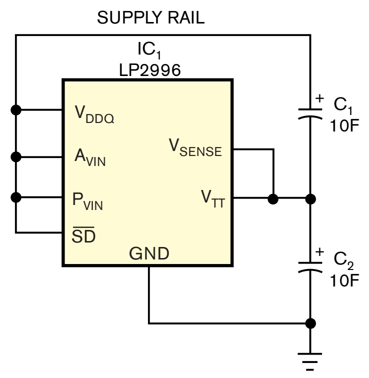

Figure 1 This simple circuit requires only a single IC to balance the charges on two series-connected, low-voltage, high-value capacitors and maintain their common junction at one-half of the supply voltage.

identical, and the loop equation, including the supply voltage, becomes: $V_{SUPPLY}=V_{C1}(0)+V_{C2}(0)+(C_1\times C_2)/(C_1+C_2)\times\int I(t)dt$. During charging to a 5V-supply level, differences in tolerances between $C_1$ and $C_2$ or residual voltages on either capacitor cause the voltage across one capacitor's terminals to exceed 2.5V and cause the other to fall below 2.5V.

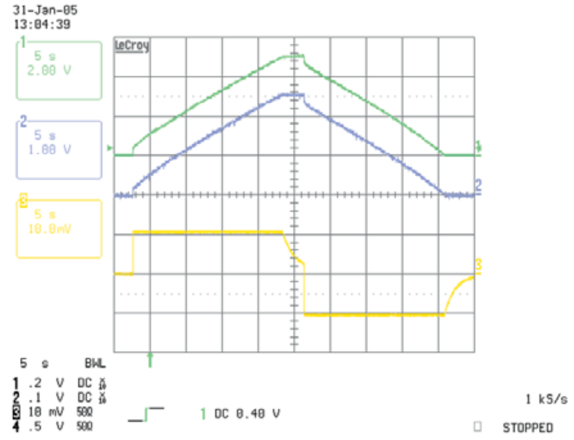

Figure 2 The oscilloscope waveforms within the active-balance circuit show the power-supply rail voltage (top trace), the midpoint voltage at the junction between the two capacitors (middle trace), and the charge/discharge current (lower trace, scaled to 1A per division). The traces reflect a 1A charge interval to 5V, followed by a 1A discharge to 0V. The waveform steps at the start of the charge and discharge intervals are due to the capacitor's internal ESRs.

To overcome this undesirable mismatch, the LP2996 DDR termination regulator, $IC_1$, sinks or sources current from both capacitors and actively maintains their voltages at one-half of the supply voltage (**Figure 1**). The LP2996 provides an active termination for DDR-SDRAM devices and can sink or source large amounts of current; its data sheet's nomenclature and labels reflect its intended memory-support role. The LP2996's Class B output, $V_{TT}$, drives the capacitors' common connection, actively maintaining the junction at $V_{DDQ}/2$ and becoming active only when the capacitors get out of balance. At balance, the LP2996 wastes no charging current and thus operates efficiently. The device's data sheet specifies that the LP2996's out-of-balance error amounts to a $V_{TT}$ offset of ±20 mV around the $V_{DDQ}/2$ setpoint. **Figure 2** shows charge and discharge waveforms for 1A current steps.

This active balancing circuit does impose some limitations. Using a power supply rated at 5V and 1A, the two capacitors achieve charge balance in a maximum of 25 sec: Charge time=5F×5V/1A. The initial charging interval overcomes any initial prebias charge on either $C_1$ or $C_2$. The steady-state current flow into and out of the LP2996 amounts to a fraction of the high current flowing through the capacitors and is just sufficient to overcome any tolerance mismatch in the two. The LP2996 includes thermal-shutdown protection, but an instantaneous short circuit across either capacitor may occur too quickly to activate the protection circuitry.

Thermal considerations determine the capacitor's maximum current-handling capability, and the PC10's data sheet derates the current downward from 2.5A. You can connect 1Ω current-limiting resistors in series with both capacitors if the power supply provides charging current in excess of 2A.

Upon interruption of the power supplied to the circuit, the LP2996 imposes a self-discharge current of less than 1 mA, which represents a capacitor-"battery" discharge rate of 5000 sec per volt into an open circuit. You can reduce the LP2996's self-discharge current by applying an external control signal to its shutdown input. Upon power interruption, the two-capacitor string can supply a constant-current load of 1A for 15 sec over a voltage change from 5 to 2V. You can connect additional pairs of capacitors in parallel to provide additional current, but, depending on capacitance mismatches, initial bias voltages, and current demand, you may need additional LP2996s to maintain charge balance.EDN

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# Voltage reference is software-programmable

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For a variety of reasons, designers often discover that their creations need yet more power-supply voltages. For example, a system powered by ±2.5V power supplies suddenly needs a precision −1.4V reference for a signal-level-shifting circuit and needs a 2.1V reference to drive an ADC. Your options include adding a couple of operational amplifiers and resistors to level-shift and buffer the system's voltage reference or adding a couple of DACs. Op-amp circuits lack programmability to accommodate design changes, and, although the DACs offer programmability, their settings are volatile, and the outputs are typically unipolar and lacking in drive capability.

The circuit in **Figure 1** offers an easy way to generate extra reference voltages and provides a few additional benefits. It allows you to easily generate positive or negative buffered references under software control. Its output buffer sinks and sources as much as 10 mA. You can read and adjust programmed voltages. On-chip storage restores the reference voltages after a power interruption, and a parity bit can indicate a malfunction if an internal device failure accidentally causes the programmed voltage to change.

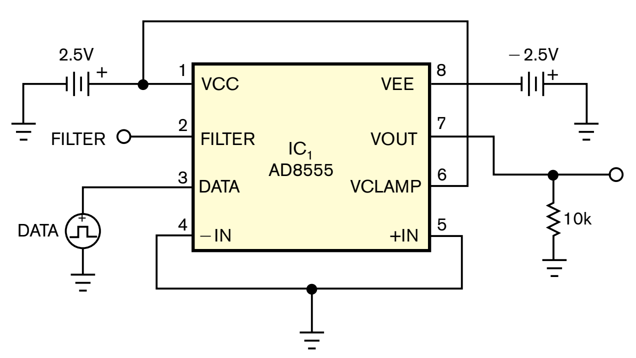


Figure 1 Occupying a tiny, eight-lead LFCSP footprint, a programmable instrumentation amplifier doubles as a last-minute adjustable-voltage bipolar-reference source.

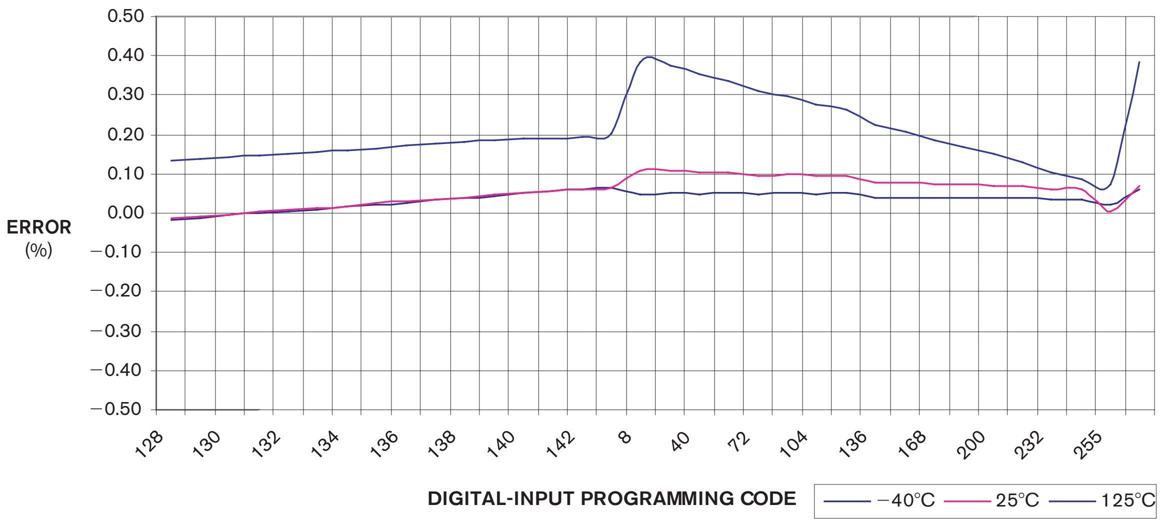
The programmable voltage reference comprises $IC_1$, an Analog Devices AD8555 high-precision auto-zero instrumentation amplifier, which contains an 8-bit DAC as part of its offset-adjustment circuit. In a change from its intended role, the monotonic DAC generates the output voltage, which can swing from $V_{SS}$ (input code 0) to $V_{DD}-1$ LSB (input code 255). The DAC's 8-bit resolution provides voltage steps of 0.39% of the difference between $V_{DD}$ and $V_{SS}$—for example, steps of 19.5 mV with a 5V supply. The output-voltage, $V_{DAC}$, temperature coefficient is less than 15 ppm/°C.

The following equation describes the DAC's approximate internal reference voltage, $V_{DAC}$:

$$V_{DAC} \approx \left(\frac{CODE+0.5}{256}\right)(V_{DD}-V_{SS})+V_{SS},$$

and the following equation yields the circuit's output voltage, $V_{OUT}$: $V_{OUT}=GAIN(V_{POS}-V_{NEG})+V_{DAC}$, in which GAIN represents the circuit's default internal gain of 70 for the differential input. Both inputs connect to ground, and the first term is thus close to 0V, or 10 μV maximum due to input-amplifier errors, and the circuit's output voltage, $V_{OUT}$, is equal to $V_{DAC}$.

Until you permanently program the internal registers, they allow you to alter the output voltage and explore the circuit's behavior as a fixed-voltage reference and reprogrammable 8-bit DAC. To program the output voltage, you apply the appropriate pattern according to the first equation and instructions from the device's data sheet. After verification, you can permanently set the output voltage by blowing certain of the device's internal polysilicon-fuse resistors. As **Figure 2** shows, for a given output-voltage level, the device's absolute error is less than 0.4% across a −40 to +140°C temperature range. **EDN**



**NOTE**: PERCENTAGE ERROR $=100\times\frac{V_{OUT(ACTUAL)}-V_{OUT(CALCULATED)}}{\text{5V FULL-SCALE}}$.

Figure 2 Output-voltage error for the reference circuit reaches a maximum of 0.4% at a temperature of −40°C and a 5V power supply.