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Scaling: a balanced view, part two

In the last installment of Analog Domain, I began a summary of Klaas Bult’s analysis on the effect of technology scaling on power dissipation (references 1 and 2). This column replicates the minimum-circuit model and Bult’s Algorithm for reference (figures 1 and 2). The algorithm depends on three process-dependent quantities and eight application-dependent parameters. It calculates six circuit measures, the last of which is the minimum power dissipation for the minimum circuit. Bult’s analysis does hang on a few assumptions, but more than a decade of

silicon-process history supports them, as do the foreseeable trends in silicon-process development.

The first value to calculate is the maximum V_{DD} . Ignoring the slight rise in the apparent dielectric strength of ultra-thin films compared with thicker film and bulk samples, V_{DD} is essentially proportional to gate-oxide thickness, T_{OX} . T_{OX} , in turn, scales directly with the process’s minimum feature size, L_{MIN} , by a ratio that has held essentially constant over process evolutions that saw L_{MIN} decline from 3 microns to 60 nm:

$$\lambda = \frac{T_{OX}}{L_{MIN}} \approx 0.03.$$

Linear circuits require head room between the signal swing and the supply rails. Bult’s model captures this quantity in the form of a *voltage efficiency*, η_{VOL} :

$$\eta_{VOL} = \frac{V_{SIG(-P)}}{V_{DD}}$$

Setting η_{VOL} to a reasonable constant value, say 80%, gives the maximum peak-to-peak signal amplitude, V_{SIG} .

The application determines the necessary dynamic range:

$$DR = \frac{V_{SIG(RMS)}}{\sqrt{\sum_i V_{UNWANTED}^2(i)}}$$

$$V_{SIG(RMS)} = \frac{V_{SIG(P-P)}}{2\sqrt{2}}$$

where $V_{UNWANTED}$ refers to the various voltage-error terms, including white noise, 1/f noise, and offset.

Though $V_{UNWANTED}$ results from the combination of multiple sources, often in practice one term dominates. As a result, the load-capacitance calculation depends on which term is most important to the application.

Applications that are sensitive to offset voltage require a high degree of device matching. Below the 700-nm node, the minimum capacitance to

attain a given degree of matching varies in proportion to $1/L_{MIN}$. (Calculations are available in Reference 2.) The minimum capacitance for a given dynamic range for circuits in which either white noise or 1/f noise is the dominant consideration varies as $1/L_{MIN}^2$. At the 90-nm node, the minimum capacitance for matching is about 200 times larger than the minimum capacitance for white noise, which is about 200 times larger than the minimum capacitance for 1/f noise. For this reason, circuits that demand a high degree of dc accuracy often use device averaging and offset-cancellation techniques.

Given the minimum capacitance that the circuit requires to attain the specified dynamic range, you can calculate the drive current necessary to meet bandwidth, slew-rate, settling-time, and distortion criteria. The next installment of this column will pick up from here. EDN

REFERENCES

- 1 Israelsohn, Joshua, “Scaling: a balanced view, part one,” *EDN*, March 30, 2006, pg 40, www.edn.com/article/CA6317072.
- 2 Bult, Klaas, “The effect of technology scaling on power dissipation in analog circuits,” *International Solid-State Circuits Conference 2006*, Feb 5, 2006.

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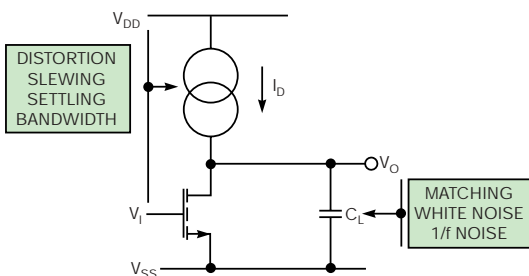


Figure 1 A single-transistor gain stage serves as Bult’s model minimum subcircuit.

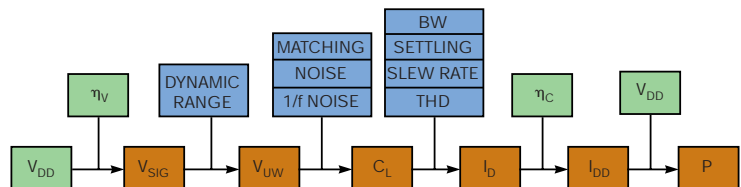


Figure 2 Bult’s analysis combines application requirements (blue) with terms that derive from the process scale (green) to generate calculated values (brown) resulting in a power estimate for the model subcircuit.