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Microcontroller, JFET form low-cost, two-digit millivoltmeter

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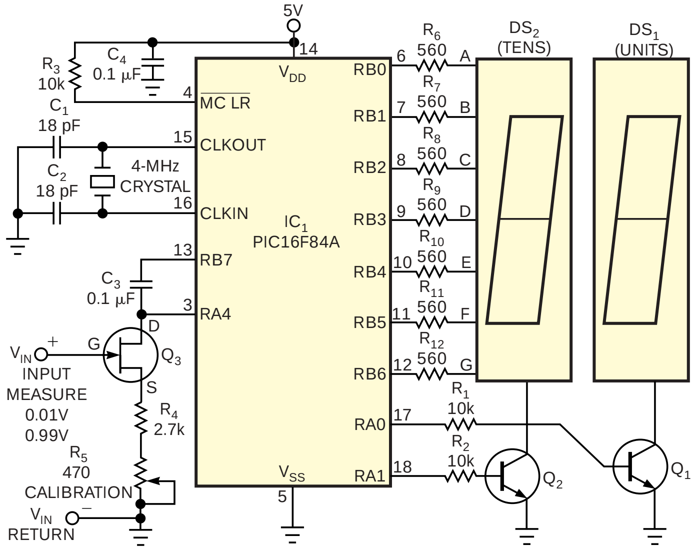
The circuit in **Figure 1** offers an inexpensive alternative to commercial digital voltmeters. Although it has only two digits, it provides considerable flexibility and thus lends itself to customization by means of a microcontroller and its software. As one of Microchip's (www.microchip.com) least expensive offerings, the PIC16F84A lacks an internal ADC. However, you can use a classic RC time-delay circuit to implement an analog-to-digital conversion by connecting capacitor C_3 between lines RB7 (output) and RA4 (input) and in series with an equivalent "unknown" resistor consisting of Q_3's drain-to-source on-resistance, plus R_4, plus R_5. Q_3, a BF245A JFET, presents the on-resistance. Q_3's "A" suffix is important because it corresponds to an on-resistance of 200Ω to 2 kΩ for a gate-to-source voltage of 0 to 1V (**Figure 2**). Other devices in the BF245 family exhibit a less pronounced change of resistance versus gate-to-source voltage. To correct the measurement nonlinearity inherent in Q_3's gate-to-source voltage versus drain-to-source on-resistance transfer, the microprocessor's software includes a 100-point look-up table that provides correction for a two-digit display.



NOTES: $Q_2=Q_1$=BC237/BC337/BC546 ... 550.
Q_3=BF245A. (USE "A" GRADE ONLY.)
C_1, C_2=SEE TEXT.
DS_1, DS_2=COMMON-CATHODE, SEVEN-SEGMENT LED DISPLAY.

Figure 1 Build a low-cost, two-digit dc millivoltmeter from a microprocessor and a few components.

For an application requiring the display of readings of 0.01 to 0.99V, you can use a 4-MHz crystal and Microchip's PIC16F84A microprocessor for IC_1. To display the rightmost three digits of readings in the 0.001 to 0.999V range, use a 20-MHz crystal and a PIC16F84A-20 microprocessor. Choose 15- to 33-pF values for capacitors C_1 and C_2, which the PIC's data sheet describes. **Listing 1**, which is available online at www.edn.com/060622di1, includes the full assembler source code for the PIC16F84A. The most critical portion of the firmware comprises a subroutine that provides a precision time delay according to the following steps:

1. Configure RA4 as an input to sense the voltage across C_3 during the charging interval. When you configure RA4 as an input, it serves as a Schmitt trigger with 1.6V low-threshold and 3.2V high-threshold voltages when drain-to-drain voltage is 5V.
2. Configure RB7 as an output and set it high to begin charging C_3. Initialize a counter (register $0C_H$) to its maximum value of FF_H.
3. Decrement the counter in a loop

until RA4 senses a low state. At that time, C_3 charges to nearly 66% of the power-supply voltage.

4. Use the time it takes to produce a low on the RA4 input as a jump value in the linearity-correction look-up table to extract a value for the two-digit LED readout.
5. Configure RB7 as an input and set it low to discharge capacitor C_3.
6. After a time delay, repeat Step 2.

To round out the design, another software subroutine solves the problem of driving a two-digit LED display at adequate visibility with a minimum amount of current. Although an LCD would use less current, LCDs aren't visible in darkness. The display subroutine examines the eight bits of the units and tens—registers 11_H and 12_H—and tests each one in sequence; if the subroutine sets a bit, then the subroutine puts a short-duration high state on its corresponding segment-driver line, RB. Doing so lights only one LED segment at a time, and, consequently, the maximum current consumption of the circuit remains relatively constant even if you add a third LED display to build a 999-count millivoltmeter.

Persistence of vision eliminates the need to keep the displayed digits continuously visible, and maintaining the segments on for approximately 33% of a 1-sec refresh interval allows a good and sufficient display effect. Transistors Q_1 and Q_2 are never simultaneously on, and only one display segment lights at a time. You can further optimize the hardware by removing current-limiting resistors R_6 through R_{12}, lifting the emitters of Q_1 and Q_2 from ground, and inserting a single 560Ω resistor between the emitters and ground.EDN

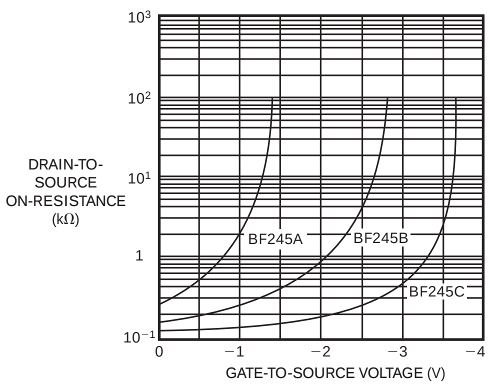


Figure 2 Gate-to-source-voltage-versus-drain-to-source-resistance-transfer curves for three selected grades of the BF245 JFET show maximum resistance variation for the "A" grade at low gate voltage.

Inexpensive envelope tracker handles wide signal variations

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Converting band-limited NRZ (non-return-to-zero) data to a digital format suitable for microprocessors and other digital systems poses problems when a signal's duty cycle or amplitude varies or when its average level unpredictably wanders within a given dc range. Transferring the signal to a fixed-reference comparator using ac coupling produces poor results because changes in duty cycle cause variations in average signal level that result in jitter or distortion of the output signal's timing.

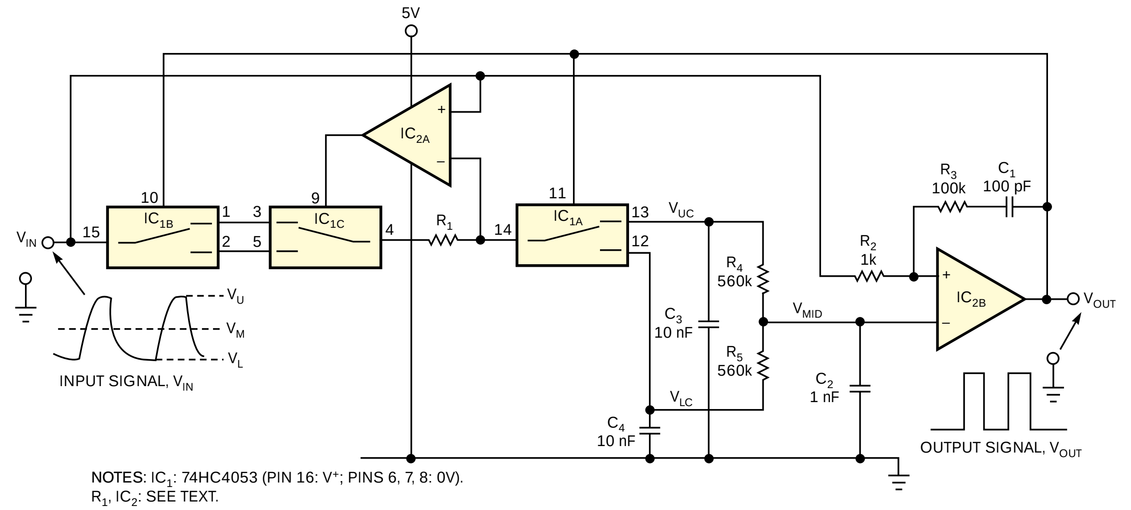
Based on diodes and RC networks, an envelope tracker creates a voltage between the input signal's excursions (**Reference** 1). Using the midpoint voltage as a reference, the comparator generates a digital output signal that faithfully replicates the original signal's timing information. Although highly effective for relatively large signals, a diode-based circuit can introduce errors or even fail completely for inputs that are small relative to a diode forward-voltage drop or when the input's average level drifts toward either of the circuit's supply-voltage rails.

Requiring no diodes, the single-supply circuit in **Figure** 1 reconstructs a band-limited NRZ data stream whose duty cycle can vary from less than 5% to more than 95% and whose amplitude varies from less than 100 mV to the supply-rail voltage—5V, for example. Furthermore, the circuit tolerates an average signal level that falls between the two supply rails. The circuit comprises triple analog switch IC_1, dual comparator IC_2, and a few passive components.

The circuit functions as a self-clocking envelope tracker by sampling the input signal's upper and lower levels, V_U and V_L, and generating corresponding dc levels, V_{UC} and V_{LC}, on capacitors C_3 and C_4. Two equal-valued resistors, R_4 and R_5, between C_3 and C_4, produce a third voltage, V_{MID}, that's equivalent to the input signal's midlevel voltage, V_M. Capacitor C_2 smoothes and filters V_{MID}, which serves as a reference potential for output comparator IC_{2B}. R_2, R_3, and C_1 provide temporal hysteresis, ensuring clean switching of V_{OUT}, even for relatively small inputs.

To understand the circuit's operation, assume that C_4, C_2, and C_3 all discharge; that is, V_{LC}, V_{MID}, and V_{UC} are all 0V. Because input signal V_{IN} is greater than V_{MID} and the potential at IC_{2A}'s inverting input, both comparators' outputs go high and cause the three analog switches to assume the positions in **Figure** 1. Now, assume that V_{IN} is at its positive peak amplitude, V_U. Capacitor C_3 now charges through R_1 and the on-resistances of the three switches. Provided that C_3 is not too large, V_{UC} rapidly acquires a value roughly equal to V_U.

When V_{IN} falls below V_{UC}, comparator IC_{2A}'s output goes low and



NOTES: IC_1: 74HC4053 (PIN 16: V^+; PINS 6, 7, 8: 0V).
R_1, IC_2: SEE TEXT.

Figure 1 This circuit tracks an NRZ signal's envelope excursions and recovers the original waveform.

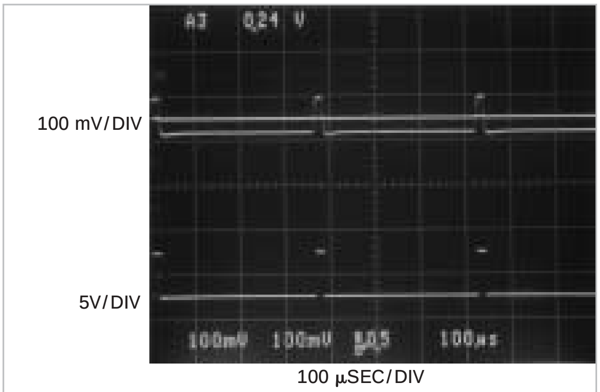


Figure 2 The lower trace shows the envelope tracker's response to a bandwidth-limited, low-duty-cycle, low-amplitude input signal. The horizontal line in the upper trace shows the signals' recovered midpoint voltage, V_{MID}.

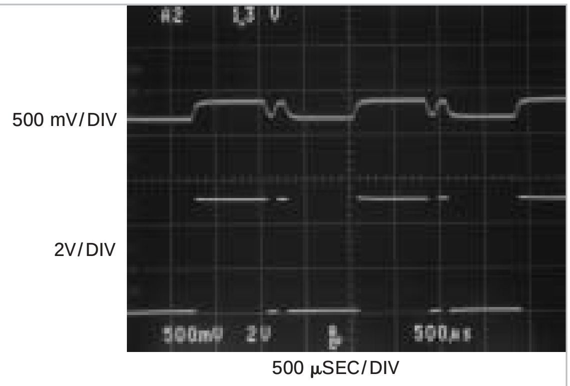


Figure 3 The lower trace shows the envelope tracker's output signal recovered from an inductively coupled data transceiver.

forces analog switch IC_{1C} to change state and disconnect C_3 from V_{IN}. Ignoring comparator input-bias currents and assuming negligible switch-leakage currents, C_3 can now discharge only through R_4. If R_4 is large enough, the relatively slow discharge rate allows V_{UC} to remain roughly equal to V_U.

During C_3's charging interval, C_2 also charges through R_4. Depending on the values of C_2 and R_4 and on the duration of the input signal's positive-going pulse, voltage V_{MID} may exceed the input signal's lower level, V_L. If V_{MID} exceeds V_L, comparator IC_{2B} trips when V_{IN} approaches V_L, and the resulting low level at V_{OUT} causes both IC_{1A} and IC_{1B} to change state. Capacitor C_4 now connects to V_{IN} through R_1 and the switches' on-resistances and quickly charges to a level at which V_{LC} approximately equals V_L.

Depending on component values and on the input signal's timing parameters, several cycles may elapse before the circuit's voltage levels stabilize at their quiescent values, at which $V_{UC} \approx V_U$, $V_{LC} \approx V_L$, and $V_{MID} \approx V_M$. However, careful selection of components ensures that the circuit rapidly reaches equilibrium. Ensuring that the comparator trips properly when V_{IN} goes below V_U or above V_L requires that R_1 provide a minimum amount of impedance of 100Ω to 1 kΩ between V_{IN} and IC_{2A}'s inverting input. Higher values result in sluggish charging of C_4 and C_3. In many designs, the combined on-resistances of IC_{1B} and IC_{1C} may allow omission of R_1.

The presence of IC_{1B}, IC_{1C}, and IC_{2A} ensures that C_3 can charge when V_{IN} is close or equal to V_U and that C_4 can charge only when V_{IN} is close or equal to V_L. Without IC_{1B}, IC_{1C}, and IC_{2A}—that is, with V_{IN} connected directly to R_1—C_3 would discharge on the downward slope of V_{IN} between V_U and V_M

and would thus pull down V_{UC}. Similarly, C_4 would continue to charge on the upward slope of V_{IN} between V_L and V_M and would thus pull up V_{LC}. Although V_{MID} might be roughly equal to V_M, such a minimal configuration performs relatively poorly, particularly for small signals and at extreme duty cycles.

The components in **Figure 1** produce good results for input frequencies of 5 to 50 kHz. Frequencies lower than 5 kHz may require larger capacitor values, and operation higher than 50 kHz may require reduction of capacitors' values and selection of a comparator with minimal response time. With properly selected components, the circuit performs well at baud rates to or exceeding 128 kbps.

The values of R_5, R_4, C_2, and, to a lesser extent, the analog switches' on-resistance and R_1, C_4, and C_3 determine the circuit's response time to a sudden change in input-signal amplitude or average level. Making C_2 approximately 10 times smaller than C_4 and C_3 ensures a rapid "attack" time, but too small a value can result in excessive ripple and noise on V_{MID}. For reliable operation, use equal values of close-tolerance resistors of 100 kΩ to 1 MΩ for R_4 and R_5. If you use high-value resistors for R_4 and R_5, choose a comparator with low input-bias currents for IC_2. For detection of signals that might approach the positive-supply rail, the 0V rail, or both, make sure that IC_2 offers rail-to-rail input capability. Bypass each IC's power-supply connections with low-impedance ceramic capacitors.

Note that, with no input signal present (that is, when applying a dc level to V_{IN}) V_{OUT} may contain random pulses caused by noise and the comparators' attempts at maintaining V_{MID} equal to V_{IN}'s average dc level. To eliminate the pulses, remove C_1 to replace temporal hysteresis with "normal" hysteresis, but ensure that the hysteresis levels that R_2 and R_3 set are not excessively large relative to the minimum input-signal amplitude.

Figure 2 shows the circuit's response to a bandwidth-limited input signal of approximately 5% duty cycle and 75-mV amplitude. The horizontal trace, V_{MID}, neatly bisects the waveform. The bottom trace shows the reconstructed signal at V_{OUT}. In **Figure 3**, the circuit processes the real-world output of an inductively coupled transceiver (upper trace) of approximately 200 mV p-p. Again, the lower trace shows the reconstructed signal at V_{OUT}. EDN

REFERENCE

1 Whipple, Roger C, "Envelope tracker quells jitter," *EDN*, July 7, 1994, pg 102, www.edn.com/archives/1994/070794/14di8.htm.

Hartley oscillator requires no coupled inductors

Jim McLucas, Longmont, CO

Examine a traditional Hartley-oscillator circuit, and you'll note its trademark: a tapped inductor that determines the frequency of oscillation and provides oscillation-sustaining feedback. Although you can easily calculate the total inductance for a given frequency, finding the coupling coefficient, k, may require experimental, or "cut-and-try," optimization. This Design Idea presents an alternative equivalent circuit that allows you to model the circuit before building the prototype.

Figures 1a and **b** show the Hartley oscillator's equivalent tuned circuit, the equations that calculate its components, and component values for an 18-MHz oscillator. The mutual inductance is $L_M=k\sqrt{L_1\times L_2}$. For the equivalent circuit, the equations are: $L_A=-L_M$, $L_B=L_2-L_A=L_2+L_M$, and $L_C=L_1-L_A=L_1+L_M$. The rest of the equations for the equivalent circuit are:

$$C_A=-\frac{1}{(2\pi f_O)^2 L_A},$$

$$f_O=\frac{1}{2\pi\sqrt{(L_B+L_C)C}},$$

and

$$C_A=\frac{1}{(2\pi f_O)^2 k\sqrt{L_1\times L_2}}.$$

Unfortunately, a truly equivalent circuit requires a negative inductance, L_A.

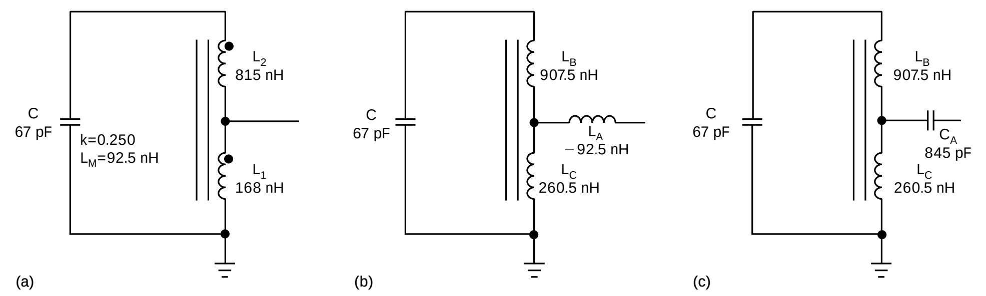


Figure 1 A traditional Hartley oscillator's resonant circuit comprises a tapped inductor and resonating capacitor (a). Allowing for mutual coupling between windings produces an equivalent circuit containing a negative inductance (b). Replacing the negative inductance with a capacitor yields an easily modeled equivalent circuit (c).

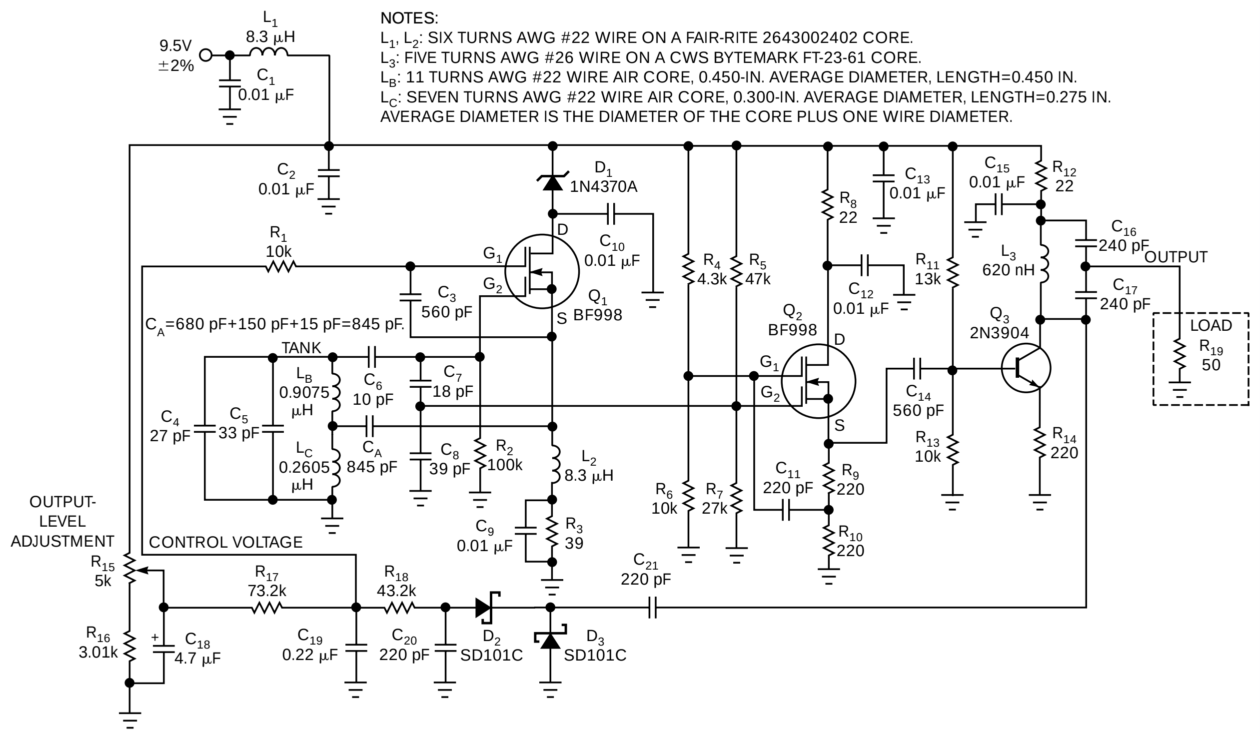


Figure 2 This buffered-output, 18-MHz oscillator has a resonant circuit that doesn't rely on mutual coupling for operation.

However, for frequencies near the resonant frequency, f_0, you can replace the negative inductor with a capacitor, in which C_A replaces L_A (Figure 1c). Note that the equivalent circuit's derivation neglects parasitic winding resistances and capacitances.

Figure 2 illustrates an oscillator and output buffer using the equivalent circuit. The constructed circuit generally performs as you would expect from an initial Spice simulation. During testing, several components' values required tweaking, and multiple iterations of Spice analysis ultimately yielded the final design. The oscillator's tank circuit comprises L_B, L_C, C_4, and C_5, plus capacitance provided by voltage divider C_6, C_7, and C_8. This capacitance of approximately 6 pF includes Q_1's and Q_2's input capacitances and some stray capacitance. The total tank capacitance of 66 pF approximates the calculated value of 67 pF. Capacitors that connect to the tuned circuit feature ceramic-dielectric construction with NP0 temperature coefficients.

Inductors L_B and L_C comprise air-core coils with their axes at right angles to each other to minimize stray coupling. However, vibration affects their inductances, and, in a final design, both should comprise windings on dielectric or toroidal cores, providing that the toroids' temperature coefficients of inductance are acceptable for the intended application. Reference 1 provides basic designs for both inductors, and adjusting the spacing of their turns tunes the oscillator to exactly 18 MHz. For a more rigorous design, you can measure the inductors before installation, but parasitic effects may require readjusting the inductors' values.

The capacitive voltage divider comprising C_6, C_7, and C_8 applies the proper signal levels to Q_1 and Q_2. Because the divider "sees" the tank circuit's effective capacitance as only 6 pF, the remaining 60 pF can comprise a variable capacitor if the design calls for a tunable oscillator. In this example, the output stage comprising Q_3 and its associated components would require modification to provide more bandwidth if the oscillator requires a tuning range exceeding ±2 MHz.

Capacitor C_3 bootstraps Q_1's Gate 2 to Q_1's source to provide additional gain from Q_1 and to reduce its Gate 1 input capacitance below its value of approximately 2.1 pF (Reference 2). An 8.3-μH inductor, L_2, connects to Q_1's source and presents relatively high impedance at 18 MHz and provides a dc path from Q_1's source to ground through R_3. The impedance of L_2 at 18 MHz comprises an inductive reactance of about 940Ω in parallel with a resistance of approximately 3.5 kΩ, which results in a choke with low resistive losses. You can substitute a smaller inductor for L_2 provided that its inductance and reactance approximate the original's values. You can use a standard-value 8.2-μH choke for L_2 provided that its resistive losses meet these low-loss criteria and that its inherent series resistance is 2Ω or lower to avoid upsetting Q_1's dc bias voltage. The inductance and resonance of the choke for L_1 are less critical than those for L_2, but using a choke with low resistive losses at L_1 helps avoid spurious resonances.

Source follower Q_2 drives the output stage, which uses a pi-matching network to transform the 50Ω output load to 285Ω at Q_3's collector. Bootstrapping Q_2's Gate 2 by one-half of its output voltage increases the source follower's gain and dynamic range and reduces its input capacitance. Potentiometer R_5 adjusts the circuit's output level from about 0.9V p-p to approximately 1.5V p-p across a 50Ω load. The circuit's frequency remains stable at a constant room temperature of about 23°C. Also, the output-level-control circuit remains stable even if you apply no load to the output. For a fixed-frequency oscillator, the output circuit's loaded resistive losses of approximately 4 provide adequate bandwidth without retuning L_3, C_{16}, and C_{17}.

To set the output level to a safe maximum, connect a 50Ω load to the output and adjust the output to 1.5V p-p. The drain-to-source voltage you apply to Q_1 remains at a safe level for all loads from 50Ω to no load, even though the output-voltage level increases as the load resistance increases. To avoid exceeding Q_1's specified maximum 12V drain-to-source voltage, do not exceed an output-voltage setting of 1.5V into a 50Ω load. Note that zener diode D_1 reduces Q_1's drain voltage to provide an additional safety margin.

In a previous Design Idea, an operational amplifier and a diode-rectifier circuit control the oscillator's gain by applying a variable voltage to Q_1's Gate 2 (**Reference 3**). In this design, a simple passive circuit serves the same purpose. A portion of the signal at Q_3's collector drives a voltage doubler comprising D_2, D_3, C_{20}, and C_{21}. The voltage doubler develops a negative voltage, part of which drives the junction of R_{18} and C_{19}, the control-voltage node. This control-voltage node also receives a positive voltage through R_{17} from variable resistor R_{15}, and the resultant voltage sets the output-signal level. At start-up, only a positive voltage is present at Q_1's Gate 2, and Q_1's maximum gain easily starts the oscillator. When the output reaches steady state, the control voltage decreases and maintains oscillation at a signal level that the output-level control determines.EDN

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3 McLucas, Jim, "Stable, 18-MHz oscillator features automatic level control, clean-sine-wave output," *EDN*, June 23, 2005, pg 82, www.edn.com/article/CA608156.