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READERS SOLVE DESIGN PROBLEMS

Error compensation improves bipolar-current sinks

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You can improve a current sink's accuracy by at least two orders of magnitude by adding two standard 1%-tolerance resistors. As a bonus, you also compensate for errors that a low-current-gain pass transistor's base current introduces. To do so, you measure the transistor's base current and add a proportionally scaled error term to the source's reference voltage. When you design a current sink, you can use a MOSFET for the sink's pass transistor because of its nearly infinite power gain and low gate current. However, a high-power MOSFET presents high input and output capacitances that reduce the sink's high-frequency output impedance.

As an alternative, a low-current-gain, bipolar power transistor presents a much lower output capacitance than does a MOSFET of comparable power ratings. **Figure 1** shows a design for a bipolar-transistor-based current sink that unfortunately suffers from accuracy errors due to Q_1's base current's flowing into the current-measurement resistor R_1. The base current varies with changes in Q_1's collector current and current gain, which in turn depend on Q_1's production tolerances, junction temperature, and collector-emitter voltage.

You can use a Darlington transistor to increase the circuit's current gain and reduce the output error, but few Darlington transistors offer good high-frequency parameters. Superbeta power transistors are rare, have typically lower unity-gain-bandwidth frequencies, and are more expensive. In other words, even though a bipolar transistor presents higher output impedance at high frequencies, the error from its base current makes it a poor choice for a high-precision current sink. You could compensate for base-current errors by measuring the output transistor's collector current and introducing a correction factor, but that approach increases circuit complexity and reduces the sink's output impedance.

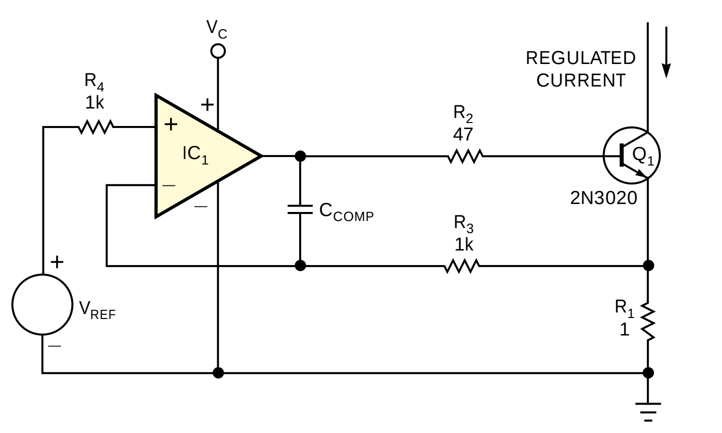

Figure 1 This typical quickly responding constant-current sink uses a bipolar transistor but suffers from base-current-induced error. Its nominal output current is $I_{OUT}=(V_{REF}/R_1)-I_B$.

Figure 2 shows a better approach, which adds a differential amplifier, IC_2, and resistors R_6 through R_9 to measure Q_1's base current by sampling the voltage across R_2. Resistors R_4 and R_5 scale and sum the error and reference voltages you apply to differential amplifier IC_1. Because IC_1's inverting input connects to current-shunt resistor R_1's upper end and not to ground, the reference voltage, V_{REF}, determines the error voltage applied to Q_1, preserving output scaling and allowing output-current calculation as V_{REF}/R_1. As a result, the regulated voltage across R_1 represents the sum of the desired output current plus the transistor's base current. Because the transistor inherently "subtracts" its base current, its collector current and, hence, the output current have no base-current error.

You can simplify the circuit and preserve its error-correction properties by combining IC_1 and IC_2; better yet, you can add two resistors to **Figure 1** to

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achieve the same effect. Figure 3 shows the final circuit. To understand its operation, think of the circuit as a voltage regulator that delivers a voltage equal to V_{REF} across R_1. If you short-circuit base resistor R_2, note that any common-mode error that resistors R_5 and R_6 introduce cancels and thus has no effect on Q_1's base voltage. When you feed the voltage drop back to IC_1's input through R_5 and R_4, the voltage drop across R_2, representing Q_1's base current, increases the regulated voltage across R_1 by the ratio of R_5/R_4. If the ratio of R_5/R_4 equals that of R_2/R_1, the voltage across R_1 includes an error term that effectively cancels the base current. If $R_3=R_4$ and $R_5=R_6$, the following equation describes the output current, I_{OUT}:

$$I_{OUT}=\frac{V_{REF}+I_B\times R_2\times\frac{R_4}{R_5}}{R_1}-I_B.$$

Because the base current, I_B, appears twice with opposite signs and cancels, the equation simplifies to: $I_{OUT}=(V_{REF}/R_1)$.

To optimize the circuit's performance, use the following resistor ratios: $R_2/R_1=R_5/R_4$, $R_5=R_6$, $R_3=R_4$, $R_5>>R_4$, and $R_3>>R_1$. Using standard 1%-tolerance resistors in the circuit of Figure 3 reduces the error from Q_1's base current to about one-one-hundredth of its uncompensated level. Without compensation, a low-gain power transistor with a typical current gain of 25 at Q_1 would introduce a full-scale current error of 4%. The circuit corrects the error to 0.04% and raises Q_1's current gain to an effective current gain of 2500. Perfect matching would result in an immeasurably small base-current error. Note that IC_1's input common-mode-voltage range must include the negative-supply-voltage rail. Equal resistances at both of IC_1's inputs balance the op amp's input-bias currents. The minimum power-supply voltage depends on IC_1's maximum current-sourcing capability and on the sum of the worst-case voltage drops across Q_1's base-emitter junction, R_1 and R_2. The circuit's maximum output current depends on Q_1's worst-case minimum current gain times IC_1's worst-case minimum output current.

To ensure stable operation, use a unity-gain-stable op amp for IC_1. When the circuit operates within its nominal current range, an op amp whose response time is substantially

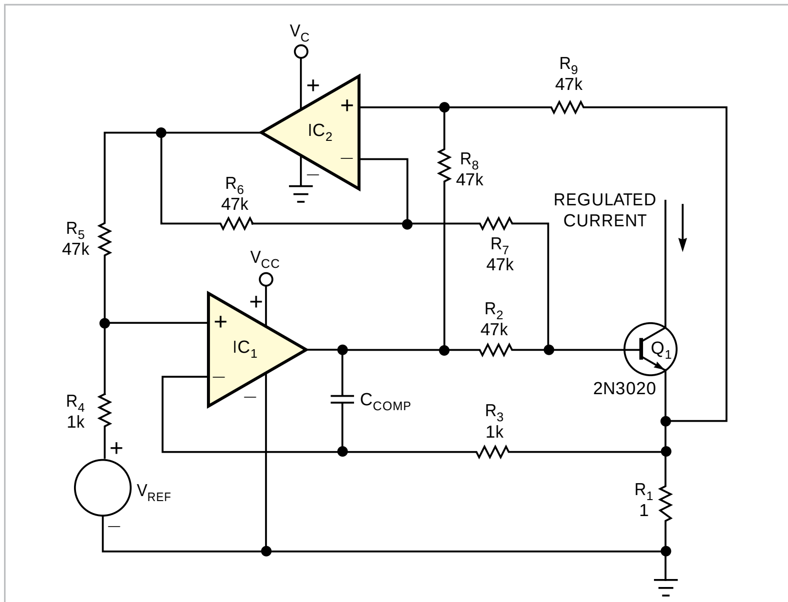

Figure 2 Adding base-current error compensation improves the circuit's performance. Using perfectly matched resistors simplifies the output-current equation to $I_{OUT}=(V_{REF}/R_1)$.

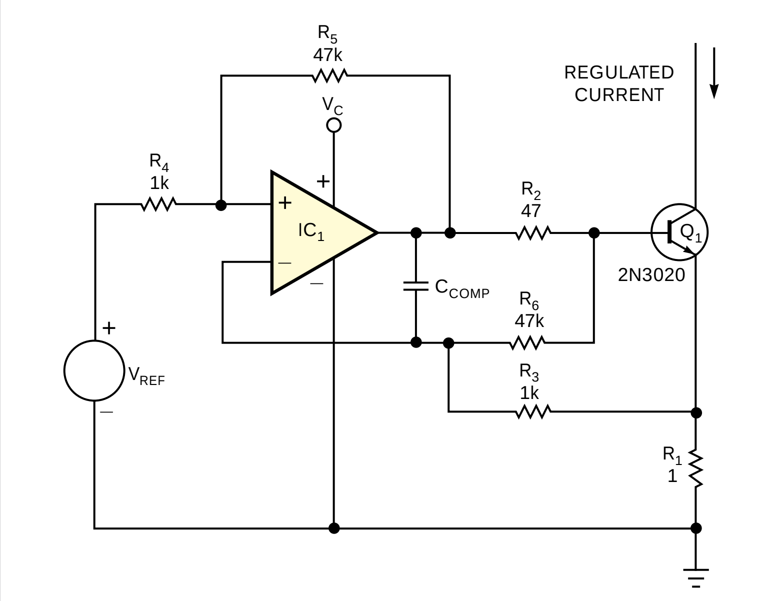

Figure 3 You can further simplify the current sink's design by adding only two resistors, R_5 and R_6, to the original in Figure 1. The output-current equation remains $I_{OUT}=(V_{REF}/R_1)$, as in Figure 2.

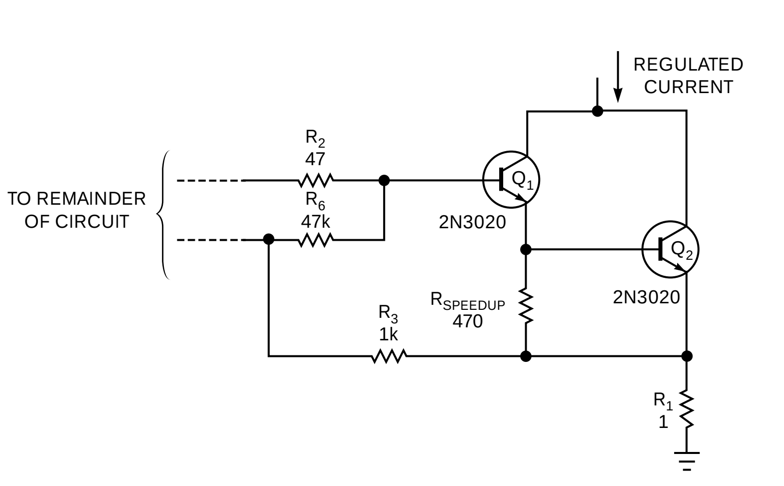

Figure 4 Adding $R_{SPEEDUP}$ improves the performance of a two-transistor Darlington output stage.

longer than Q_1's generally doesn't require installation of compensation capacitor C_{COMP}. However, a small capacitor of a few tens of picofarads guarantees stability under all conditions—for example, when the circuit's output current and the feedback voltage across R_1 approach zero.

The circuit in **Figure 3** works equally well if you use a Darlington transistor for Q_1 because its higher current gain further improves the circuit's operation. If you use two discrete bipolar transistors, you can improve the composite Darlington transistor's turn-off time by connecting a resistor between the output transistor's base and emitter to remove its excess base charge (**Figure 4**).

You can use either a fixed or an adjustable reference-voltage source, but for the smallest possible error, the reference source's output impedance should be fairly low to sink feedback current from R_4. You can also proportionally increase the values of resistors R_3 through R_6 to reduce the amount of current that the reference source absorbs. It's amazing what you can achieve by adding only two resistors to an already-simple circuit. EDN

Phase-sequence indicator uses few passive components

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In a three-phase ac system, a power source with three wires delivers ac potentials of equal frequency and amplitudes with respect to a zero-potential wire, each shifted in phase by 120° from one wire to the next. Two possibilities exist for establishing a phase sequence. In the first, voltage on the second wire shifts by 120° relative to the first, and, in the second, a −120° shift occurs with respect to the first wire. Phase order determines the direction of rotation of three-phase ac motors and affects other equipment that requires the correct phase sequence: a positive 120° shift. You can use a few low-cost passive components to build a phase-sequence indicator.

Figure 1 shows a conceptual circuit that can detect both phase sequences. For certain component values, the following conditions apply: The voltages across R_1 and C_2 are equal—that is, their magnitudes and phases are the same—only when V_{S2} occurs exactly 120° ahead of V_{S1}, which indicates the correct phase sequence. In this case, the voltage between points A and B is zero. Conversely, the voltages across C_2 and R_3 are equal only when V_{S2} is ahead of V_{S3} by 120°, which corresponds to a reversed sequence.

Referring to the phasor diagram in **Figure 2**, when the voltages across R_1 and C_2 are equal, $V_{C1}=-V_{R2}$, $V_{C1}+V_{R1}=V_{S1}$, and $V_{C2}+V_{R2}=V_{S2}$. The following **equations** satisfy these conditions: $|V_{R1}|=|V_{C2}|=(1/2)|V_{S2}|=(1/2)|V_{S1}|$, and $|V_{C1}|=|V_{R2}|=\cos(30°)|V_{S1}|=\cos(30°)|V_{S2}|$. You calculate the component values by

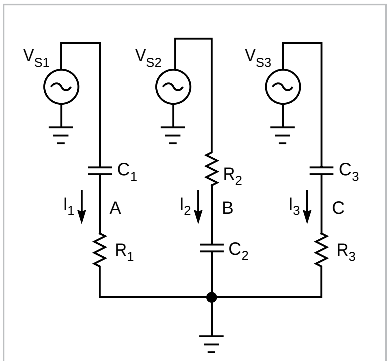

Figure 1 This conceptual circuit can detect both phase sequences.

solving the following **equations**: $|X_{C1}|=\tan(60°)\times R_1=\sqrt{3}\times R_1$, and $R_2=\tan(60°)\times|X_{C2}|$, where $X_C=-j[1/(2\pi\times f\times C)]$, and f represents the frequency of the V_S voltages.

Also, to ensure detection of a reversed phase sequence, $C_1=C_3$, and $R_1=R_3$; that is, the components in the

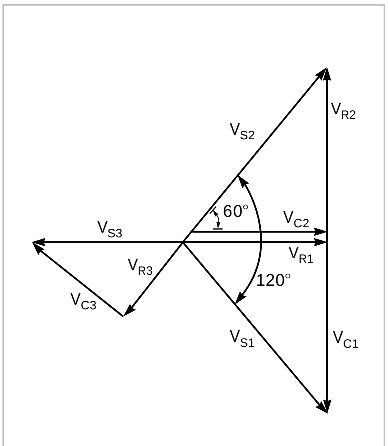

Figure 2 When the voltages across R_1 and C_2 are equal, $V_{C1}=-V_{R2}$, $V_{C1}+V_{R1}=V_{S1}$, and $V_{C2}+V_{R2}=V_{S2}$.

third branch are identical to those in the first branch. The phase-sequence-detection circuit in Figure 3 eliminates the requirement for an accessible ground wire by adding resistors R_4 and R_5 that connect in parallel with the first and third branches. Eliminating the ground-wire requirement also dictates a ratio between $|X_{C1}+R_1|$ and $|X_{C2}+R_2|$. For no current to flow to ground from Node G, the sum of currents in the branches must equal zero, and, if you disconnect Node G from ground, its potential with respect to ground is also zero.

As long as the proportions of X_{C1} to R_1, X_{C2} to R_2, and X_{C3} to R_3 remain as noted, the balance of voltage drops remains across R_1, C_2, and R_3. Multiplying the impedance of any branch by a constant influences only the magnitude of the currents through the respective branch. The current through any branch presents the same phase angle as the voltage across a resistor in the branch. The phasor diagram in Figure 4 shows the currents in Figure 3. From this diagram, if $|I_2|=\tan(60°)\times|I_1|$, then $I_1+I_2=-2\times I_3$. Thus, I_3 has half the magnitude of and an exactly opposite direction from (I_1+I_2).

A vector diagram of the currents shows that adding two currents, each with magnitudes equal to I_3 and the same phases as V_{S1} and V_{S3}, produces a summed current with the same magnitude and phase as I_3; therefore, the total current at Node G is zero: $I_1+I_2+I_3+I_1'+I_3'=I_1+I_2+2\times I_3=0$. To make the sum of the currents equal zero, $R_4=R_5=|R_1+X_{C1}|=|R_1-j[1/(2\pi\times f\times C_1)]|$. The two LEDs in Figure 3 indicate correct or reversed-phase sequence. When LED_2 lights and LED_1 remains dark, the voltage between nodes A and B is 0V, which corresponds to a correct phase sequence. A reversed-phase sequence lights LED_1 while LED_2 remains dark. The diodes connected in parallel with the LEDs protect against exceeding the LEDs' reverse-breakdown voltages, and resistors R_6 and R_7 limit forward currents through the LEDs. For greater sensitivity, you can replace the LEDs with high-input-impedance ac-detector circuits.

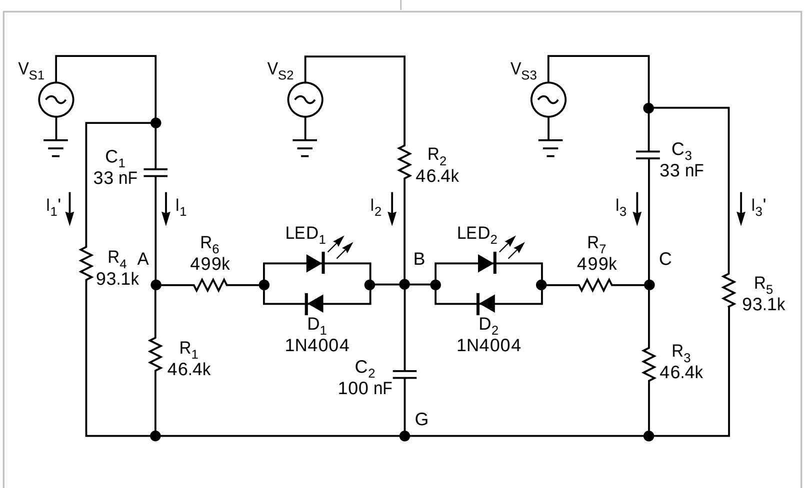

Figure 3 This phase-indicator circuit balances branch voltages and currents and requires no ground reference. These component values are for a 60-Hz line frequency.

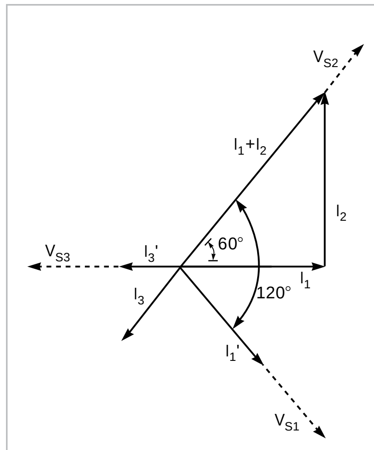

Figure 4 I_3 has half the magnitude and an exactly opposite direction to (I_1+I_2) in Figure 3.

The circuit's final version includes indicators that show whether all three phases carry voltage. In the circuit in Figure 3, a phase that carries 0V lights both LEDs. Depending on your application, you can connect voltage-detection circuits comprising LEDs and protection diodes in series with current-limiting resistors between V_{S1}, V_{S2}, and V_{S3} and Node G. You can also use low-wattage neon lamps with appropriate series-current-limiting resistors.

When selecting components, ensure that their values conform to the following proportions. For an arbitrarily chosen value for C_1, $R_1=R_2=R_3=1/(2\pi\times f\times C_1\times\tan(60°))$, $C_1=C_3$, $C_2=3C_1$, and $R_4=R_5=2\times R_1$. When you select a value for C_1, the currents through the detection circuitry should be significantly lower than the currents through the branches, which excludes arbitrarily low values for C_1. EDN

Microcontroller's single I/O-port line drives a bar-graph display

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Instrument designs featuring a digital display may benefit from a secondary display that provides an analog version of the displayed parameter. A bar-graph display provides an easily interpreted graphical indicator that allows comparison with its full-scale value, but a conventional microcontroller-based design uses at least one eight-line I/O port to drive an eight-segment-bar-graph LED display.

As an alternative, some microcontrollers include a PWM (pulse-width-modulated) output. You can minimize the number of required I/O lines by using the PWM output to drive National Semiconductor's (www.national.com) LM3914 bar-graph-display-driver circuit or an equivalent. In operation, the microcontroller's program adjusts the PWM output's pulse width such that the average voltage that feeds to the LM3914 circuit illuminates the required number of bars in the display.

The design in **Figure 1** obviates the shortcomings of these approaches and uses only one port line to drive an eight-segment bar graph. This design does not use a PWM output and hence can apply to any microcontroller. Referring to the timing diagram in **Figure 2**, whenever the bar-graph display requires an update, the microcontroller's software delivers a pulse train through its output port. The first pulse comprises a pulse of width T_1 that's longer than the width of the pulse T_2, which triggering monostable IC_1, a 74123 or equivalent, produces. You apply both pulses to IC_3, a 7400 or equivalent NAND gate, which together with IC_1 forms a long-pulse detector. Use the equation in IC_1's data sheet to select values for C_1 and R_1 that yield a value of approximately 1.5 msec for T_2's output pulse. Typical widths for T_1 and T_3 are 3 and 1 msec, respectively.

The output pulse from IC_3 goes low for a duration of T_1-T_2, and this pulse clears IC_2, an 8-bit serial-in parallel-out shift register, which forces all of IC_2's outputs to go low and lights all segments of the bar-graph array (LED_1 to LED_8).

To light N segments of the bar-graph array, the microcontroller immediately sends a serial train of (8−N) pulses of width T_3 through the output-port line. Because the width of these pulses is less than T_2, NAND gate IC_3's output always remains high and thus does not clear the shift register. The rising edge of each of the microcontroller's output pulses loads a high to one of IC_2's outputs.

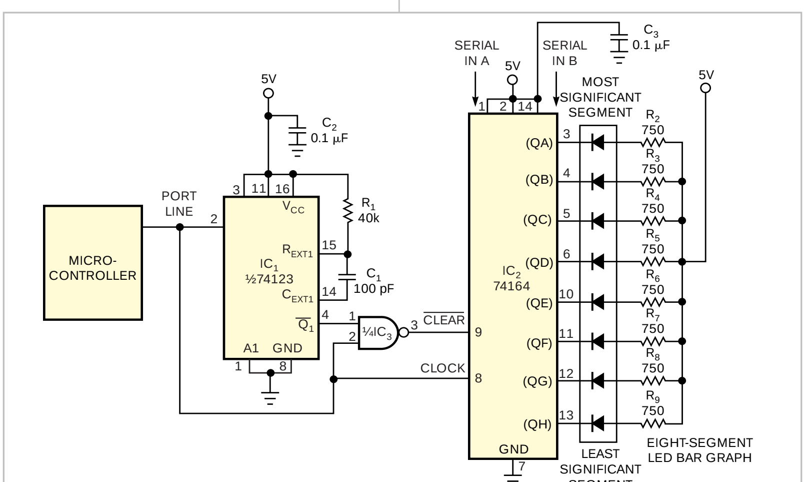

Figure 1 You can add a multisegment bar-graph display to a microcontroller that has only one output line.

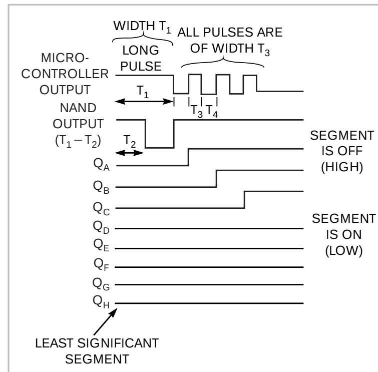

Figure 2 During the first pulse of the microcontroller's output-pulse sequence, the NAND gate's output clears the shift register and lights all of the display's segments.

Note that shift register IC_2's QA output connects to the bar graph's most significant segment. Hence, the first pulse switches off the most significant segment. Starting with the most significant segment, for (8−N) pulses, 8−N segments switch off, and N segments beginning with the least significant segment remain lighted. Using this reverse logic takes advantage of the shift register's outputs' ability to sink more current than they can source—8 versus 0.4 mA, respectively, and thus produce a brighter bar-graph display without adding output buffers. **Figure 2** shows a sample timing diagram that lights five of eight display segments.

If a second output-port line is available, you can omit using monostable multivibrator IC_1 and NAND gate IC_3 and use the second port to clear the shift register by outputting a zero whenever the bar graph requires an update. To obtain finer resolution, you can add segments to the bar graph by cascading additional shift registers. To light N segments of a display that is M segments long, the first output port sends M−N pulses to the shift register's clock input.

This design lends itself well to situations in which unused I/O-port lines are at a premium, as is the case for microcontrollers with reduced pin counts, or if you need to retrofit a bar-graph display by adding a daughterboard to a design. EDN