



BY JOSHUA ISRAELSOHN, CONTRIBUTING TECHNICAL EDITOR

Scaling: a balanced view, part three

In the last installment of Analog Domain, the application's matching, noise, and 1/f noise requirements determined the model minimum circuit's load capacitance, C_{MIN} —a representation of the following stage's input impedance. Matching varies in inverse proportion to $1/L_{\text{MIN}}$; noise and 1/f noise follow an inverse-square-law relationship with the minimum length (references 1 and 2).

For example, for applications in which matching constrains the dynamic range, such as track-and-hold amplifiers and several ADC architectures, you can express the offset voltage, V_{OS} , as

$$V_{\text{OS}} = \frac{n_{\sigma}\gamma T_{\text{OX}}}{\sqrt{WL}}$$

Here, n_{σ} is the number of sigmas that your company's yield model requires, γ is a process-dependent parameter, T_{OX} is the gate-oxide thickness, and W and L are the device width and length.

The gate capacitance, C_{GATE} , of the transistors that must meet the matching requirements is

$$C_{\text{GATE}} = \frac{\epsilon_0\epsilon_r WL}{T_{\text{OX}}}$$

where ϵ_0 is the permittivity of free space and ϵ_r is the relative permittivity of the gate oxide. Combining these two equations gives the C_{MIN} of the transistors that satisfies the matching requirements:

$$C_{\text{GATE}} = \epsilon_0\epsilon_r n_{\sigma}^2 \gamma^2 T_{\text{OX}} \frac{\text{DR}^2}{V_{\text{SIG(RMS)}}^2}$$

where DR is the application's matching-limited dynamic-range requirement. Due to the strong influence that matching requirements have on C_{MIN} and, as a result, dissipation, circuits that demand tight matching between large numbers of transistors often make use of circuit techniques, such as offset can-

cellation, that reduce the requirements for individual devices.

In applications for which white noise limits the dynamic range, including a broad class of small-signal amplifiers, converters, and filters,

$$V_{\text{NOISE}}^2 = \frac{kT}{C_{\text{NOISE}}}$$

though recent efforts suggest methods that beat this traditional floor. Expressing this limit as a minimum capacitance, with dynamic range as a parameter, yields

$$C_{\text{NOISE}} = kT \frac{\text{DR}^2}{V_{\text{SIG(RMS)}}^2}$$

After determining the load capacitance necessary to meet dynamic-range requirements, the next step is to calculate the current necessary to sufficiently drive this capacitance to meet the application's ac specifications—bandwidth, settling time, slew rate, and total harmonic distortion.

Fundamental to these measures is the MOSFET's transconductance, gm:

$$g_m = \frac{2I_D}{V_{\text{GT}}}$$

where $V_{\text{GT}} = V_{\text{GS}} - V_{\text{T}}$ in strong inversion and

$$V_{\text{GT}} = \frac{2nkT}{q}$$

in weak inversion. Bandwidth, the ratio

of the unity-gain frequency, F_0 , to the dc gain, A_0 , follows from the transconductance and gate capacitance:

$$\text{BANDWIDTH} = \frac{F_0}{A_0} = \frac{g_m}{2\pi A_0 C_{\text{GATE}}}$$

In certain applications, meeting the application's bandwidth requirements is not insufficient; designs must prevent slew-rate limiting, which can impose another requirement on the minimum current:

$$I_{\text{SR}} = 2\pi F_{\text{SIG}} V_{\text{SIG}} C_{\text{L}}$$

Similar equations describe the minimum current necessary to attain specific second- and third-harmonic-distortion levels with and without feedback. For these, refer to **Reference 2**.

As was the case with the voltage efficiency, the model requires an assumption of current efficiency, η_c . Given a differential-signal path—a practical departure from the single-transistor string under discussion thus far—and modest current scaling in the bias-current mirror, an η_c of one-third is a good, if somewhat conservative, starting assumption for current efficiency of a single stage. In practice, common circuit-design practices more efficiently distribute bias currents, but the precise number depends upon both bias-generator and signal-path-circuit topologies.

The sum of string currents—or, in the case of differential circuits, the half-circuit currents—multiplied by the current efficiency yields the supply current, I_{DD} . The product of supply current and supply voltage, which you calculated from the application's signal-swing requirements, results in the minimum power dissipation necessary to attain the originally stated parametric goals. EDN

REFERENCES

References are available at www.edn.com/060720ji.

Joshua Israelsohn is director, technical information at International Rectifier Corp. You can reach him at edn-joshua@mindspring.com.