Low-dropout regulator, SMPS cascade suppress ripple, maintain efficiency

Scot Lester, Texas Instruments, Dallas, TX

A step-down SMPS (switched-mode power supply) efficiently converts unregulated power to a regulated output voltage. However, unwanted switching-induced ripple and input transients may appear on the output. Applying noisy power to an RF power amplifier can inject spurious signals or modulated noise into the broadcast spectrum. Analog- and RF-system engineers favor traditional low-noise power-supply designs that comprise a transformer, rectifier, and filter followed by a linear voltage regulator. A low-dropout linear regulator's low output noise and high PSRR (power-supply rejection ratio) ensure clean power that imposes no interference on a power amplifier's output.

Unfortunately, a transformer-and-rectifier power supply delivers a fluctuating output voltage that depends on its input voltage. As the difference between its input and output voltage increases, a low-dropout regulator's efficiency decreases, and its power dissipation increases. To remain in regulation at low ac-line voltages, even a low-dropout regulator requires a certain amount of head-room input-to-output voltage.

To overcome the disadvantages inherent in both circuits, you can use an SMPS to maintain high efficiency and a low-dropout regulator to reduce the output noise and ripple voltage of the SMPS. Setting the output voltage of the SMPS slightly higher than the low-dropout regulator's minimum dropout voltage reduces the regulator's power dissipation, accommodates the voltage margin you need for good switching-noise rejection, and maintains high efficiency. The regulators' PSRRs add, and the combined circuits' PSRR exceeds that of either the regulator or the SMPS alone.

Figure 1 shows a cascade circuit comprising an SMPS followed by a linear regulator. This circuit's output voltage ranges from 1.5 to 5V at an output cur-

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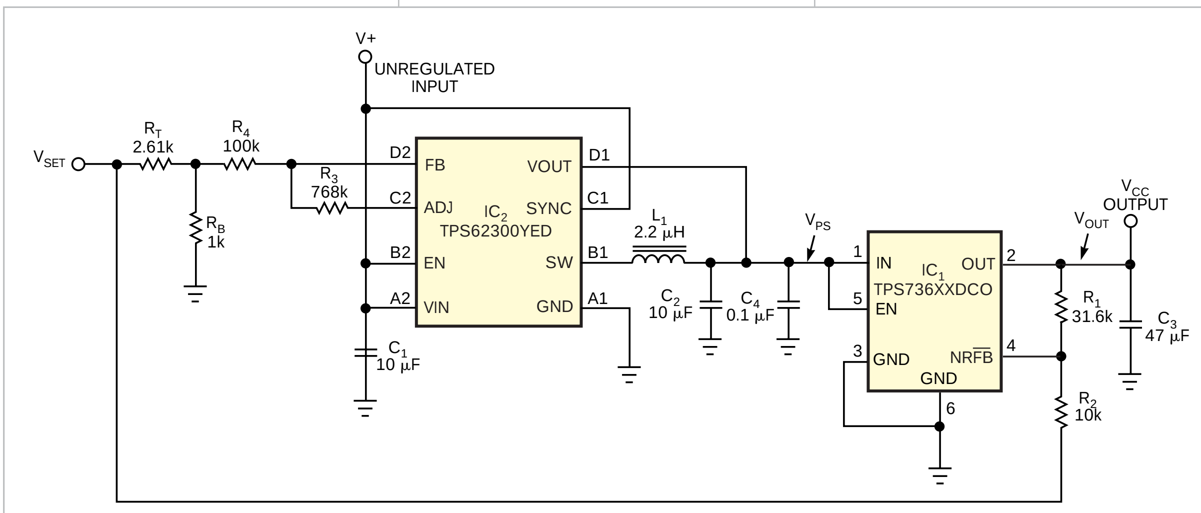

Figure 1 Connected in cascade, a low-dropout linear regulator and a switched-mode power supply improve output-voltage ripple and maintain overall efficiency. (Note: In IC_1's part designation, "XX" represents the regulator's output voltage.)

rent as high as 400 mA. Although a fixed 6V supply powers the cascaded circuit, its design accommodates any input voltage at least 0.5V higher than the cascaded pair's desired output voltage.

Adjusting the reference voltage, V_{SET}, over 0 to 1.105V linearly varies the circuit's output voltage. Resistors R_1 and R_2 and reference voltage V_{SET} determine the low-dropout regulator's output voltage and thus the cascaded pair's output voltage. Resistors R_T, R_B, R_3, and R_4 divide V_{SET} to maintain the SMPS' output voltage, V_{PS}, at a constant 0.2V higher than the regulator's output voltage, reducing the regulator's power dissipation to 80 mW at full output current and any output voltage.

At its maximum output current of 400 mA, the cascaded supply reaches a maximum efficiency of 89% with a 6V input and a 4.69V output (**Figure 2**). The overall efficiency decreases as the output voltage decreases. **Figure 3** compares the PSRRs of the SMPS alone and of the SMPS cascaded with the regulator, which improves PSRR by 46 dB at 500 Hz—essentially that of the regulator alone at 500 Hz.

Over a frequency range of 100 Hz to 100 kHz, the low-dropout regulator improves PSRR by at least 25 dB (Figure 3). Circuit-layout and -measurement techniques compound the difficulty of making accurate small-signal measurements, and the graph's PSRR values may not appear additive. The linear regulator governs the circuit's switched-load transient response, which may represent an improvement over the response of the SMPS. However, the cascade circuit's low output ripple and high efficiency make the circuit well worth investigation. EDN

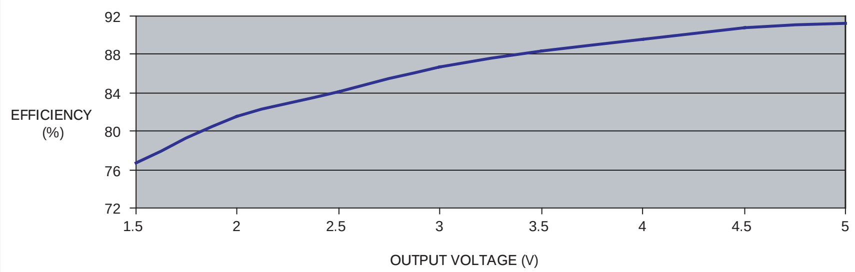

Figure 2 The regulator cascade's combined efficiency improves as the unregulated output voltage increases.

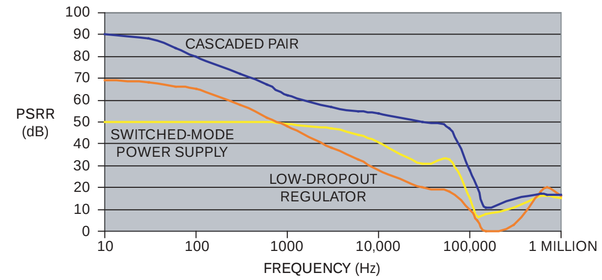

Figure 3 The power-supply rejection ratio improves significantly (blue trace) when you cascade switched-mode (yellow trace) and linear (red trace) voltage regulators.

Novel circuit isolates temperature sensor from its host

Alfredo H Saab and Tamer Mogannam,
Maxim Integrated Products Inc, Sunnyvale, CA

Temperature sensors must sometimes operate at locations whose return potentials differ considerably from that of the data-acquisition system's common—that is, equipotential—ground. In consequence, the temperature sensor's support circuitry must provide galvanic isolation between the sensor and its data-acquisition system. Also, the data-acquisition system seldom provides an isolated source of power for the sensor. The circuit in **Figure 1** solves both problems by isolating the sensor's signal and power supply.

The complementary, fixed-frequency square-wave outputs of a power-transformer driver—IC_1, a Maxim (www.maxim-ic.com) MAX845—drive a Halo Electronics (www.haloelectronics.com) TGM-010P3 1-to-1-to-1 transformer with dual primary windings and a single untapped secondary winding (**Reference 1**). The secondary winding feeds a Graetz-bridge rectifier that generates approximately 4.5V to power IC_2, a Maxim MAX6576 sensor. Combining a temperature sensor, signal-processing electronics, and an easy-to-use digital-I/O interface in a low-cost package, the MAX6576 draws little current from a single supply source and maintains its specified accuracy over a 3 to 5V supply-voltage range.

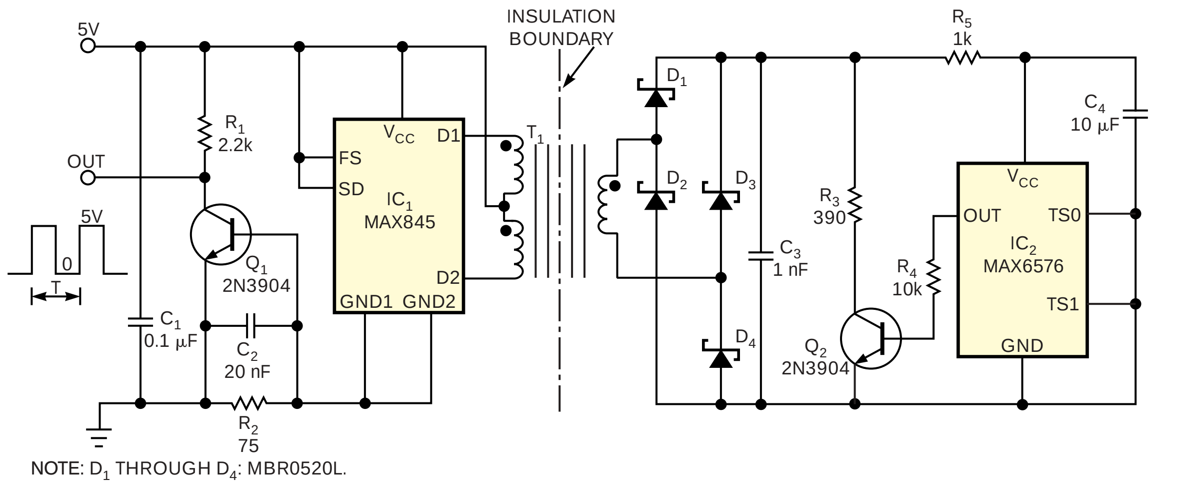

Figure 1 Transformer T_1 isolates the temperature sensor, IC_2, from the equipment under test. The period of IC_1's digital output varies as a function of temperature. The circuit's output period varies at a rate of 10 µsec/°K. User-selected scale factors range from 10 to 640 µsec/°K.

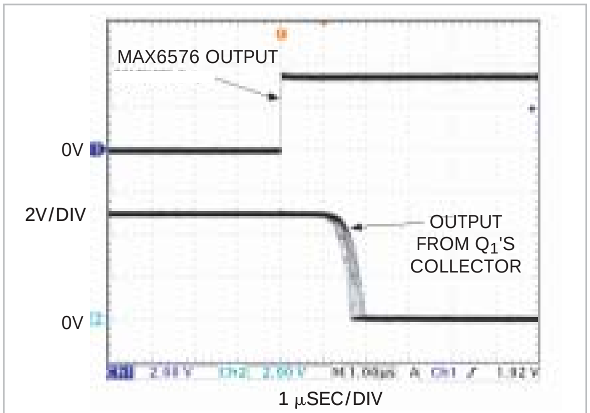

Figure 2 Measured from the positive-going edge of IC_2's output to the circuit's output at Q_1's collector, the relative jitter averages less than 1 µsec.

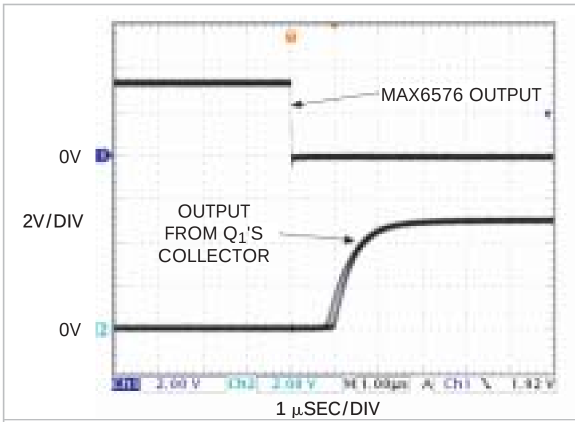

Figure 3 As in Figure 2, Q_1's average output jitter with respect to IC_1's negative-going output also averages less than 1 µsec.

If you connect the sensor as **Figure 1** shows, it operates as an absolute temperature-to-period converter and provides a nominal conversion constant of 10 µsec/°K, which, at room temperature, yields a period of approximately 2.980 msec—a frequency of 335 Hz. You can adjust the conversion constant from 10 to 640 µsec/°K. Note that longer conversion constants allow more signal-integration time to minimize noise effects. The sensor's symmetrical square-wave output drives NPN transistor Q_2's base through R_4, a 10-kΩ resistor. A 390Ω resistor, R_3, serves as Q_2's collector load and connects to the same lines that deliver power to the temperature sensor. When Q_2 conducts, it draws an asymmetrical power-supply current that exceeds the supply current during the sensor output's positive half-cycle.

In IC_1's sensor output-to-ground return on the data-acquisition system's side, resistor R_2 and capacitor C_2 shunt Q_1's base-emitter junction. The values of R_2 and C_2 ensure that the sum of IC_2's current and transformer T_1's magnetizing current cannot drive Q_1 into conduction. When Q_2 conducts, it draws about 12 mA from the isolated 4.5V power-supply line. Reflecting to the primary, Q_2's conduction current flows from the 5V supply into IC_1, out through its ground terminals, and partly through R_2. The voltage drop across R_2 exceeds Q_1's base-emitter voltage threshold and supplies sufficient base current to turn on Q_1.

Thus, when Q_2 conducts, so does Q_1, which copies IC_1's isolated square-wave output to Q_1's collector circuit. As the waveforms of **figures 2** and **3** show, Q_1's output rise and fall times, jitter, and propagation delay total about 2 µsec. The equivalent measurement error due to timing jitter amounts to less than 0.1°K at the fastest conversion constant of 10 µsec/°K. Varying the circuit's supply voltage through a range of 4.5 to 5.5V introduces an error of less than 0.1°K. The output at Q_1's collector can sink several milliamperes at a voltage excursion of 0 to 5V.

This design can accommodate temperature-to-frequency converters and other types of temperature sensors. For further information on IC_1 and IC_2, review the devices' data sheets and the data sheet for the MAX845 evaluation kit (references 2, 3, and 4). EDN

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Find resistor values for arbitrary programmable-amplifier gains

Sid Levingston, DML Engineering Inc, Aloha, OR

When available fixed-gain values match design requirements, a PGA (programmable-gain-amplifier) IC offers a drop-in choice, but what does a designer do when a suitable PGA is unavailable? Before the PGA's advent, a circuit designer who needed selectable, fixed amounts of gain chose a suitable operational amplifier and designed a switched-resistor gain-setting network. This Design Idea discusses two methods of designing the desired resistive network.

Figure 1 shows a series-ladder-resistor network comprising a string of resistors whose junctions connect to switch-selectable taps that determine the circuit's gain. Little current flows through the switch, and the resistance of the switch thus doesn't affect the design. A circuit with N discrete-gain values requires an N-position switch, usually an analog multiplexer, and N+1 resistors in its ladder. Equation 1 describes the circuit's gain in the general case:

$$\text{GAIN}[n] = \frac{\sum_{i=1}^{n} R_i}{\sum_{i=n+1}^{N+1} R_i} + 1. \quad (1)$$

You can solve Equation 1 for the resistor summations and expand a few terms as follows:

$$\frac{\sum_{i=1}^{n} R_i}{\sum_{i=n+1}^{N+1} R_i} = \text{GAIN}[n]-1. \quad (2)$$

$$\sum_{i=1}^{n} R_i = (\text{GAIN}[n]-1) \times \sum_{i=n+1}^{N+1} R_i. \quad (3)$$

$$R_1 = (\text{GAIN}[1]-1) \times (R_2 + R_3 + ... + R_{N+1}), \quad (4)$$

$$R_1 + R_2 = (\text{GAIN}[2]-1) \times (R_3 + ... + R_{N+1}), \quad (5)$$

and

$$R_1 + R_2 + R_3 + ... + R_N = (\text{GAIN}[N]-1) \times (R_{N+1}). \quad (6)$$

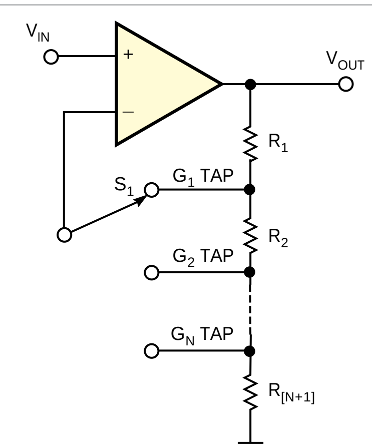

Figure 1 A series-resistor-ladder network and a single-pole, multiple-throw switch form a custom-value programmable-gain amplifier.

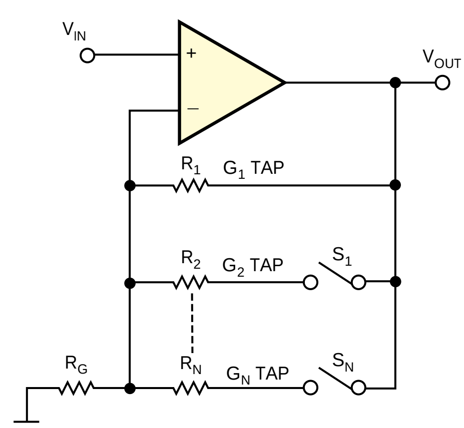

Figure 2 In a parallel-resistor-ladder network, connecting one resistor at a time in parallel with R_1 determines the circuit's gain.

Next, normalize R_1 to 1Ω and solve the equations for R_1:

$$1=(GAIN[1]-1)\times(R_2+R_3+...+R_{N+1}), \quad (7)$$

$$1=-R_2+(GAIN[2]-1)\times(R_3+...+R_{N+1}), \quad (8)$$

and

$$1=-R_2-R_3-...-R_N+(GAIN[N]-1)\times(...+R_{N+1}). \quad (9)$$

$$\begin{bmatrix} GAIN[1]-1 & GAIN[1]-1 & GAIN[1]-1 & GAIN[1]-1 \\ -1 & GAIN[2]-1 & GAIN[2]-1 & GAIN[2]-1 \\ ... & ... & ... & ... \\ -1 & -1 & -1 & GAIN[N]-1 \end{bmatrix} \times \begin{bmatrix} R_2 \\ R_3 \\ ... \\ R_{N+1} \end{bmatrix} = 1. \quad (10)$$

A network that synthesizes N gain values results in an N×N matrix whose upper echelon equals the desired gains minus one, in ascending order, and its lower echelon equals negative one. To produce the resistor values for the desired gains, invert the matrix and calculate its dot product with a unity matrix. For example, a circuit requiring four gain values of three, five, 24, and 50 also requires five resistors. Stuffing and solving the matrix yields:

$$\begin{bmatrix} 2 & 2 & 2 & 2 \\ -1 & 4 & 4 & 4 \\ -1 & -1 & 23 & 23 \\ -1 & -1 & -1 & 49 \end{bmatrix} \times \begin{bmatrix} R_2 \\ R_3 \\ R_4 \\ R_5 \end{bmatrix} = 1. \quad (11)$$

$$\begin{bmatrix} R_2 \\ R_3 \\ R_4 \\ R_5 \end{bmatrix} = \begin{bmatrix} 0.2000 \\ 0.2375 \\ 0.0325 \\ 0.0300 \end{bmatrix}. \quad (12)$$

Scale the resistors' values to 1 kΩ and select the closest available standard resistor values to produce gains of:

$$\begin{bmatrix} R_2 \\ R_3 \\ R_4 \\ R_5 \end{bmatrix} = \begin{bmatrix} 200 \\ 237 \\ 32.4 \\ 30.1 \end{bmatrix}. \quad R_1=1\,k\Omega. \quad GAINS=\begin{bmatrix} 3.002 \\ 5.007 \\ 23.99 \\ 49.82 \end{bmatrix}. \quad (13)$$

Figure 2 shows a parallel-resistor-ladder network. To select a gain value, connect an additional resistor in parallel with the other resistors. A circuit with N discrete gains requires N resistors in the ladder; an additional gain resistor, R_G; and N−1 switches. **Equation 14** describes the circuit's gain in the general case:

$$GAIN[n]=\frac{R_1\|R_2\|...\|R_N}{R_G}+1, \quad (14)$$

and **Equation 15** describes the parallel-resistor combination for each gain:

$$R_P[n]=(GAIN[n]-1)\times R_G. \quad (15)$$

The nth value of R_P equals the nth−1 value of R_P in parallel with the ladder's nth resistor. Solve the following equations for the nth resistor value:

$$R_P[n]=R_P[n-1]\,\|\,R_n, \quad (16)$$

$$R_1=(GAIN[1]-1)\times R_G, \quad (17)$$

and

$$R_n=\frac{R_P[n]\times R_P[n-1]}{R_P[n-1]-R_P[n]}. \quad (18)$$

To find the desired network's resistors, select the desired gain values and R_G and then use **Equation 14** to calculate the parallel values. Use the resulting values to solve **Equation 15** and find the required resistor values. As in the previous example, a circuit must produce gain values of three, five, 24, and 50. Four gain values require four resistors. Let R_G=1Ω. Solving **Equation 14** for the parallel-values matrix yields:

$$\begin{bmatrix} R_P[1] \\ R_P[2] \\ R_P[3] \\ R_P[4] \end{bmatrix} = \begin{bmatrix} 49 \\ 23 \\ 4 \\ 2 \end{bmatrix}. \quad (19)$$

Substituting these values into **Equation 15** yields the resistors' values:

$$R_1=49\times1=49\Omega, \quad (20)$$

$$R_2=\frac{23\times49}{49-23}=43.35\Omega, \quad (21)$$

$$R_3=\frac{4\times23}{23-4}=4.842\Omega, \quad (22)$$

and

$$R_4=\frac{2\times4}{4-2}=4\Omega. \quad (23)$$

Scaling to 1 kΩ and selecting the closest available standard-value resistors yields gains of:

$$\begin{bmatrix} R_1 \\ R_2 \\ R_3 \\ R_4 \end{bmatrix} = \begin{bmatrix} 48,700 \\ 43,200 \\ 4870 \\ 4002 \end{bmatrix}. \quad R_G=1\,k\Omega. \quad GAINS=\begin{bmatrix} 49.7 \\ 23.9 \\ 5.02 \\ 3 \end{bmatrix}. \quad (24)$$

Reference 1 provides a review of the matrix math. EDN

REFERENCE

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