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WITH NEW DFM-TOOL COMPANIES POPPING UP EVERY MONTH, IT CAN BE HARD TO SELECT WHICH YOU NEED FOR 65-NM PROCESSES. BUT THE TOP THREE FOUNDRIES AT THAT NODE HAVE MADE SOME OF THE CHOICES FOR YOU.

# SIFTING THE DFM PLAYERS

**D**oes DFM stand for “design for manufacturing” or “design for marketing”? That’s a question many observers of the EDA industry have been asking ever since someone uttered the term a few years ago. At the 130-nm node, lithography equipment could no longer clearly print certain semiconductor features, and OPC (optical-proximity-correction) tools from EDA vendors such as Numerical Technologies and OPC Technologies came to the rescue. As design processes have continued to shrink to 90 and 65 nm, lithography, mask-making, and fabs have become even more reliant on EDA-vendor inventions and fixes in design tools to ensure the accurate manufacture of chips. Fabs are turning to EDA tools even to help improve yield, which was once the sole responsibility—and a big selling point—of the fabs.



## AT A GLANCE

▣ Fabs now provide varying degrees of process and lithography data to DFM (design-for-manufacturing)-tool vendors.

▣ TSMC (Taiwan Semiconductor Manufacturing Co), UMC (United Microelectronics Corp), Chartered, IBM, and Samsung posted \$13.5 billion in fab revenue in 2005, according to Gartner.

▣ The entire fab segment posted revenue of \$18.4 billion, according to Gartner.

▣ If you buy the fab-recommended DFM tools, you will need at least \$1 million more than what you would pay for traditional tools.

▣ Rules-based lithography simulation and analysis are giving way to model-based approaches as designs move to the 65-nm node.

As such, the EDA industry, which has remained in a \$4 billion-in-revenue rut for the last four years, has identified DFM as a promising avenue of growth. That assertion recently received its strongest confirmation as the three biggest foundries employing 65-nm processes—TSMC (Taiwan Semiconductor Manufacturing Co), UMC (United Microelectronics Corp), and the CIS (Chartered/IBM/Samsung) Alliance—have all added a number of DFM technologies to their reference flows. In doing so, they are putting some of the burden to improve fabrication quality and yield on designers.

Luckily, plenty of EDA vendors are willing to provide you with DFM tools. Indeed, it seems that at least one new DFM start-up emerges every month, announcing itself to the world with claims of having essential technology. Meanwhile, some established companies have miraculously re-emerged as DFM vendors with few changes to legacy technologies but many changes to their marketing literature. And the big EDA vendors—Cadence, Synopsys, Mentor, and Magma—have aggressively added DFM

technologies and features to their established flows and have even reclassified as DFM some tools—mostly from the physical-design, physical-verification, design-for-test and TCAD (technology-computer-aided-design) lineups.

By June, research company Gartner Dataquest ([www.gartner.com](http://www.gartner.com)) had identified 16 DFM companies offering tools that layout engineers would use. Those companies are Anchor Semiconductor, Aprio Technologies, Blaze DFM, Brion Technologies, Cadence, ChipMD, Clear Shape Technologies, Ponte Solutions, Magma Design Automation, Mentor Graphics, Nanno Solutions, Nannor Technologies, Predictions Software, Sigma-C, Synopsys, and Xyalis. The list does not include vendors of statistical-timing tools, but it should (see **sidebar** “Statistical timing will become DFM”). The DFM segment of the EDA market has become so large that several subcategories of DFM now exist.

With all this in mind, you may be wondering what tools you will need to purchase to implement a design at 65 nm. If you want to do it right, the short answer is that you are going to need several tools. Oh, and bring your checkbook, too; it's going to be expensive.

Most of the dozens of IDMs (integrated-device manufacturers) don't publicly reveal what DFM companies they are working with or what technologies they have built on their own. But one way to separate the wheat from the chaff in DFM is to examine which tools the foundries

say you will need to get the best performance from 65-nm silicon. By press time, three of the top four foundries—first-ranked TSMC, second-ranked UMC, and fourth-ranked CIS Alliance—will have released their 65-nm reference flows. SMIC, the third-largest foundry, is now getting its 90-nm process up and running, but you can bet that it will soon be working on a 65-nm technology.

TSMC, UMC, Chartered, IBM, and Samsung posted a combined total of \$13.5 billion in fab revenue in 2005. The entire fab segment posted revenue of \$18.4 billion, according to Gartner. If that trend continues, the five fabs will likely manufacture the bulk of 65-nm ICs. None of the foundries says that it is necessary that you buy DFM tools to implement 65-nm silicon. You could use your 90-nm tool flow, they claim, but all strongly suggest that you buy “recommended” DFM tools if you want to quickly get the most out of their 65-nm processes.

## PROCESS DATA IS CRUCIAL

A couple of years ago, foundries were less than willing to share their sensitive defect density, yield data, and lithography models with EDA vendors, especially start-ups, fearing that the data would end up in competitors' hands. To their credit, TSMC, UMC, and the CIS Alliance foundries have been more than willing to give EDA vendors this data, with varying degrees of disclosure and protection.

According to Ed Wan, senior director of design-services marketing for TSMC,

## STATISTICAL TIMING WILL BECOME DFM

SSTA (statistical static-timing analysis) is promising technology, but its role and importance in the tool flow will likely evolve as the technology matures. It's likely that users will employ early SSTA tools to get a better idea of the true timing of circuits, rather than rely on worst-case timing models, which fabs provide in the form of wire-load models. The first evolution of SSTA will supplement static-timing tools and perhaps even replace them as sign-off tools.

SSTA-tool developers hope that the tools will one day enable engineers to make trade-offs among timing, power, and yield early in the design cycle. For example, squeezing high performance from a design may involve penalties to the design's power targets and reduce yield. But if they skimp on timing, they may see better yield and lower power consumption. Companies offering commercial SSTA include Altos Design Automation, Extreme DA, IBM, Magma, and Synopsys.

two years ago, TSMC recognized that sharing data with EDA vendors would be essential to the success of 65-nm silicon and EDA-DFM-tool development. TSMC this year unveiled its DDK (DFM Data Kit) and DUF (DFM Unified Format), which encapsulate data for LPC (lithography-process check), CMP (chemical-mechanical-polishing) analysis, and CAA (critical-area analysis). Devising this common format allows TSMC to work more closely with established EDA vendors but also provide up-and-coming tool vendors in the EDA market with solid data to try to make their tools comply with TSMC's 65-nm flow.

UMC has no common data format per se, but it does provide yield data to EDA vendors and selected customers. "We don't use absolute yield; we provide relative-yield information," says Patrick Lin, chief SOC (system-on-chip) architect for system and architecture support at UMC. "We don't provide direct data; rather, it's encrypted. Some tool companies don't require a lithography model, but, if they do, we encrypt it. We don't

## ALL THREE FOUNDRIES HAVE EVALUATED THE COMMERCIAL DFM OFFERINGS IN AN ATTEMPT TO SHAPE THEIR DFM FLOWS FOR CUSTOMERS.

think format is an important issue, as others do," he says. "Our goal is to just get a few tools ready for customers. To provide a solution to our customers is important; to provide a data format is not. If the whole industry is targeting a standard format, we're willing to participate."

The founders of the CIS Alliance formed the group to ensure that all three companies' 65-nm fabs were similar and thus worked from the same process rules and data format. The alliance has made available model kits that contain sensitive fab data in encrypted formats. Fab data in these model-based kits are for CAA, shape simulation, and CMP simulation.

### RECOMMENDED TOOLS

In creating their 65-nm flows, TSMC, UMC, and the CIS Alliance all have been working closely with the big four in EDA—Cadence, Synopsys, Mentor, and Magma—to ensure not just that the four have the DFM-point tools, but also that their flows synchronize with the new processes. The three foundries, however, differ in which point-tool companies they work with. In general, UMC works with any point-tool vendor that its customers want. TSMC, as in years past, has developed a reference flow for 65 nm outlining how Cadence's, Synopsys', or Magma's flows work with TSMC. The TSMC reference flows also include tools from smaller companies in case those three EDA vendors' flows don't provide the functions that TSMC recommends. This year, TSMC also created a DFM-compliance program in which it provides its DDK files to start-ups so that they can develop future DFM technologies. Somewhat as a result of its common-foundry

format, the CIS Alliance has extensively evaluated available commercial-EDA tools and strongly recommends that its customers use its suggested list of vendors. With 16 independent EDA vendors to choose from, all three foundries have evaluated the commercial DFM offerings in an attempt to shape their DFM flows for customers.

### TSMC REFERENCE FLOW

Every year, TSMC issues a new reference flow, which helps users get a better idea of design challenges and which tools they need to design for a given node. At last month's Design Automation Conference in San Francisco, TSMC unveiled reference flow 7.0, enabling customers to use flows from Cadence, Synopsys, and, new this year, Magma to design 65-nm ICs targeting TSMC's foundry (Figure 1). As in years past, the reference flow includes DFM and low-power tools. This year, however, TSMC also recommends that users buy SSTA (statistical-static-timing-analysis) tools, arguably a subcategory of DFM.

For years, TSMC has been driving the big vendors to ensure that their tools support its 65-nm process, according to Wan. Cadence, Synopsys, and Magma now all have complete DFM flows, so, if users want to go with single-vendor, all-in-one flows, TSMC verifies that their flows comply with TSMC's 65-nm process, he says. Synopsys and Magma already comply with TSMC's stipulation for SSTA. Cadence, on the other hand, is not yet fielding an SSTA technology. Cadence also until recently lacked a CMP-simulation technology but recently acquired CMP-simulation tool Praesagus to tie up that loose end.

In addition to its reference flow, TSMC has also announced a DFM-qualification program to ensure that third-party-DFM vendors also offer compliant tools. For lithography-process characterization and simulation, TSMC has thus far qualified Anchor Semiconductor's NanoScope DFP, Cadence's Virtuoso RV, Clear Shape's InShape, Magma's Blast Yield TX, Mentor Graphics' Calibre LFD (lithography-friendly design), and Synopsys' DFM LCC (lithography-compliance checking). For CMP simulation, TSMC has qualified Cadence/Praesagus Solutions'

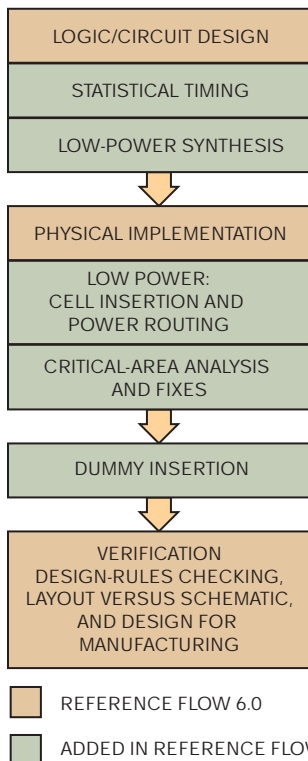


Figure 1 TSMC's 7.0 reference flow adds SSTA, DFM, and power management.

DVIP, Magma's Blast Yield TX, and Synopsys' DFM-CMP. For CAA, TSMC has qualified Cadence's Encounter-CAA, Magma's Blast Yield TX, Mentor's Calibre YieldAnalyzer, Ponte's Yield Analyzer, Predictions Software's Eyes, and Synopsys' IC Compiler. TSMC will add other companies over the coming months.

Wan says that TSMC is well-aware that many users want to use a mixed-tool flow or may be developing their own. For this group, TSMC provides a reference kit that combines scripts, application notes, and test cases. Meanwhile, TSMC recommends Blaze DFM for simultaneous power and yield enhancement.

### UMC's FLOW IS FLEXIBLE

UMC says that some DFM-tool functions are necessary for its 65-nm flow, especially those technologies adding functions to placement and routing, but other DFM tools are not yet necessary for sign-off. "Within DFM, there are a lot of different levels, and the needs of customers vary," says Lin. "Some require DFM tools, but they are not using them for sign-off but as learning tools for future processes. Customers can take advantage of some tools to improve their 65-nm designs." UMC will work with any EDA vendor customers ask for, but the company does have a reference flow (Figure 2). "In our reference

**"ANYTHING TO DO WITH ROUTING IS ESSENTIAL, AND, ONCE YOU ARE TALKING ABOUT ROUTING, THEY NEED TO KNOW LITHOGRAPHY, CAA, AND NORMAL DFM RULES."**

flow, we recommend the functions they should look at, but, as far as EDA vendors go, it's the customer's choice," says Lin. "Some of these tools need to tie closely to foundries. The tools must be accurate, and we've worked closely with some vendors to achieve that goal."

DFM functions for routers, such as metal fill, double-via insertion, and wire spreading, are essential, says Lin. In this area, the company has been working closely with Cadence, Synopsys, and Magma. "Anything to do with routing is essential, and, once you are talking about routing, they need to know lithography, CAA, and normal DFM rules," says Lin. CAA is also growing in importance, he says. "It is an area in which the fab needs

to provide relative-yield data," he says. "These tools allow customers to make a trade-off from a cost point of view. Customers often pressure us to provide some data." Two types of DFM technologies to help enhance lithography are also growing in importance, he notes. The first includes tools that can identify potential lithography hot spots in the physical-design steps. The second includes tools that identify lithography's impact on shape. "We need these tools so that we can calculate what impact a given shape change will have on electrical properties," says Lin. "That will take some time. Designers would love to have those tools, but a unified system doesn't yet exist." He says that UMC is working on that problem with Mentor Graphics, Clear Shape, and Anchor Semiconductor.

CMP simulation is also gaining importance. "CMP is a tricky area," says Lin. "For large designs, we will see some flatness issues, and that's where CMP simulation is necessary. In the early stage of the process, the flatness won't be good, but, as the process matures, it will be." He notes that it is helpful to have a CMP model for extraction tools so that they safely reflect the interlayer capacitance and series resistance of the interconnect. The company has been working most closely in this area with Cadence's recent acquisition, Praesagus, but Synopsys and Magma claim to also offer this technology.

SSTA is another promising area, says Lin. "I don't believe people will use it to sign off the design as yet," he says. "They will use the SSTA to tighten the on-chip-variation global margin. That's a first step. Maybe in the future nodes, they will make it a standard sign-off tool." The company has been working closely with SSTA start-up Extreme DA. The company is also working with Apache Design on thermal analysis, which can impact power and yield. Lin also notes that IP (intellectual property) and IP tools must also become more lithography-friendly and more adaptable to manufacturing.

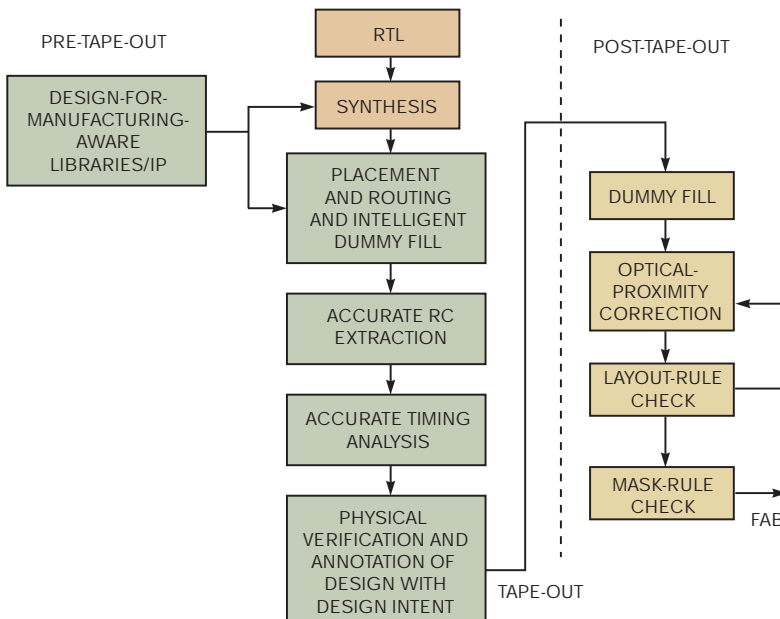


Figure 2 UMC's DFM flow stresses DFM-aware IP in addition to new tools.

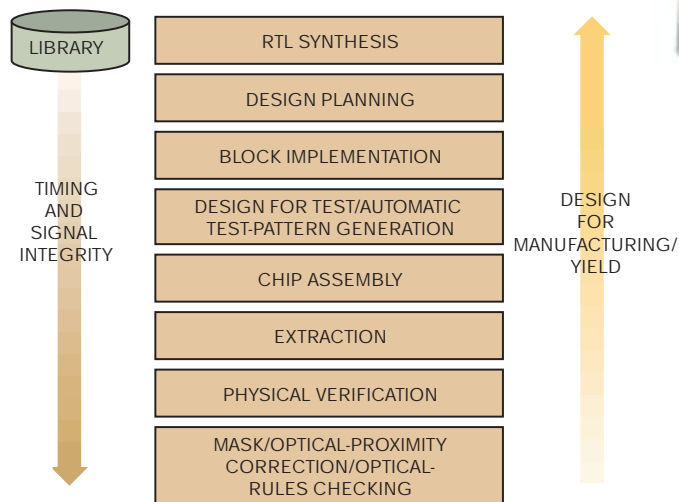


Figure 3 The CIS Alliance selected a DFM flow.

saves customers time in evaluating tools, but it also ensures that customers can ship their designs to Chartered, IBM, or Samsung fabs—likely with necessary adjustments to GDSII (Graphic Design System II) files and masks. Walter Ng, senior director for platform alliances at Chartered Semiconductor Manufacturing, says that when the CIS Alliance emerged last year, the three companies created eight subcommittees focusing on DFM-design guidelines: CAA, reference flows, lithography-based simulation, shape-based simulation, variation-aware timing, DFM services, CMP simulation, and DFM checking. Each subcommittee evaluated third-party tools and ran through evaluations to come up with a flow (Figure 3). “We selected the best technologies out there at least at the time the evaluations were done,” says Ng.

In the DFM-checking area, Chartered selected Mentor Graphics in the back-end for OPC, RET (resolution-enhancement technology), and lithography. “Even though it is a rule-checking tool, we still see it as a critical piece,” says Ng. “We don’t believe we can move completely from rules to model-based approaches.” The company selected Mentor Graphics Calibre DFM, which is now the Yield-Analyzer tool. “We’ve weighted the recommended rules, so folks can run their layouts through the checking deck,” says Ng. “It allows them to bin the highest priority rules and then focus on where they are going to fix the layout for those highest return-on-investment areas and then rerun it and see that the relative scoring

has improved for that cell or block.”

For CAA, Chartered selected Ponte Solutions’ model-based approach that accounts for defect densities on a per-layer basis. “The Ponte tool was at the time the most accurate in CAA and identifying hot spots,” says Ng. In the reference-flow area, the company is working with Cadence, Synopsys, and Magma. “They are all looking at ways to make their routers more intelligent and do a correct-by-construction approach,” says Ng. CMP simulation and fill capability offer accurate parasitic extraction, providing feedback to timing analysis and signal integrity to ensure that fill is uniform. The alliance picked Cadence’s Praesagus tool for this purpose.

The CIS Alliance uses Mentor Graphics’ LFD for shape and lithography simulation. The collaborative project helps designers locate potential trade-offs and effects on manufacturability, Ng notes. “We have been working with them to make sure that a product does what we expect from it,” says Ng. “The product is highly accurate because the input to it is the actual OPC deck.” The CIS Alliance is also working with Clear Shape in shape and lithography simulation. Because it works with an abstracted model, Clear Shape has greater capacity and performance than Calibre LFD, but the alliance deems the Mentor tool to be more accurate, says Ng. “Calibre LFD can be accurate, and Mentor is always enhancing its capabilities in accuracy, performance, and capacity,” he says.

No tools exist for DFM-layout guide-



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lines, but the CIS Alliance believes it has an advantage over competitors in this area by virtue of its common platform. "We have dedicated chapters to layout recommendations for manufacturability," says Ng, who points out that the alliance augments these recommendations as more designs, targeting different applications, go through fabs. "Between Chartered, IBM, and Samsung, we get to see a range of designs at various complexities," says Ng. "We've collaborated to bring together a DFM-layout-guideline document for our clients, and we update that a couple of times a quarter to make sure that the document encapsulates the latest observations and learning."

The CIS Alliance has also been working closely since last year's DAC with Blaze DFM for leakage reduction and yield optimization. "We have been working with some of our major customers with Blaze to demonstrate proof and value, and we've gone through some silicon, and that is promising technology," says Ng.

The CIS Alliance does not name the company it is working with for SSTA. However, it will likely get this technology from IBM, which has for years performed acclaimed research in SSTA. IBM's SSTA-tool-development group won the 2005 EDN Innovator of the Year award, and the group last year introduced an SSTA tool, but the technology has yet to appear in commercial flows outside IBM. "We are doing some work in that area, and we didn't announce a technology because we haven't yet produced a deliverable for the common process yet," says Ng. Although some of the technologies may become mandatory, right

now it's a trade-off. "The designers know better what they are willing to trade off against what," says Ng. "In this case, yield is one of the trade-off vectors at stake. Customers say, 'All I expect you guys to do is see what those trade-offs are, and I'll make those trade-offs and enable the data to make these tools work.' At some point, these tools may become critical. I can, for example, see that some of these technologies may end up augmenting DRC (design-rule checking). It is becoming more difficult, and the design rules for 45 nm are restrictive." He says that encapsulating the rules files requires large DRC decks.

### NOW, THE BAD NEWS: COST

If you add up the reported minimum cost of these tool flows, you come up with a sum of \$1 million to \$3 million for just one license of each point tool. For example, Blaze DFM's tool costs \$2 million for a one-year site license. Prices for the other DFM tools range from \$100,000 to \$250,000 for a single annual license. However, at every node, overblown hype regarding the cost of tools emerges, according to the foundries. Ng points out, for example, that hype sur-

### FOR MORE INFORMATION

Altos Design Automation <a href="http://www.altos-da.com">www.altos-da.com</a>	Magma Design Automation <a href="http://www.magma-da.com">www.magma-da.com</a>
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Chartered Semiconductor <a href="http://www.charteredsemi.com">www.charteredsemi.com</a>	Predictions Software <a href="http://www.icyield.com">www.icyield.com</a>
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Clear Shape Technologies <a href="http://www.clearshape.com">www.clearshape.com</a>	Sigma-C <a href="http://www.sigma-c.com">www.sigma-c.com</a>
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	Xyalis



rounded the emergence of signal integrity and the resultant retooling it required but that vendors eventually integrated the technology into the larger EDA-tool sets. "Some of these capabilities will go the same way, and vendors will build them into existing tools," says Ng. "There is certainly more consolidation to happen. Some of these DFM companies may find it hard to hang around as independent companies without being tightly coupled to these larger integrated solutions."

UMC's Lin points out that some of these functions are becoming more important and, in some cases, require users to purchase them in addition to the traditional 90-nm flow. He notes, however, that existing tools will absorb some of these features and that the company will solve some of these problems in the fab. "We didn't push that much of the burden to designers," he says. "But there is some benefit to push some of it to designers. We're trying to work from the fab side to

reduce problems and pass information to them, so that they can better use the flow. They don't have to be scared. I want to stress that it's the traditional flow; it's an add-on. There isn't much more the designer needs to do." With CMP, for example, designers need only a technology file from the fab to run SSTA.

Now that DFM has established itself, as with other EDA technologies, such as power and timing, EDA vendors will come up with technologies to allow designers to address manufacturing earlier in the flow—at floorplanning, for example, or even in the RTL (register-transfer level). Driving the correct-by-construction approach and making sure IP cores and foundation elements are DFM-ready will become necessary.

DFM is addressing problems and, therefore, at least for the 65- and 45-nm nodes, is becoming an avenue of growth for the EDA industry. Most vendors agree that nice-to-have features today in DFM

for the 65-nm node will likely become must-have features as the industry moves into the 45-nm node and below. It will be interesting to see whether standard tool flows absorb most of the DFM EDA technologies and whether the EDA vendors can successfully ensure that their tools account for most of the nasty DFM issues. It will also be interesting to see whether foundries can get the upper hand on many of these manufacturing issues, so that when you refer to DFM, you see it as a way to home in on performance, power, and yield targets rather than as an extra task you need to perform to make up for the shortcomings of the foundries. EDN



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