"Brick-wall" lowpass audio filter needs no tuning

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When a system's specifications call for a lowpass filter with a steep frequency-cutoff characteristic, an engineer can opt for a "brick-wall"-filter design that features a sharp transition band. For example, in an FM stereophonic-broadcast system, the lowpass filter in the baseband audio's left and right channels should have a −3-dB cutoff frequency of at least 15 kHz, a passband ripple of less than 0.3 dB, a stopband start frequency of at least 19 kHz, a stopband attenuation greater than 50 dB, and identical phase response for both channels.

The filter should provide adjustable gain to maximize SNR at the audio processor's first stage. The filter's frequency response should also include a notch at 19 kHz to achieve maximum attenuation at the FM-subcarrier pilot-tone frequency and thus minimize phasing problems. To reduce manufacturing costs, the filter should require no in-process adjustments. Conventional analog active-filter designs cannot meet these goals at reasonable cost and complexity without time-consuming adjustments. This Design Idea outlines an active-filter-synthesis approach that reduces a filter's sensitivity to passive-component tolerances and enables construction of inexpensive, high-order and highly selective filters.

The design process begins with selection of an appropriate passive-filter topology—in this example, a seventh-order elliptic filter with 50Ω input and output impedances (**Figure 1**). Setting the beginning of the stopband frequency span at 18.72 kHz produces a notch at the 19-kHz stereo-pilot frequency. Using the following **equation** to transform each component's impedance leaves the filter's amplitude-versus-frequency response characteristics unaltered.

$$Z'(s)=\frac{k}{s}\times Z(s).$$

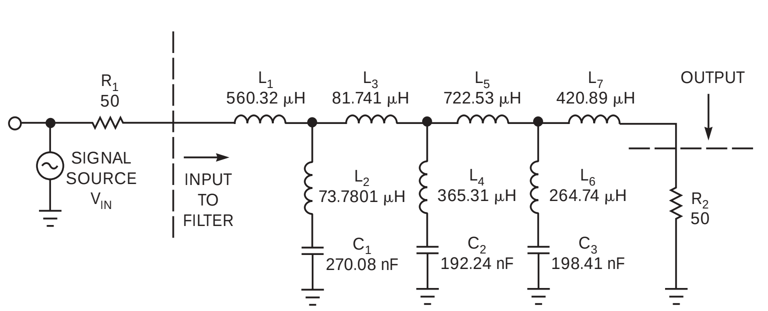

Figure 1 This seventh-order, elliptic, lowpass, passive-filter prototype features a 15-kHz cutoff frequency and stopband rejection exceeding 50 dB.

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As a result of the transformation, all resistors undergo transformation into capacitors, and adjusting the value of parameter k yields reasonable capacitance values for using 10%-tolerance parts. In this instance, select a value of 2.2 nF for C_1':

$$k=\frac{1}{R_1\times C_1'}.$$

Inductors transform into resistors, and using 2%-tolerance or better components meets the circuit's requirements. Capacitors transform into "supercapacitors" whose impedance exhibits a $1/s^2$ dependence:

$$Z'(s)=\frac{k}{s}\times\frac{1}{C_i s}=D_i'\times\frac{1}{s^2}.$$

Selecting a topology for a passive filter that contains the maximum number of inductors and references all capacitors to ground yields a transformed filter that consists of many resistors, several supercapacitors, and only two capacitors. You cannot obtain a supercapacitor as an off-the-shelf component, but its electrical analog comprises a few operational amplifiers and resistors (**Figure 2**). The following **equation** defines the gyrator's input impedance, Z_{IN}, with respect to ground:

$$Z_{IN}=\frac{Z_1\times Z_3\times Z_5}{Z_2\times Z_4}.$$

Selecting $Z_1=Z_3=1/Cs$ in the equation, setting capacitor value C at 2.2 nF, replacing impedances Z_2 and Z_5 with $R=11\ k\Omega$, and setting $Z_4=R_4$ yield a solution for D_i':

$$D_i' = \frac{C^2}{R_4}.$$

Figure 2 shows the filter's final schematic. Potentiometer R_1 adjusts the overall gain, and connecting resistors R_2 and R_{26} in parallel with capacitors C_1 and C_8 prevents dc blocking. The finished filter design uses medium-tolerance resistors, only eight capacitors, and two LF347 quad operational amplifiers—few amplifiers for a seventh-order active filter that requires no component adjustments to meet its specifications. Thanks to the design's precise implementation of the pilot-tone-rejection notch, the filter's measured attenuation at 19 kHz exceeds 60 dB. EDN

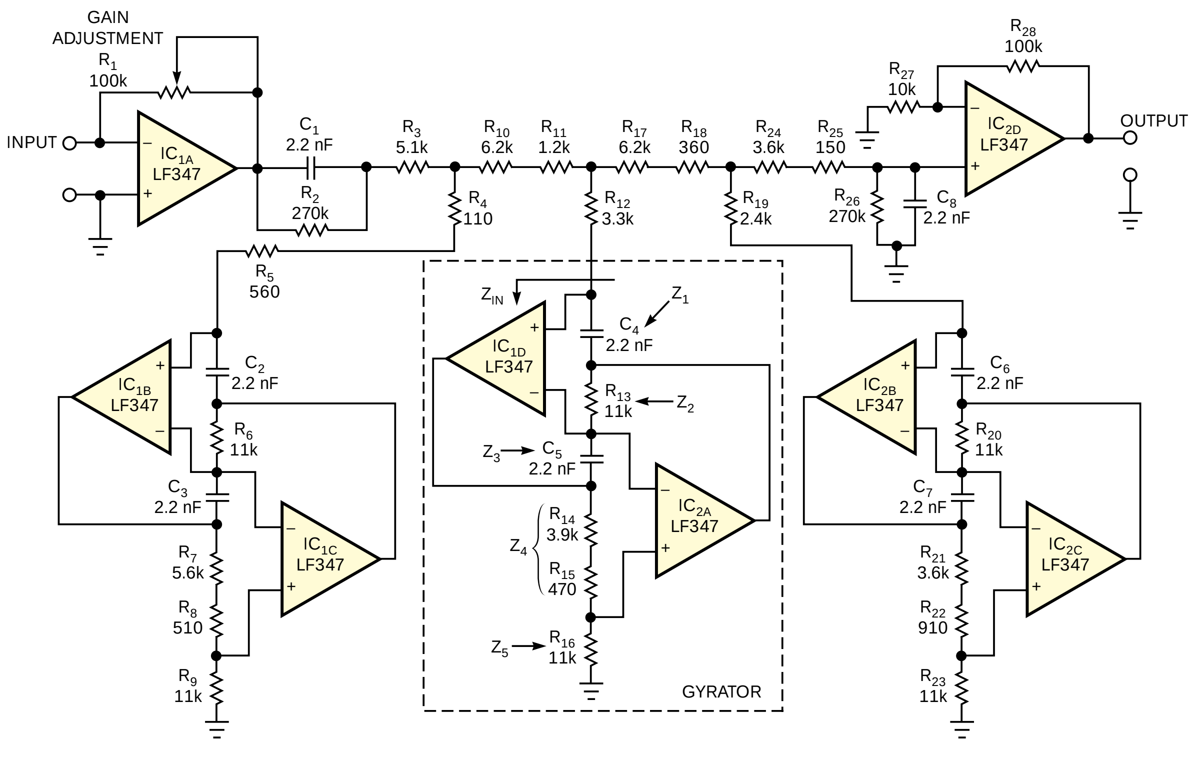
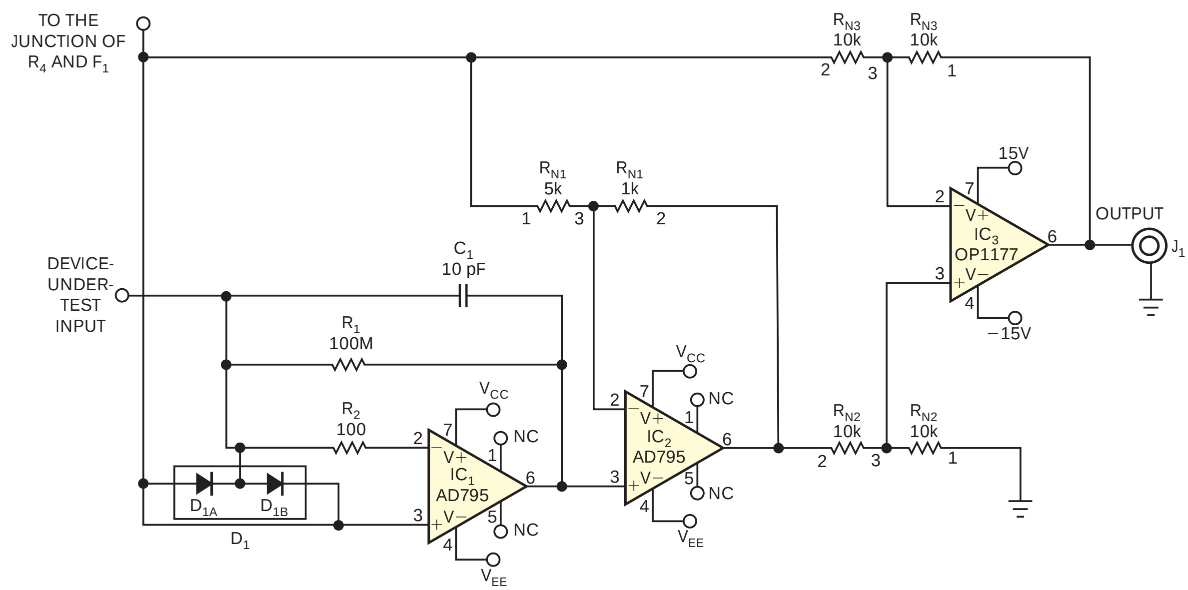


Figure 2 The finished circuit design eliminates inductors and substitutes gyrators as "supercapacitors." Using medium-tolerance components and quad op amps to reduce component count minimizes circuit cost.

Fast-settling picoammeter circuit handles wide voltage range

Rob Whitehouse, Analog Devices, Wilmington, MA

Evaluating analog switches, multiplexers, operational amplifiers, and other ICs poses challenges to IC-test engineers. A typical test scenario requires application of a test or forcing voltage to a device's input and measurement of any resultant leakage and offset currents, often at levels of 1 pA or less. In contrast to slow and expensive commercially available automated testers, the low-power measurement circuit in figures 1 through 3 can force a wide range of test voltages and offer fast settling to maximize device-test throughput. Extensive use of surface-mounted components minimizes



NOTE: R_{N1}, R_{N2}, AND R_{N3} ARE VISHAY MPM-SERIES RESISTOR NETWORKS.

Figure 1 This IVC uses a feedback-ammeter topology, which subtracts an unknown current from a feedback current and delivers an output voltage proportional to the unknown current.

its pc-board-space requirements and allows packaging of multiple measurement circuits close to the test fixture.

The circuit comprises a forcing-voltage buffer/amplifier, a floating-rail power supply, and an IVC (current-to-voltage converter). Applying a forcing voltage to a device under test induces leakage current, which the circuit converts to an output voltage proportional to the leakage current. In a conventional IVC, the current to be measured develops a voltage across a shunt resistor. The IVC uses a feedback-ammeter topology in which operational amplifier IC_1, an Analog Devices AD795, subtracts an unknown current from a feedback current and delivers an output voltage proportional to the unknown current (Figure 1).

In this design, the input's dc resistance consists mostly of R_2 and IC_1's effective input resistance, or slightly more than 100Ω at dc. At frequencies in the power-line range of 50 to 300 Hz, the circuit's ac impedance averages approximately 10 kΩ, or 1000 times less than a typical shunt-resistance IVC's input resistance of approximately 10 MΩ. The circuit's 100-MΩ feedback resistor, R_1, provides a current-to-voltage-conversion ratio that exceeds the shunt-conversion ratio by a factor of 10. This design settles much faster and provides better interference rejection at power-line frequencies than shunt converters. It also reduces unwanted voltage-divider effects when testing operational amplifiers' input currents.

R_1 produces a current-to-voltage-conversion ratio of 100 μV/pA. Amplifier IC_2, an AD795, provides an additional voltage gain of 10, boosting the ratio to 1 mV/pA and reducing the effect of errors that differential ampli-

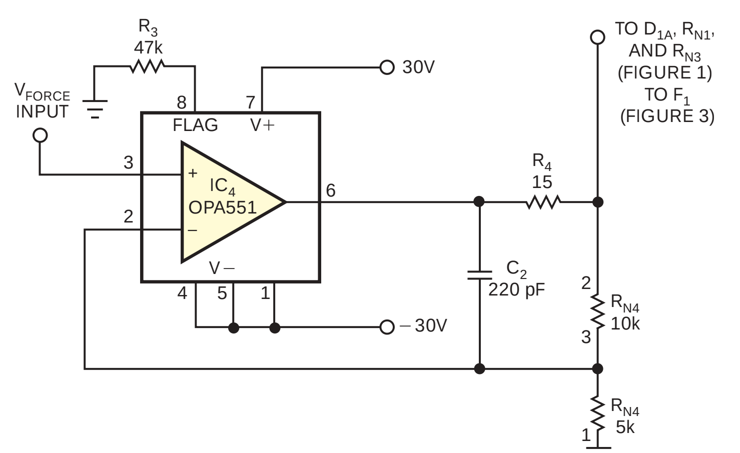


Figure 2 A gain-of-three high-voltage amplifier derives forcing voltages as high as ±22V from voltages of ±7V from test equipment.

fier IC_3's CMRR (common-mode-rejection ratio) introduces. Differential amplifier IC_3, an OP1177, subtracts the forcing voltage from the IVC's output and provides a ground-referenced output signal.

A back-to-back pair of BAV199 diodes, D_{1A} and D_{1B}, protects IC_1 from voltage overloads by shunting high currents to the forcing-voltage amplifier, IC_4, and its protective fuse, F_1. When the forcing voltage rapidly slews from one value to another, the diodes greatly improve the IVC's settling time by providing high-drive currents during high-slew-rate intervals.

Operating from ±30V supply rails, a lightly compensated, gain-of-three, high-voltage OPA551 amplifier, IC_4, derives forcing voltages as high as ±22V from ordinary ATE (automatic-test-equipment) voltages of ±7V (Figure 2). In case of a catastrophically shorted device under test, fuse F_1 prevents further damage by limiting fault current from IC_4, which can deliver as much as 380 mA of short-circuit current.

The output of IC_4 also drives a regulator circuit that produces ±5V floating-power-supply voltages referenced to the test-input forcing voltage (Figure 3). This part of the circuit dissipates less than 100 mW of power with ±30V supplies. Vishay/Siliconix (www.vishay.com) SST505 JFET constant-current regulator "diodes" Q_1 and Q_4 provide 1-mA constant-current sources, which transistors Q_2 and Q_3 buffer. Each current-regulator diode carries a 45V maximum rating, and the buffers provide overvoltage protection by limiting the voltages applied across the diodes to approximately 3V.

Applying 1 mA to resistors R_5 and R_6 develops the ±5V rail voltages. Diodes D_2 and D_3 compensate for the base-emitter-voltage drops across emitter followers Q_{6B} and Q_{7B}. Transistors Q_{6A} and Q_{7A} provide overvoltage protection when a defective device under test short-circuits its power supply to the IVC's input node. Transistors Q_5 and

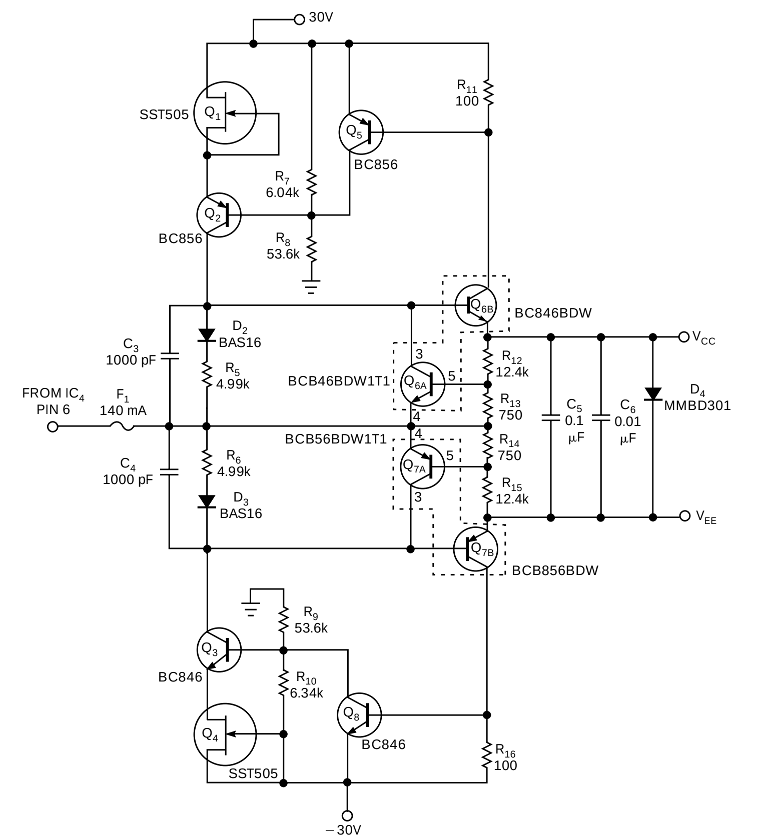


Figure 3 This floating-regulator circuit produces ±5V floating-power-supply voltages V_{CC} and V_{EE} referenced to the test input's forcing voltage.

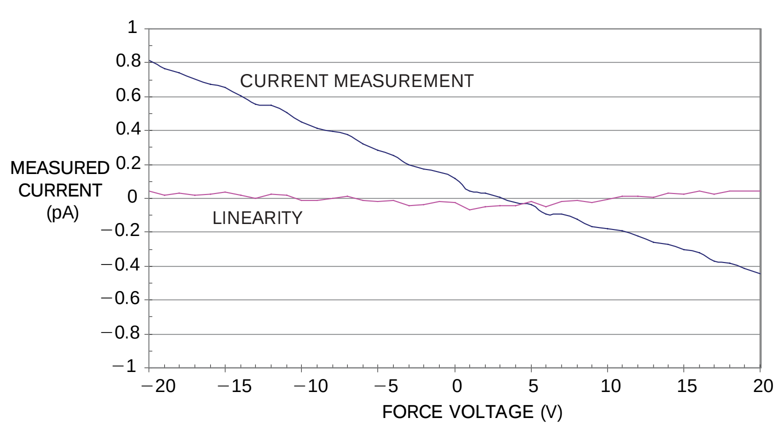


Figure 4 Over a ±20V forcing-voltage span, the circuit produces an unloaded-output current-measurement error of −31 fA/V.

Q_8 limit the floating supplies' output currents by shunting the current diodes. Diode D_4 protects against polarity inversion of the floating-supply rails during unusual start-up conditions.

In operation, the circuit delivers an output of 0.999V/nA over a ±4-nA full-scale input range at an effective transresistance of 1 GΩ. The circuit's output offset corresponds to approximately 143 fA. Beyond the forced-voltage span of ±22V, the floating-supply-rail voltages begin to saturate, the input-CMRR limitations of IC_3 become evident, and the IVC's output voltage becomes nonlinear. **Figure 4** shows the circuit's current-measurement error of −31 fA/V from the circuit's unloaded output over a ±20V forcing-voltage span. The differential amplifier comprising IC_3, R_{N2}, and R_{N3} contributes most of the circuit's gain, and IC_1's low input-bias current contributes to the low offset error. Output linearity over the ±20V forcing-voltage range averages 111 fA p-p.

THE CIRCUIT'S SLEW-RATE CAPABILITY VARIES CONSIDERABLY, BUT IN GENERAL THE OUTPUT FAITHFULLY SLEWS THE ENTIRE 40V FORCING-VOLTAGE SPAN IN 100 μSEC OR LESS.

The circuit's slew-rate capability varies considerably, but in general the output faithfully slews the entire 40V forcing-voltage span in 100 μsec or less as D_1 drives the device under test. Once the high-slew period completes, the IVC comes out of saturation, and its output becomes an exponential voltage with a time constant of 1 msec. The output settles to 100 fA in approximately 10.6 msec. Under no-load conditions, the circuit consumes approximately 10.2 mA from the ±30V supplies and 400 μA from the ±15V supplies. The prototype circuit's layout occupies approximately 1.5 in.^{2} on a single-sided pc board, and placing components on both sides of a double-sided board would reduce the area to 1 in.^{2} For best performance, the layout must include guard rings around the input terminal and all traces attached to Pin 2 of IC_1. The circuit's size allows its placement on a device-under-test fixture to minimize lead lengths and power-line-induced electromagnetic interference. Although able to measure currents as small as 1 pA, the circuit can accommodate larger currents by reducing the value of R_1. EDN