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Stacking up

Advances in IC packaging and back-end manufacturing processes that take advantage of 3-D structures are beginning to blur the line between fabrication and packaging technologies. That the result could substantially increase the IC's I/O density is an understatement: IBM reports results that suggest that an exponential improvement in I/O density is possible with 3-D-IC integration (**Reference 1**).

With the widespread adoption of surface-mount-assembly methods in the 1980s, package-to-board interconnect density took the important step from through-hole technology's traditional 100-mil lead pitch to a 50-mil pitch. Though perhaps a quaint perspective now, this move at the time seemed like a bold one because the surface-mount components did not mechanically interlock with the board to ensure their alignment. As assembly equipment, alignment methods, and surface-mount-soldering technologies continued to improve, so did package I/O density, leading to the use of the now-ubiquitous BGA (ball-grid array). (Students of packaging history will note that IBM developed an early form of BGA in the

1960s for mounting transistors in the System 360. Such mounting methods, however, did not enjoy widespread use for three more decades.)

During this same historic interval, the density at the die-to-package interface increased, as well, reflecting the growth in functional density that CMOS-fabrication-process scaling facilitated. One innovation, the MCM (multichip module), allowed manufacturers to combine chips in a single package—an economic construction reminiscent of comparatively expensive chip-and-wire hybrids. As with hybrids, MCM assembly mounts dice in a planar arrangement on a substrate. Unlike hybrids, MCMs generally use organic packaging and leave passives as external components. Traditional wire bonds can make the chip-to-package connections, or, in the case of high-I/O-count modules, those interconnects can take advantage of flip-chip technology, with I/O pitch in the 150- to 200-micron range. These modules reach interconnect densities on the order of 10^3 I/O per cm^2 (**Figure 1**).

So-called SIP (system-in-package) technologies replace the MCM's planar layout with die stacking. Die stacking provides a rare opportunity in assembly technologies to construct shield plates, which are useful for shielding sensitive nodes in high-gain analog-signal

chains from noisy digital sections in mixed-signal modules (**Reference 2**). The vertical structures also facilitate shorter interchip connections for better high-frequency performance than MCMs provide. Low-I/O-density functions can use bond wires for chip-to-chip and chip-to-package connections and still reduce the finished product's footprint to less than that of an equivalent MCM. In high-density modules, area-array interconnects feature I/O pitches of approximately 50 microns and connection densities greater than 10^4 I/O per cm^2 .

The IBM paper describes a stacked-die technology, 3-D-IC integration, that exploits silicon through-vias and attains a 6-micron pitch and 10^6 I/O per cm^2 . The silicon-on-silicon technology provides interconnection bandwidths as high as 6 GHz and avoids differential coefficients of thermal expansion of adjacent layers for mechanical robustness.

One challenge to high-speed, high-density modules is decoupling. The 3-D-IC integration provides for integrated bypass capacitors constructed on silicon-interposer layers on the chip side of the chip-to-board stray inductances.

Thermal plates on the top can conduct heat from the active devices to the package's lid. Such 3-D-cooling structures can further enhance the package's ability to support both speed and functional density.EDN

REFERENCES

- 1 Knickerbocker, John, et al, "3-D silicon integration and silicon packaging technology using silicon through-vias," *IEEE Journal of Solid-State Circuits*, August 2006, pg 1718.
- 2 Israelsohn, Joshua, "Newton's chips: low-g accelerometer ICs," *EDN*, Oct 28, 2004, pg 65, www.edn.com/article/CA472836.

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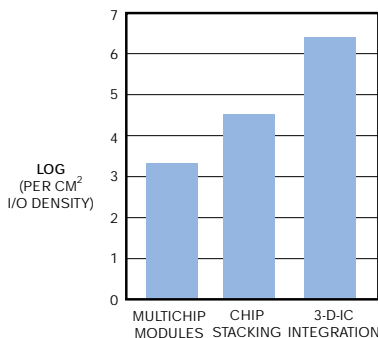


Figure 1 A stacked-die technology, 3-D-IC integration, increases density over multichip modules and chip stacking.