

Load-transient-response testing for voltage regulators

VARIATIONS OCCUR IN VOLTAGE REGULATORS' TRANSIENT LOADS; THUS, THE DEVICES REQUIRE CAREFUL EVALUATION AND TESTING.

Semiconductor memory, card readers, microprocessors, disk drives, piezoelectric devices, and digital systems create transient loads that voltage regulators must service. Ideally, regulator output would be invariant during a load transient. In practice, however, some variation occurs, and this variation becomes problematic if a system exceeds its allowable operating-voltage tolerances. This problem mandates testing the regulator and its associated support components to verify desired performance under transient-loading conditions. You can use various methods to generate transient loads and allow observation of regulator response.

Figure 1 shows a conceptual load-transient generator. The

regulator under test drives dc and switched resistive loads, which may be manually variable. The device monitors its switched current and output voltage, permitting comparison of the output voltage and the load current under static and dynamic conditions. The switched current is either on or off; there is no electronically controllable linear region.

Figure 2 shows a practical implementation of the load-transient generator. Capacitors augment the voltage regulator under test; these capacitors provide an energy reservoir, similar to a mechanical flywheel, to aid transient response. The size, dielectric, and location of these capacitors, particularly C_{OUT} , have a pronounced effect on transient response and overall regulator stability (references 1 and 2). The input pulse triggers the

LTC1693 FET driver to switch Q_1 , generating a transient-load current from the regulator. An oscilloscope monitors the instantaneous load voltage and, through a "clip-on" wideband-probe, current (see sidebar "Probing considerations for load-transient-response measurements"). Figure 3 provides an evaluation of the circuit's load-transient-generating capabilities by substituting a low-impedance power source for the regulator. The combination of a high-capacity power supply, low-impedance connections, and generous bypassing maintains low impedance across frequency. Figure 4 shows the circuit in Figure 3's response to the LTC1693-1 FET driver (Trace A) by cleanly switching 1A in 15 nsec (Trace B). Such speed is useful for simulating many loads but has restricted versatility. Although fast, the circuit cannot emulate loads between the minimum and the maximum currents.

CLOSED-LOOP TESTERS

Figure 5's conceptual closed-loop load-transient generator linearly controls Q_1 's gate voltage to set instantaneous transient current at any desired point, allowing simulation of nearly any load profile. Feedback from Q_1 's source to the A_1 control amplifier closes a loop around Q_1 , stabilizing its operating point. Q_1 's current assumes a value that depends on the control-input voltage and the current-sense resistor over a wide bandwidth. Once A_1 biases to Q_1 's

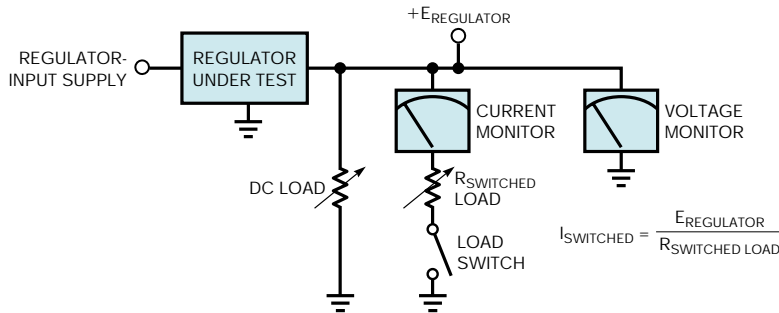


Figure 1 This conceptual regulator-load tester includes switched and dc loads and voltage and current monitors. The resistor values set dc and switched-load currents. The switched current is either on or off; there is no controllable linear region.

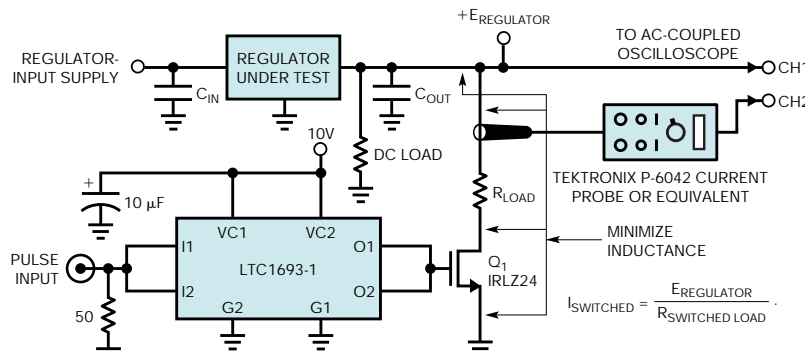


Figure 2 A practical regulator-load tester includes a FET driver and Q_1 switch. The oscilloscope monitors the current-probe output and regulator response.

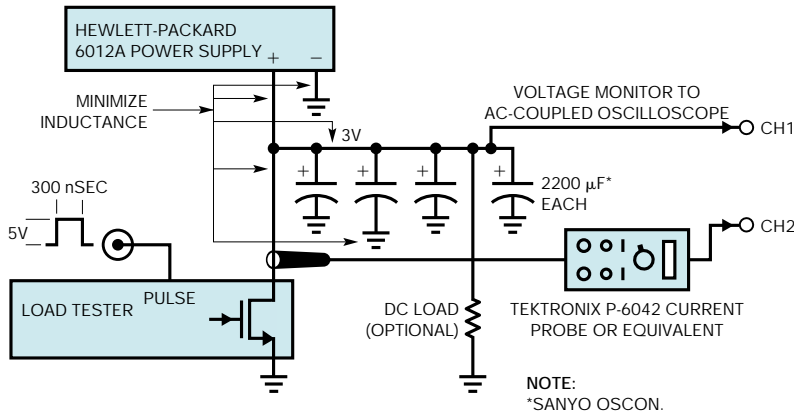


Figure 3 Substituting a well-bypassed, low-impedance power supply for the regulator lets you determine the load tester's response time.

conductance threshold, small variations in A_1 's output result in large current changes in Q_1 's channel. As such, A_1 need not output large excursions; its small signal bandwidth, rather than its slew rate, is the fundamental speed limitation. Within this restriction, Q_1 's current waveform is the same shape as A_1 's control-input voltage, allowing linear control of load current. This versatile capability permits a variety of simulated loads.

FET-BASED CIRCUIT

Figure 6 shows a practical incarnation of a FET-based closed-loop load-transient generator, including dc-bias and waveform inputs. A_1 must drive Q_1 's high-capacitance gate at high frequency, necessitating high peak A_1 output currents and attention to feedback-loop compensation. A_1 , a 60-MHz current-feedback amplifier, has an output-current capacity exceeding 1A. Maintaining stability and waveform fidelity at high frequency while driving Q_1 's gate capacitance necessitates settable gate-drive-peaking components, a damper network, feedback trimming, and loop-peaking adjustments. You make the required dc trim first. Without applying an input, trim the 1-mV adjust

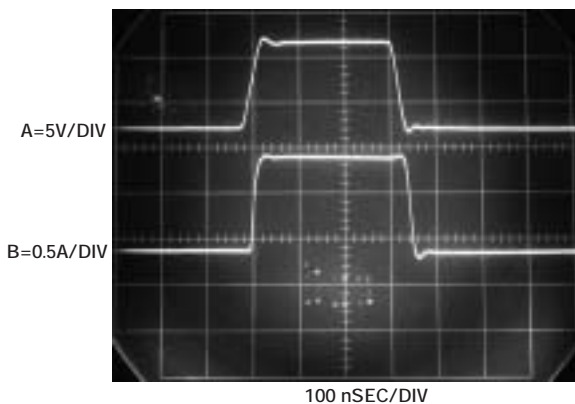


Figure 4 Figure 2's circuit responds to the FET driver's output (Trace A), switching a 1A load (Trace B) in 15 nsec.

for 1 mV dc at Q_1 's source. You make the ac trims using Figure 7's arrangement. Similar to the circuit in Figure 3, this "brick-wall"-regulated source provides minimal ripple and sag when the load-transient generator step-loads it. Apply the inputs as the figure shows and trim the gate drive, feedback, and loop-peaking adjustments for the cleanest square-cornered response on the oscilloscope's current-probe-equipped channel.

BIPOLAR TRANSISTORS

The circuit in Figure 8 considerably simplifies the previous circuit's loop dynamics and eliminates all ac trims. The major trade-off is a halving of speed. The circuit is similar to the one in Figure 6, except that Q_1 is a bipolar transistor. The bipolar's greatly reduced input capacitance allows A_1 to drive a more benign load. This approach permits you to use an amplifier with lower output current and eliminates the dynamic trims necessary to accommodate Figure 6's FET-gate capacitance. The sole trim is the 1-mV adjustment, which you accomplish as described. You can eliminate this trim at the cost of circuit complexity (see sidebar "A trimless, closed-loop-transient-load tester"). Aside from the twofold speed decrease, the bipolar transistor also introduces a 1% output-current error due to its base current. You add Q_2 to prevent excessive Q_1 base current when the regulator supply is absent. The diode prevents reverse-base bias under any circumstances.

CLOSED-LOOP-CIRCUIT PERFORMANCE

Figures 9 and 10 show the two wideband circuits' operation. The FET-based circuit (Figure 9) requires only a 50-mV A_1 swing (Trace A) to enforce Trace B's flat-topped current pulse with 50-nsec edges through Q_1 . Figure 10 details the bipolar-transistor-based circuit's performance. Trace A, taken at Q_1 's

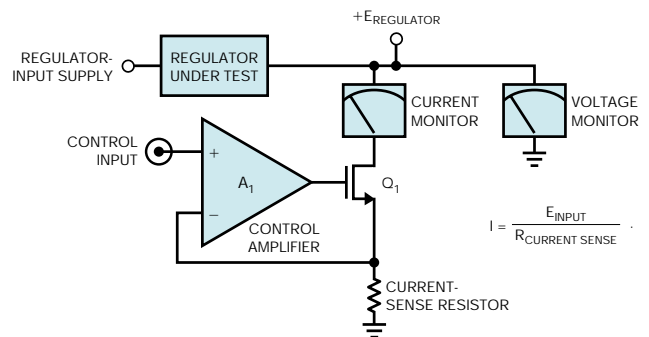


Figure 5 In this conceptual closed-loop-load tester, A_1 controls Q_1 's source voltage, setting the regulator's output current. Q_1 's drain-current waveshape is identical to A_1 's input, allowing linear control of the load current. The voltage and current monitors match those in Figure 1.

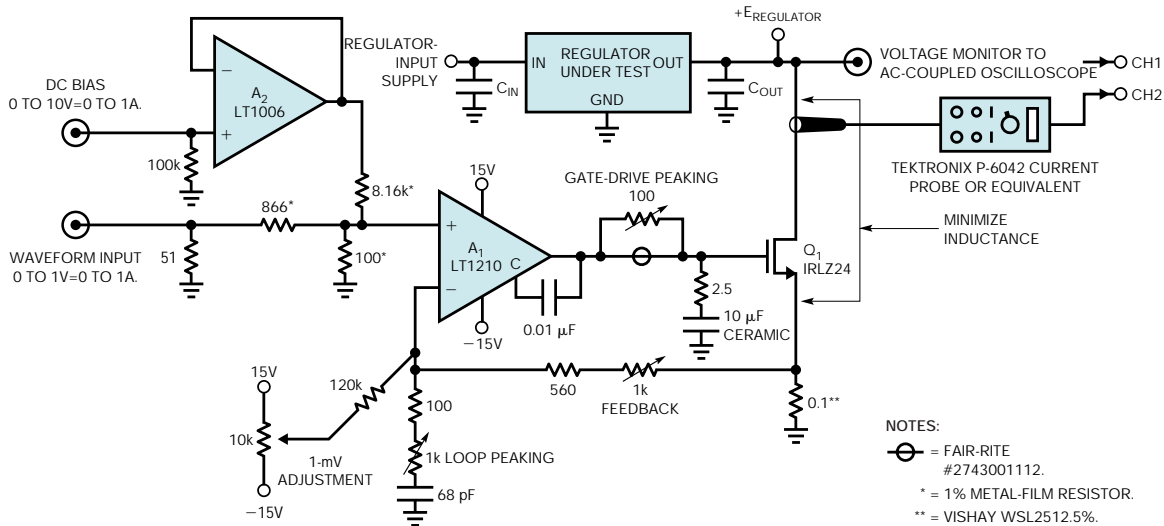


Figure 6 In a detailed closed-loop-load tester, the dc-level and pulse inputs feed A_1 to the Q_1 current-sinking-regulator load. Q_1 's gain allows a small A_1 output swing, permitting wide bandwidth. The damper network, feedback, and peaking trims optimize edge response.

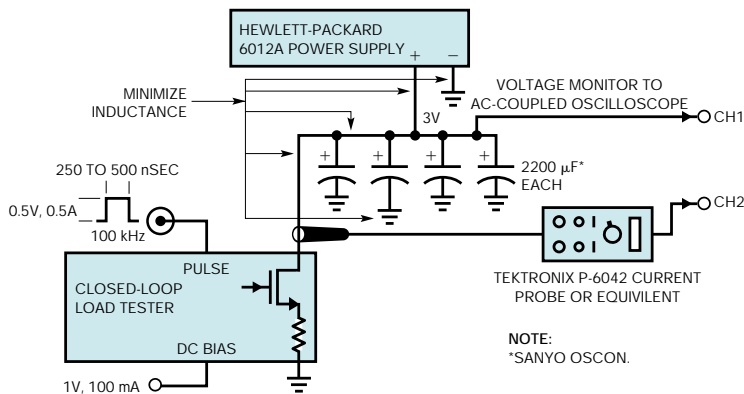


Figure 7 Determining the closed-loop-load-tester response time occurs as in Figure 3. A "brick-wall" input provides a low-impedance source.

base, rises less than 100 mV, causing Trace B's clean, 1A current conduction through Q_1 . This circuit's 100-nsec edges, about two times slower than the more complex FET-based version, are still fast enough for most practical transient-load testing.

LOAD-TRANSIENT TESTING

These circuits permit rapid and thorough voltage-regulator load-transient testing. **Figure 11** uses **Figure 6**'s circuit to evaluate an LT1963A linear regulator. **Figure 12** shows regulator response (Trace B) to Trace A's asymmetrically edged input pulse. The ramped leading edge, within the LT1963A's bandwidth, results in Trace B's smooth 10-mV p-p excursion. The fast trailing edge, well outside the LT1963A's passband,

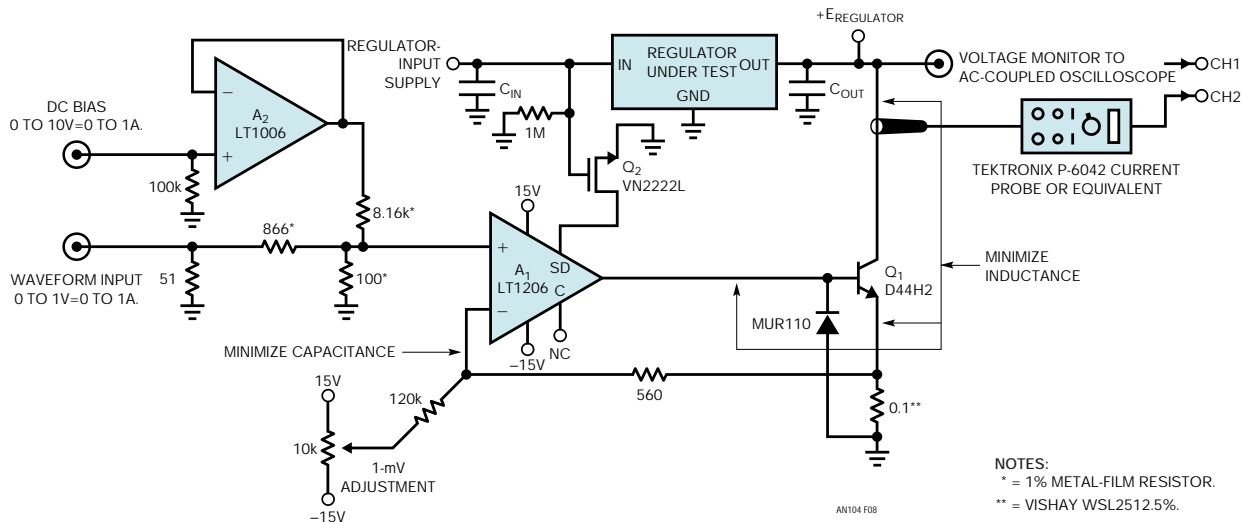


Figure 8 This circuit matches that of **Figure 6** but with a bipolar transistor. Q_1 's reduced input capacitance simplifies loop dynamics, eliminating compensation components and trims. The trade-off is a halving of speed and a base-current-induced 1% error.

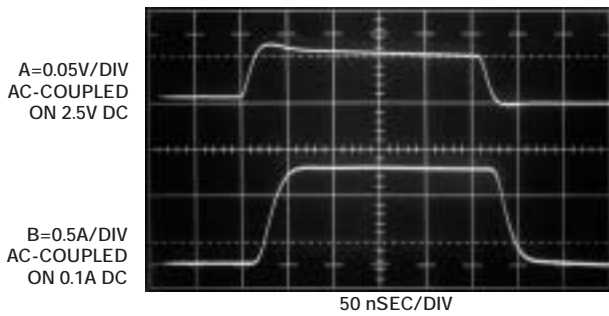


Figure 9 Figure 6's closed-loop-load-tester step response is quick and clean, showing 50-nsec edges and a flat top. (Q_1 's current is Trace B.) A_1 's output (Trace A) swings only 50 mV, allowing wideband operation. Trace B's presentation is slightly delayed due to voltage and current-probe time skew.

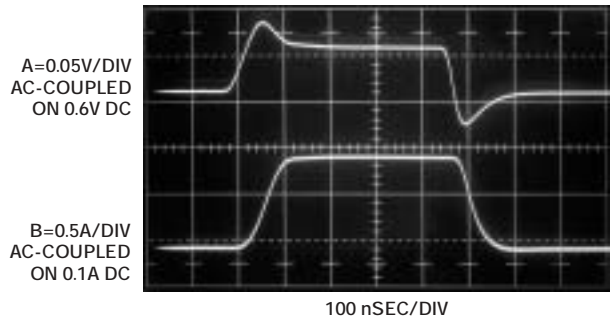


Figure 10 Figure 8's bipolar-output-load-tester response is two times slower than the FET version, but the circuit is simpler and eliminates compensation trims. Trace A is A_1 's output, and Trace B is Q_1 's collector current.

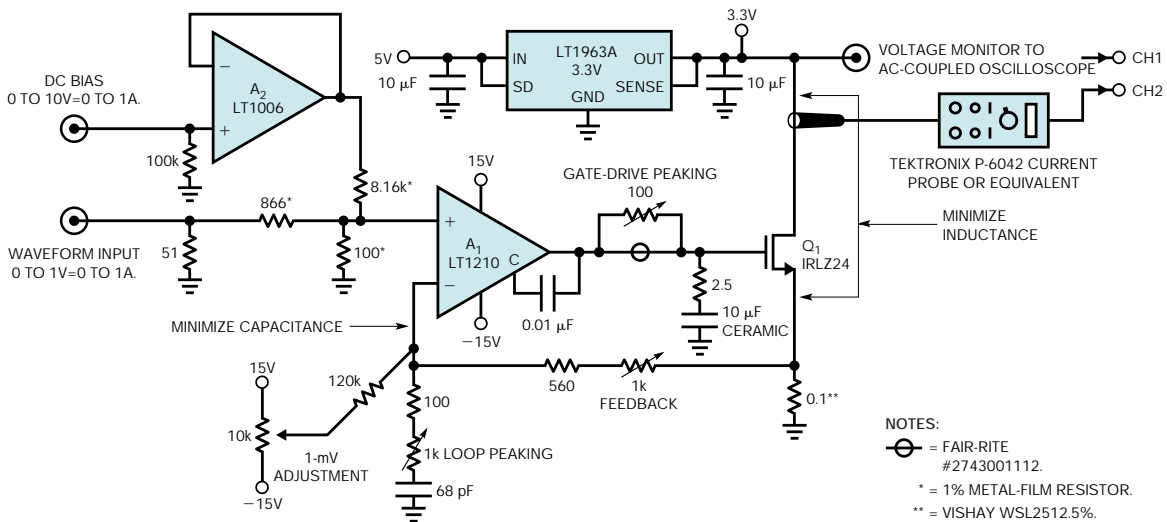


Figure 11 This closed-loop-load tester with an LT1963A regulator provides load testing for a variety of current and load waveshapes.

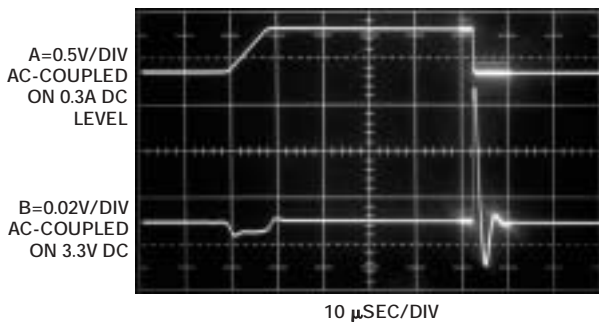


Figure 12 The circuit in Figure 11 responds (Trace B) to an asymmetrically edged pulse input (Trace A). A ramped leading edge within the LT1963A's bandwidth results in Trace B's smooth, 10-mV-p-p excursion. A fast trailing edge outside the LT1963A's bandwidth causes Trace B's abrupt 75-mV-p-p disruption. The photo intensifies the trace's latter portion for clarity.

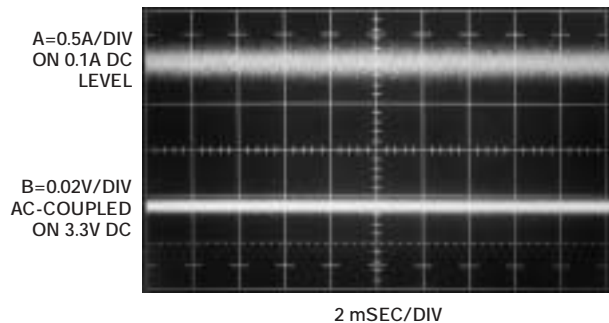


Figure 13 A 500-mA-p-p, 500-kHz noise load (Trace A) within the regulator's bandpass produces only 6-mV artifacts at Trace B's regulator output.

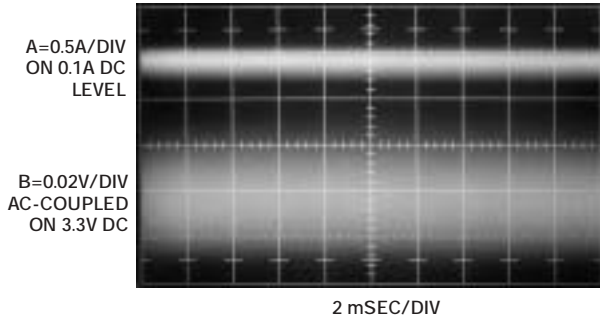


Figure 14 This waveform has the same conditions as Figure 13, except with increased noise bandwidth of 5 MHz, exceeding the regulator's bandwidth and resulting in 50-mV-p-p output error.

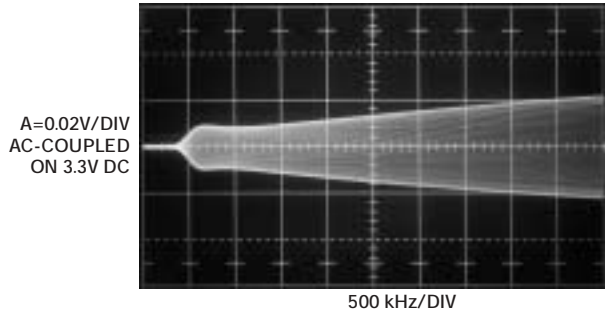


Figure 15 A swept, dc to 5-MHz, 0.35A load on 0.2A dc causes the regulator's output impedance to rise with frequency and correspondingly increases output error.

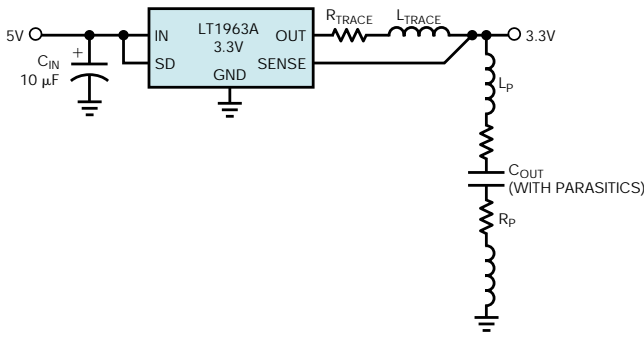


Figure 16 C_{OUT} dominates the regulator's dynamic response; C_{IN} is much less critical. Parasitic inductance and resistance limit the capacitor's effectiveness at frequency. The capacitor's value and dielectric significantly influence the load-step response. Excessive trace impedance is also a factor.

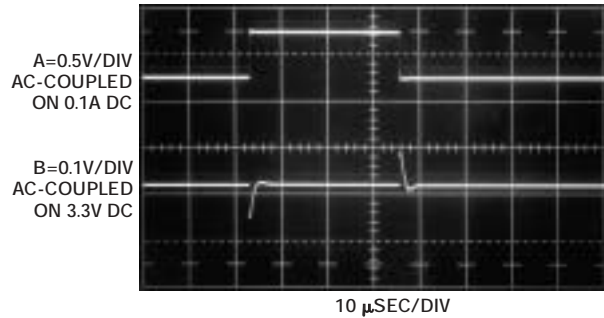


Figure 17 A stepped 0.5A load to Figure 16's circuit (Trace A) with $C_{IN}=C_{OUT}=10\ \mu\text{F}$ results in Trace B's regulator output. The use of low-loss capacitors promotes controlled output excursions.

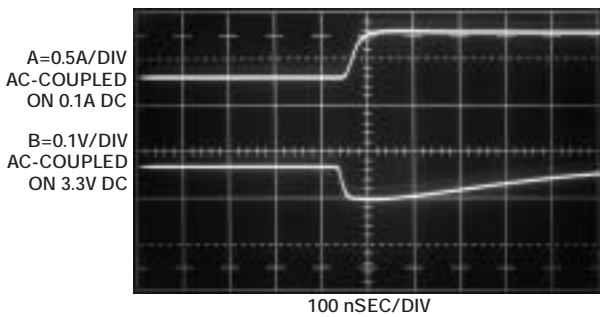


Figure 18 The expanding horizontal scale shows Trace B's smooth regulator-output response. Mismatched current- and voltage-probe delays account for slight time skewing.

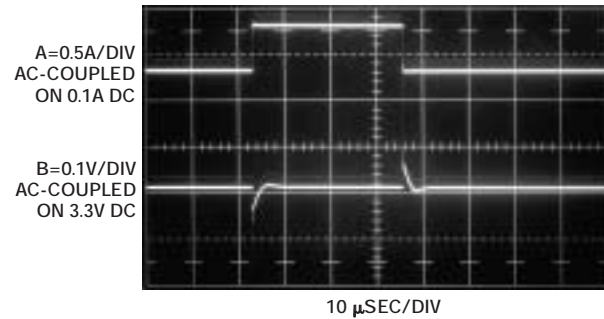


Figure 19 An "equivalent" 10- μF C_{OUT} capacitor to the one in Figure 17 shows performance that appears similar at 10 $\mu\text{sec/division}$.

causes Trace B's abrupt disruption. C_{OUT} supplies too little current to maintain output level, and a 75-mV-p-p spike results before the regulator resumes control. In **Figure 13**, a 500-mA p-p, 500-kHz noise load, emulating a multitude of incoherent loads, feeds the regulator in Trace A. This frequency is within

the regulator's bandwidth, and only 6 mV p-p of disturbance appears in Trace B, the regulator output. **Figure 14** maintains the same conditions, except that noise bandwidth increases to 5 MHz. This increase exceeds regulation bandwidth, resulting in more than 50-mV p-p error, an eightfold increase.

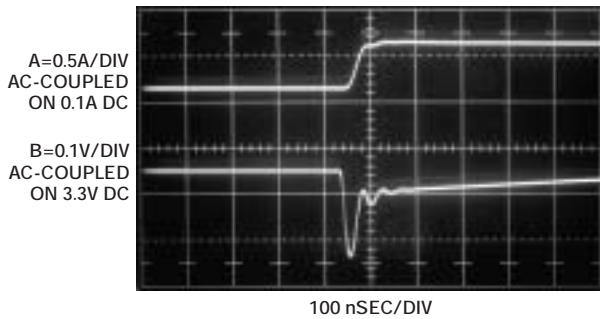


Figure 20 The horizontal-scale expansion reveals that the “equivalent” capacitor produces two times more amplitude error than the one in Figure 18. Mismatched probe delays cause time skewing between traces.

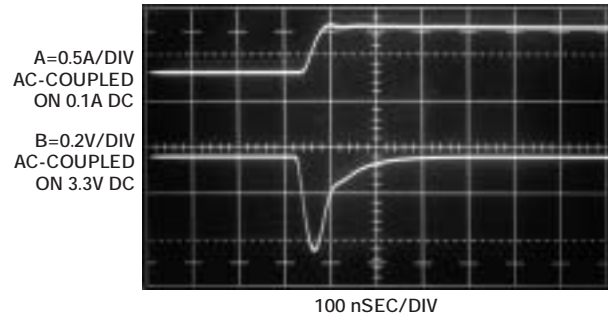


Figure 21 An excessively lossy 10- μF C_{OUT} allows a 400-mV excursion—four times Figure 18’s amount. The time skewing between the traces derives from probe mismatch.

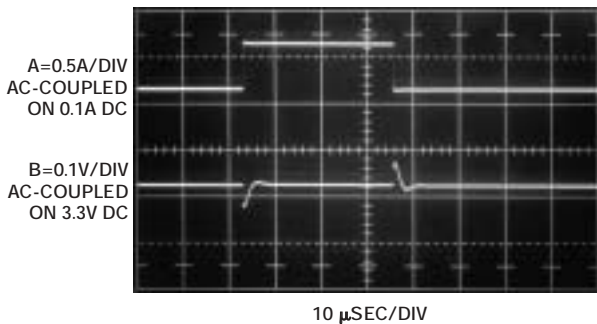


Figure 22 Replacing C_{OUT} with a low-loss, 33- μF unit yields a 40% smaller output-response transient than that of Figure 17.

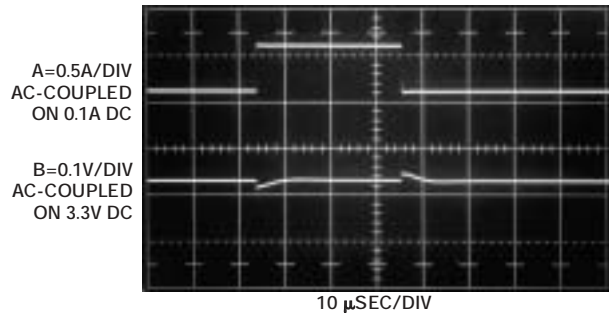


Figure 23 A low-loss, 330- μF capacitor keeps output-response transients to less than 20 mV—four times lower than Figure 17’s 10- μF capacitor.

Figure 15 shows what happens when you present a 0.2A, dc-biased, swept, dc to 5-MHz, 0.35A load to the regulator. The regulator’s rising output impedance versus frequency results in ascending error as frequency scales. This information allows determination of regulator output impedance versus frequency.

CAPACITOR’S ROLE IN REGULATOR RESPONSE

The regulator employs capacitors at its input (C_{IN}) and output (C_{OUT}) to augment its high-frequency response. You should carefully consider the capacitor’s dielectric, value, and location because they greatly influence regulator characteristics (references 1, 2, and 3). C_{OUT} dominates the regulator’s dynamic response; C_{IN} is much less critical, as long as it does not discharge below the regulator’s dropout point. **Figure 16** shows a typical regulator circuit and emphasizes C_{OUT} and its parasitics. Parasitic inductance and resistance limit capacitor effectiveness at frequency. The capacitor’s dielectric and value significantly influence load-step response. A “hidden” parasitic, impedance buildup in regulator-output-trace runs, also influences regulation characteristics, although you can minimize the parasitic effects by remote sensing and distributed capacitive bypassing.

Figure 17 shows **Figure 16**’s circuit responding (Trace B) to a 0.5A load step biased on 0.1A dc (Trace A) with $C_{\text{IN}}=C_{\text{OUT}}=10\ \mu\text{F}$. The circuit employs low-loss capacitors, resulting in Trace B’s well-controlled output. **Figure 18** greatly expands the horizontal time scale to investigate high-frequency behavior.

Regulator-output deviation (Trace B) is smooth with no abrupt discontinuities. **Figure 19** runs the same test as **Figure 17** using an output capacitor claimed as “equivalent” to the one that **Figure 17** employs. At 10 $\mu\text{sec/division}$, the scope photos seem similar, but **Figure 20** indicates problems. This photo, taken at the same higher sweep speed as the one in **Figure 18**, reveals the “equivalent” capacitor to have twice as much amplitude error, higher frequency content, and higher resonances than the one in **Figure 18**. (Always specify components according to observed performance, rather than salesmen’s claims.) **Figure 21** substitutes a lossy 10- μF unit for C_{OUT} . This capacitor allows a 400-mV excursion (note Trace B’s vertical-scale change), greater than four times **Figure 18**’s amount. Conversely, **Figure 22** increases C_{OUT} to a low-loss, 33- μF type, decreasing Trace B’s output-response transient by 40% versus **Figure 18**. **Figure 23**’s further increase, to a low-loss, 330- μF capacitor, keeps transients inside 20 mV: four times lower than **Figure 18**’s 10- μF value.

The lesson is clear: Capacitor value and dielectric quality have a pronounced effect on transient-load response. Try before specifying!

RISE TIME VERSUS REGULATOR RESPONSE

The closed-loop-load-transient generator also allows investigating load-transient rise time on regulation at high speed. **Figure 24** shows **Figure 16**’s circuit ($C_{\text{IN}}=C_{\text{OUT}}=10\ \mu\text{F}$), respond-

PROBING CONSIDERATIONS FOR LOAD-TRANSIENT-RESPONSE MEASUREMENTS

Signals of interest in load-transient-response studies occur within a bandwidth of approximately 25 MHz and a rise time of 14 nsec. This modest speed range eases probing techniques, but high-fidelity measurement requires some care. You measure load current with a dc-stabilized, Hall-effect, clip-on current probe such as the Tektronix (www.tektronix.com) P-6042 or A6302/AM503. The conductor loop in the probe jaws should encompass the smallest possible area to minimize introduced para-

sitic inductance, which can degrade measurement. At higher speeds, grounding the probe case may slightly decrease measurement aberrations, but this effect is usually small.

You perform voltage measurement, typically ac-coupled and ranging from 10 to 250 mV, using the arrangement in Figure A.

This arrangement feeds the measured voltage to a BNC 50 Ω , back-terminated cable, which drives the oscilloscope through a dc-blocking capacitor and a 50 Ω termination. The back termination is strict prac-

tice, enforcing a true 50 Ω signal path. You can eliminate the unit's 6-dB attenuation if it presents problems with only minor signal degradation in the 25-MHz measurement pass-band. The termination at the oscilloscope end is not negotiable. Figure B shows a typical observed load transient with no back termination but 50 Ω at the oscilloscope. The presentation is clean and well-defined. Figure C removes the cable's 50 Ω termination, causing a distorted leading edge, ill-defined peaking, and pro-

nounced postevent ringing. Even at relatively modest frequencies, the cable displays unterminated-transmission-line characteristics, resulting in signal distortion.

In theory, a 1 \times scope probe using a probe-tip coaxial connection could replace the described circuit, but such probes usually have bandwidth limitations of 10 to 20 MHz. Conversely, a 10 \times probe is wideband, but the oscilloscope's vertical sensitivity must accommodate the introduced attenuation.

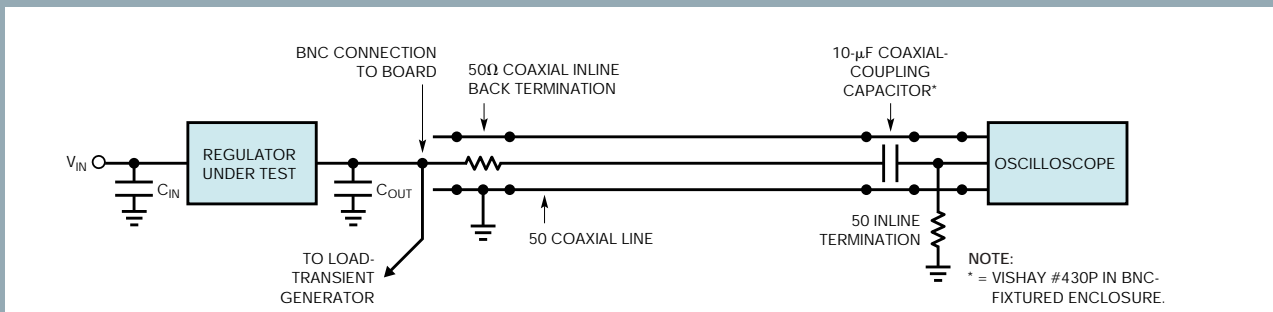


Figure A A coaxial-load-transient voltage-measurement path promotes observed signal fidelity. You can remove the 50 Ω back termination with minimal impact on the 25-MHz signal path's integrity.

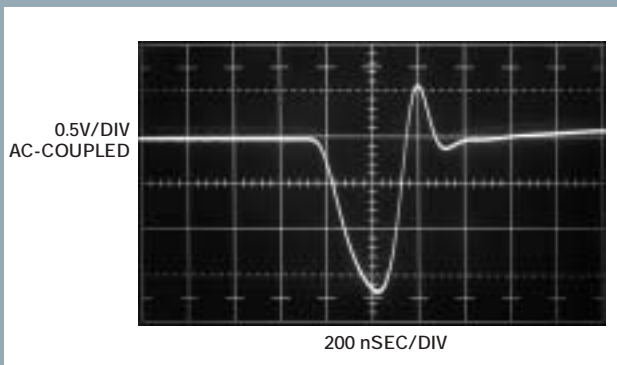


Figure B Observing a typical high-speed transient through Figure A's measurement path presents a clean and well-defined signal.

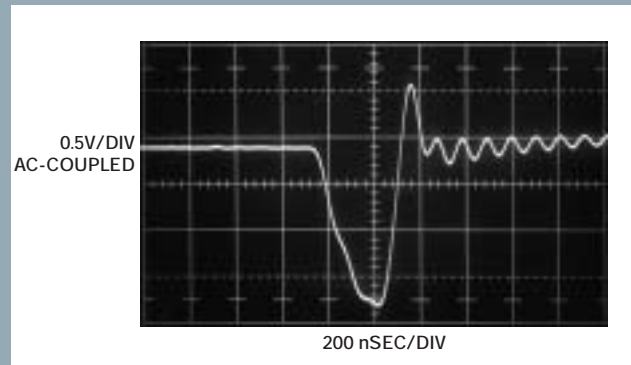


Figure C Measuring Figure B's transient without the 50 Ω oscilloscope's termination shows results in waveform distortion and postevent ringing.

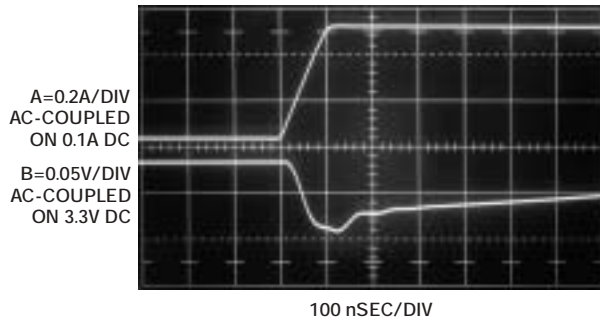


Figure 24 The regulator's output response (Trace B) to a 100-nsec rise-time current step (Trace A) for C_{OUT} is 10 μ F. The response decay peaks at 75 mV.

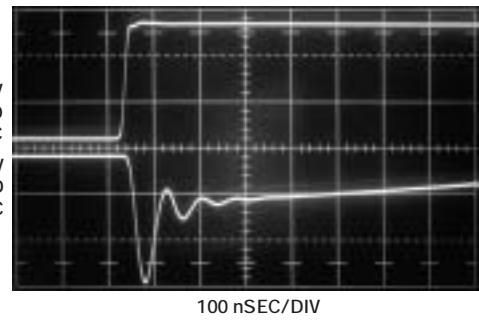


Figure 25 Faster rise-time current step (Trace A) increases response-decay peak (Trace B) to 140 mV, indicating increased regulation loss versus frequency.

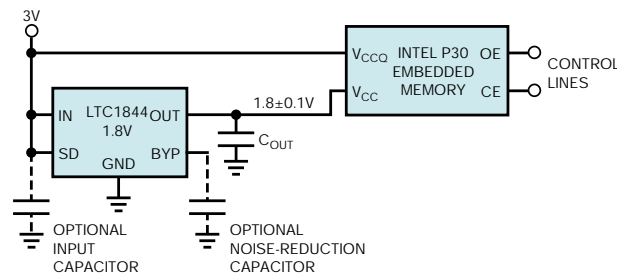


Figure 26 The P30 embedded-memory voltage regulator must maintain a ± 0.1 V error band. Control-line movement causes 50-mA load steps, necessitating attention to C_{OUT} selection.

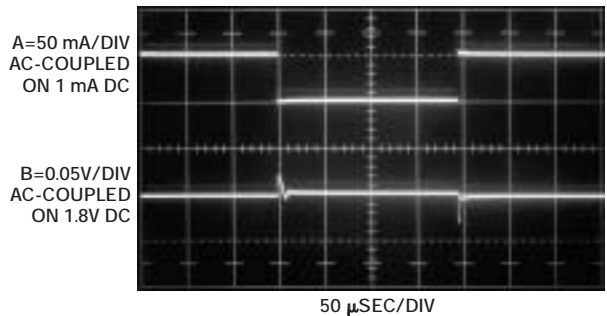


Figure 27 A 50-mA load step (Trace A) results in 30-mV regulator-response peaks, two times better than error-budget requirements. C_{OUT} is a low-loss, 1- μ F capacitor.

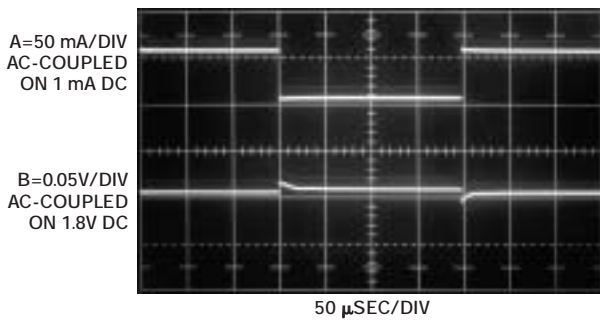


Figure 28 Increasing the value of C_{OUT} to 10 μ F decreases regulator-output peaks to 12 mV, almost six times better than required.

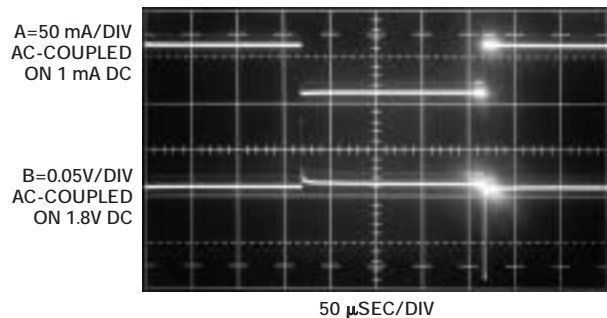


Figure 29 A low-grade, 10- μ F C_{OUT} causes 100-mV regulator-output peaks (Trace B), violating the P30 regulator's memory limits. The scope photo intensifies the trace's latter portion for clarity.

ing to a 0.5A, 100-nsec rise-time step on a 0.1A dc load (Trace A). Response decay (Trace B) peaks at 75 mV with some following aberrations. Decreasing Trace A's load-step rise time (**Figure 25**) almost doubles Trace B's response error, with attendant enlarged following aberrations. This scenario indicates increased regulator error at higher frequency.

All regulators present increasing error with frequency—some more than others. A slow load transient can unfairly make a poor

TABLE 1 INTEL P30 EMBEDDED-MEMORY VOLTAGE-REGULATOR ERROR BUDGET

Parameter	Limits
Intel-specified supply limits	1.8V \pm 0.1V
LTC1844-regulator initial accuracy	$\pm 1.75\%$ (± 31.5 mV)
Dynamic-error allowance	± 68.5 mV

