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PSoC microcontroller and LVDT measure position

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Connecting an LVDT (linear-variable-differential transformer) to a microcontroller can prove challenging because an LVDT requires ac-input excitation and measurement of ac outputs to determine its movable core's position (**Reference 1**). Most microcontrollers lack dedicated ac-signal-generation and -processing capabilities and thus require external circuitry to generate harmonic-free, amplitude- and frequency-stable sine-wave signals. Conversion of an LVDT's output signals' amplitude and phase into a form compatible with a microcontroller's internal ADC usually requires additional external circuitry.

In contrast with conventional microcontrollers, Cypress Semiconductor Corp's (www.cypress.com) PSoC microcontrollers include user-configurable logic and analog blocks that simplify generation and measurement of ac signals. PSoC devices have the unusual feature of being able to generate analog signals without demanding continuous CPU attention. The PSoC's flexible analog and digital blocks can drive an LVDT and measure its outputs without requiring any external circuitry. **Figure 1** shows the complete circuit of the LVDT interface, and **Figure 2** shows

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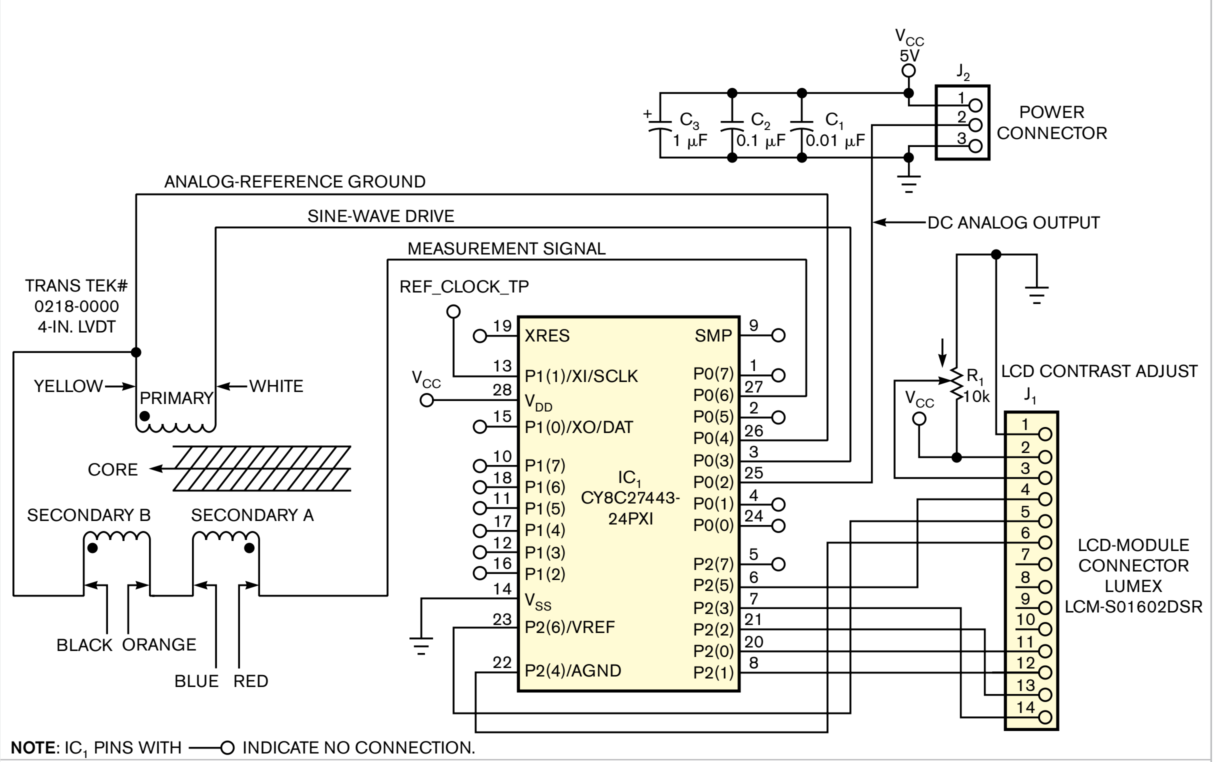


Figure 1 A single PSoC can excite an LVDT, digitize the position of its core, and present the data to an external LCD.

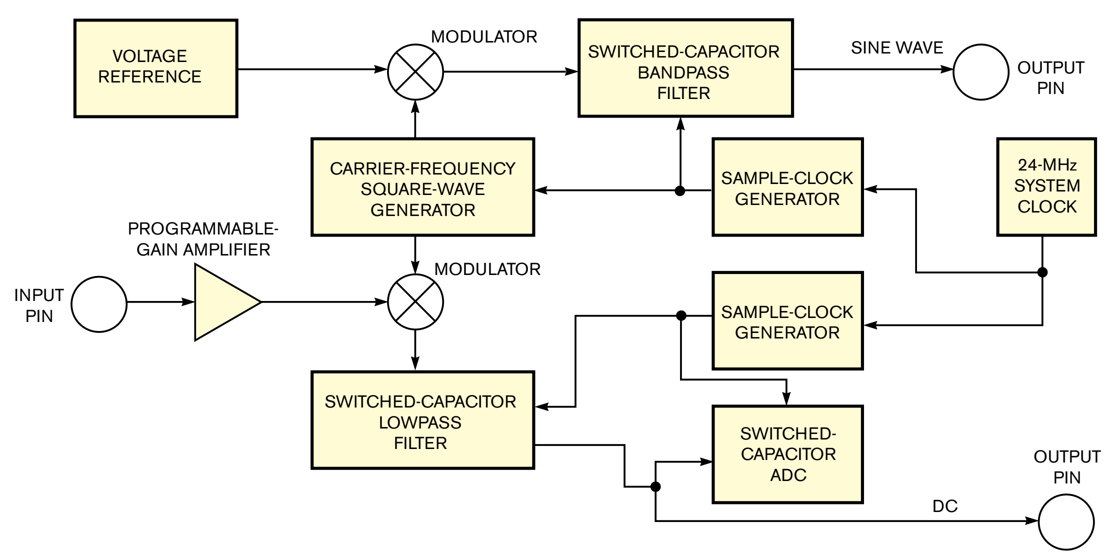


Figure 2 The LVDT-interface circuit requires many analog functions.

the PSoC microcontroller's internal circuit blocks.

The PSoC uses pairs of user-configurable switched-capacitor blocks to implement both bandpass and lowpass filters. You can create a high-quality sine wave by generating a square wave and applying it to a PSoC switched-capacitor filter through a modulator built into the first switched-capacitor block. Passing the square wave through a narrow bandpass filter centered on the square wave's fundamental frequency removes most of the harmonics.

To obtain the highest fidelity sine waveform from a PSoC switched-capacitor bandpass filter, use the highest possible oversampling rate—a factor of approximately 33—or 33 steps per sine-wave cycle. The resultant sine wave is smooth enough to drive an LVDT, which attenuates any residual higher order harmonics. Scaling the PSoC's internal voltage reference with a programmable-gain amplifier provides coarse control over the square wave's amplitude before it undergoes filtering. To compensate for the waveform's dc-offset voltage, an amplifier buffers the 2.6V internal analog-ground reference and drives an output pin that serves as the LVDT's analog-ground return.

The LVDT's output consists of a variable-amplitude sine-wave voltage whose phase angle with respect to the sine-wave excitation voltage undergoes a significant and variable shift that sometimes exceeds 180°. A signal from the LVDT drives one of the PSoC's programmable-gain amplifiers, whose output feeds a switched-capacitor lowpass filter followed by a modulator for synchronous rectification. The rectified signal drives an output pin and one of the PSoC's switched-capacitor ADCs.

Applying the LVDT's output to a synchronous rectifier followed by a lowpass filter produces a dc voltage that can feed an ADC or directly drive an analog feedback-control system. In a PSoC microcontroller, a lowpass switched-capacitor filter connected to an ADC requires that the same sample clock drive both circuits, resulting in a conversion rate for the PSoC's 11-bit delta-sigma ADC that's approximately one-half of the lowpass filter's corner frequency. Synchronous rectification produces a ripple frequency twice that of the excitation frequency and thus is easier to remove with a lowpass filter. Relocating the lowpass filter's corner frequency to one-third of the excitation frequency allows measurements of the LVDT's output to 11-bit resolution with a standard deviation of 1 LSB (least significant bit) or less.

Dividing the PSoC's 24-MHz internal system clock with logic blocks configured as counter chains generates all of the digital clock signals the switched-capacitor analog-circuit blocks require. After power application or a reset, the PSoC's CPU configures all the configured analog and digital blocks and starts their operation. From then on, the hardware excites the LVDT and measures its output at 500 samples/sec without further intervention by the CPU. With the PSoC's CPU running at 12 MHz, processing the ADC's housekeeping activities and interrupts consumes less than 3% of the CPU's resources.

Plenty of the PSoC's resources remain available for calculating the LVDT's position and for displaying the results in text format on an LCD module. Four analog blocks, five logic blocks, and many I/O pins remain available to support a more demanding application. **Figure 3** (next page) shows configurable blocks that are available for adding features.EDN

REFERENCE

1 "Linear variable differential transformer," *Wikipedia*, http://en.wikipedia.org/wiki/Lvdt.

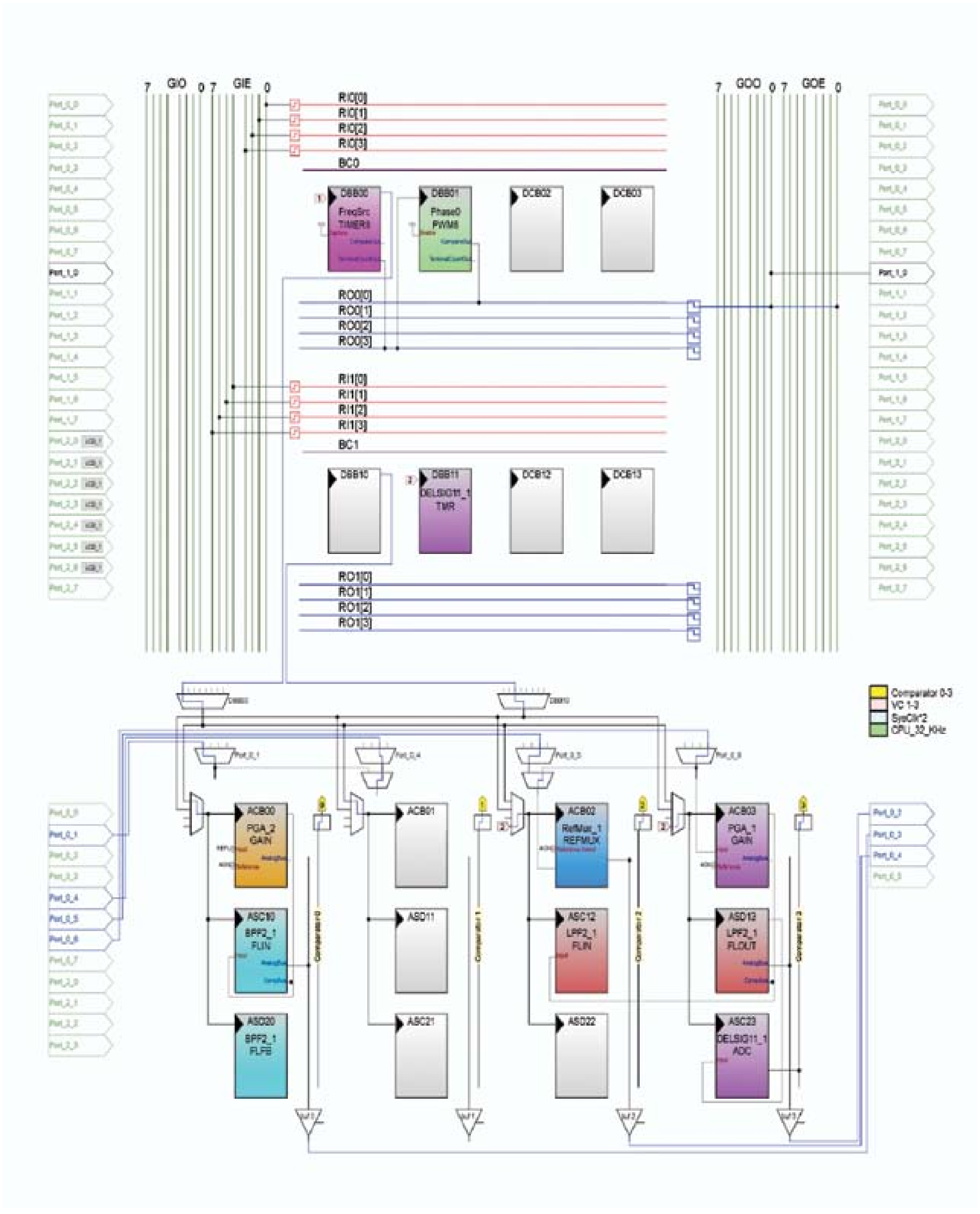


Figure 3 You can use the unlabeled circuit blocks for expansion.

Single microcontroller pin senses ambient light, controls illumination

Loren Passmore, Berkeley, CA

As in a previous Design Idea (**Reference 1**), this design uses an LED as a transducer to measure the ambient-light level and to provide illumination. This Design Idea uses the same principle as its predecessor but consists of only one LED, two resistors, one IC, and one 0.1-µF bypass capacitor. This circuit for providing ambient-light feedback requires no additional components. Despite requiring only a few components, the circuit in **Figure 1** offers considerable flexibility because the microprocessor's software controls the LED's brightness and its relationship to ambient-light levels. For night-light applications, one mode turns on the LED when ambient light decreases. Conversely, for power-saving regulation of a portable device's LCD backlight, a second mode turns on the LED when the ambient-light level increases.

You can download **Listing 1**, sample code for this Design Idea, at www.edn.com/061026di1. The code provides 64 levels of PWM (pulse-width-modulated) intensity control over the LED's brightness in either mode. In operation, one of the microprocessor's multifunction pins drives the LED with a PWM waveform for several hundred milliseconds. After the waveform's final cycle, the software switches the microprocessor's pin to input mode and connects the LED to the microprocessor's internal 16-bit sigma-delta ADC. Ambient light illuminates the LED, producing voltage, which the ADC measures, and the microprocessor computes the PWM waveform's parameters for the next series of illumination cycles. The cycle rate's high repetition frequency eliminates any discernible flickering of the LED.

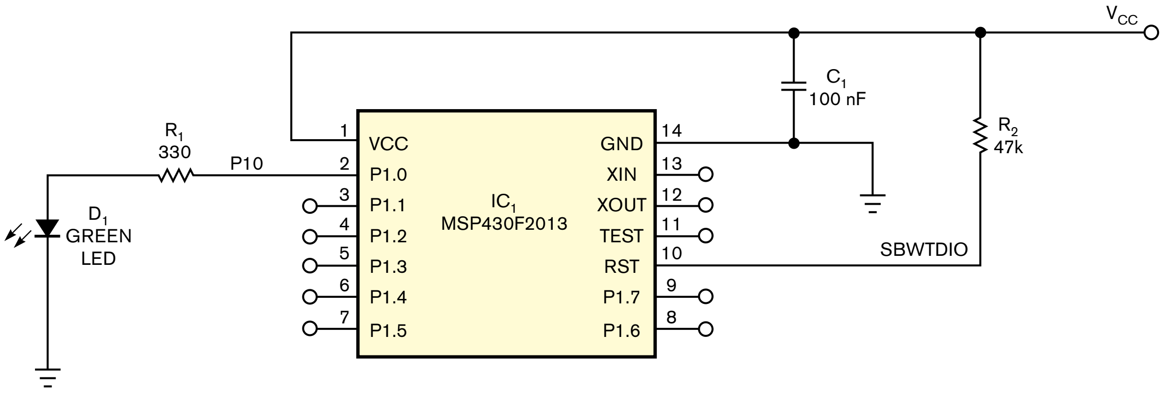
In the **listing**, when the software and ambient-light level specify that the LED should turn off for an extended interval, the CPU goes into a low-power state for 250 msec. During its sleep mode and for a few hundred microseconds while performing ADC conversions, the circuit draws only about 20 µA and thus suits itself well to battery-powered-system applications.

At start-up, the microprocessor stores an initial voltage level, which the LED produces, and uses this value to scale the PWM levels. Shading the LED or moving the circuit into a darker area immediately increases the LED's brightness, which the **listing**'s 64 PWM levels control in small steps. The MSP430F2013's ADC presents input impedance of approximately 200 kΩ. When driving this impedance, an LED occupying a small, 0805, surface-mount footprint generates only a few 10s of millivolts. However, the MSP430F2013's 16-bit ADC resolves the LED's voltage with sufficient resolution to ensure good performance under normal room-lighting levels.

In addition, the MSP430F2013 includes a four-level PGA (programmable-gain amplifier), offering gains of one, four, eight, and 16 to further amplify the LED's minuscule output voltage. The circuit also exploits the microprocessor's onboard low-frequency clock oscillator, which allows low-powered operation without an external crystal. The resultant circuit includes only six components, including a battery. Note: The code can execute on Texas Instruments' (www.ti.com) eZ430 demonstration board without hardware modifications because the board includes an LED connected to port P1.0. **EDN**

REFERENCE

1. Myers, Howard, "Stealth-mode LED controls itself," *EDN*, May 25, 2006, pg 98, www.edn.com/article/CA6335303.



NOTE: IC$_1$'S PINS WITH ——○ INDICATE NO CONNECTION.

Figure 1 An LED, a microprocessor, two resistors, and one capacitor constitute the entire circuit.

Hartley oscillator requires no coupled inductors

Jim McLucas, Longmont, CO

Editor's note: *EDN* originally ran this Design Idea in its June 22, 2006, issue. However, due to a number of schematic and textual errors, we have decided to run a corrected, up-to-date version here. We apologize for the errors and hope this version clears up any and all confusion.

Examine a traditional Hartley oscillator circuit, and you'll note its trademark: a tapped inductor that determines the frequency of oscillation and provides oscillation-sustaining feedback. Although you can easily calculate the total inductance required for a given frequency, finding the coupling coefficient, k, poses technical difficulties and may require experimental optimization, also referred to as the "cut-and-try" method. This Design Idea presents an alternative equivalent circuit that allows you to model the circuit before building the prototype.

Figure 1 shows the Hartley oscillator's equivalent tuned circuit and component values for an 18-MHz oscillator. The mutual inductance is $L_M=k\sqrt{L_1 \times L_2}$. For the equivalent circuit, the equations are: $L_A=-L_M$, $L_B=L_2-L_A=L_2+L_M$, and $L_C=L_1-L_A=L_1+L_M$. The rest of the equations for the equivalent circuit are:

$$C_A=-\frac{1}{(2\pi f_O)^2 L_A},$$

$$f_O=\frac{1}{2\pi\sqrt{(L_B+L_C)C}},$$

and

$$C_A=\frac{1}{(2\pi f_O)^2 k\sqrt{L_1 \times L_2}}.$$

Unfortunately, a truly equivalent circuit requires a negative inductance, L_A. However, for frequencies near the resonant frequency f_0, you can replace the negative inductor with a capacitor as (**Figure 1c**), where C_A replaces L_A. Note that the equivalent circuit's derivation neglects parasitic winding resistances and capacitances.

Figure 2 illustrates an oscillator and output buffer using the equivalent circuit. When constructed, the circuit generally performed as expected from an initial Spice simulation. During testing, several components' values required tweaking, and multiple iterations of Spice analysis ultimately yielded the final design.

The oscillator's tank circuit consists of L_B, L_C, C_4, and C_5, plus the capacitance provided by the voltage divider C_6, C_7, and C_8—approximately 6 pF, including Q_1's and Q_2's input capacitances and some stray capacitance. The total tank capacitance of 66 pF approximates the calculated value of 67 pF. Capacitors that connect to the tuned circuit feature ceramic-dielectric construction with NP0 temperature coefficients.

Inductors L_B and L_C consist of air-core coils mounted with their axes at right angles to each other to minimize stray coupling. However, vibration affects their inductances, and, in a final design, both should consist of windings on dielectric cores or on toroidal cores, providing that the toroids' temperature coefficients of inductance are acceptable for the intended application.

The information in **Reference 1** provided basic designs for both inductors, and adjusting the spacing of their turns tuned the oscillator to exactly 18 MHz. For a more rigorous design, you can measure the inductors before installation, but parasitic effects may require some adjustment of the inductors.

The capacitive voltage divider, C_6, C_7, and C_8, applies the proper signal levels to Q_1 and Q_2. Because the divider's effective capacitance as "seen" by the tank circuit amounts to only 6 pF, you can replace the remaining 60 pF consisting of C_4 and C_5 with a variable capacitor if the design calls for a tunable oscillator. In this example, the output stage consisting of Q_3 and its associated components would require modification to provide more bandwidth if the oscillator requires a tuning range exceeding ±2 MHz.

Capacitor C_3 bootstraps Q_1's Gate 2 to its source, which provides additional gain and reduces Q_1's Gate 1 input capacitance below its already-low value of approximately 2.1 pF (**Reference 2**). An 8.3-μH inductor, L_2, of less than 2Ω dc resistance connects to Q_1's source and presents a relatively high impedance at 18 MHz and provides a dc path from Q_1's source to ground through R_3. At 18 MHz, L_2 has an impedance that consists of an inductive reactance of about 940Ω

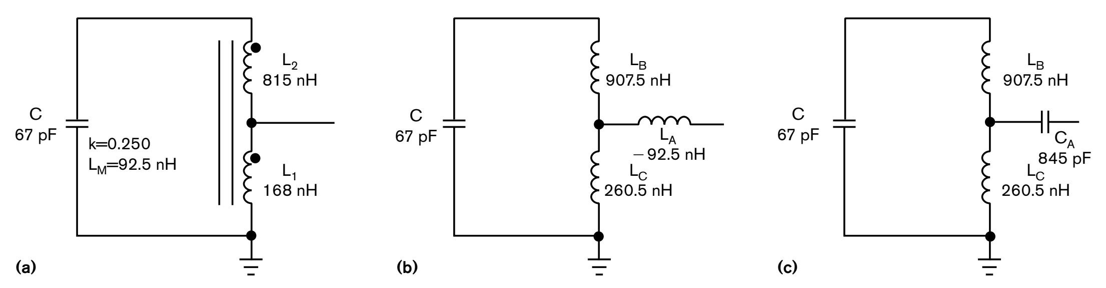
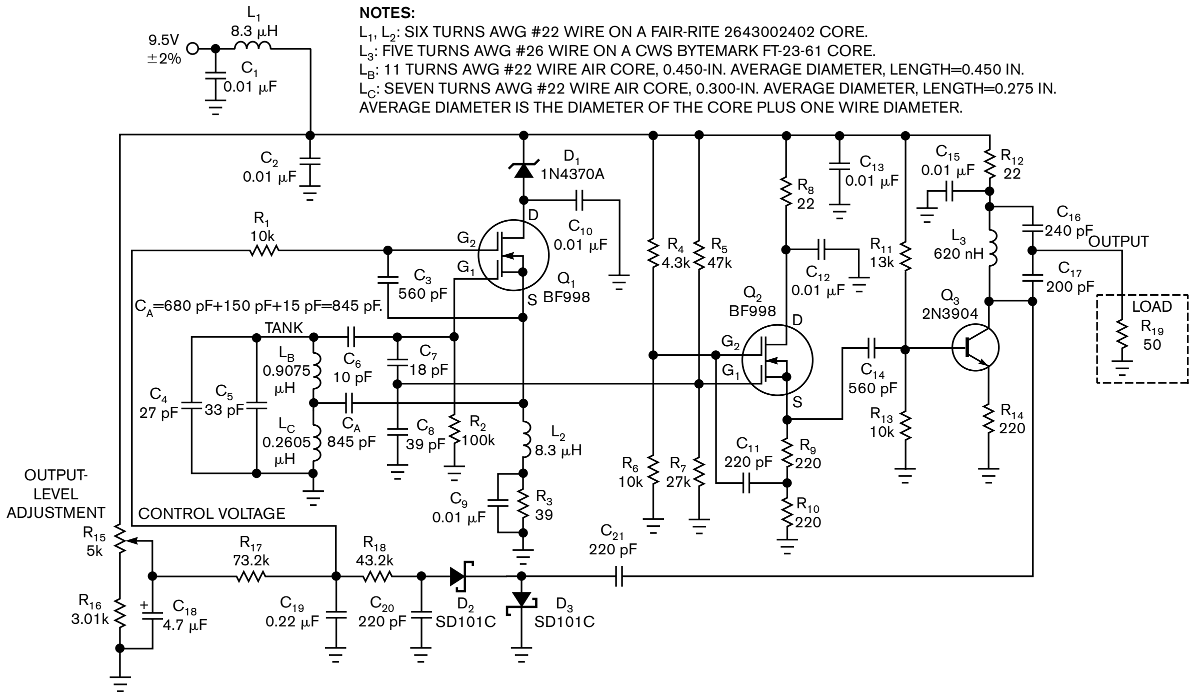


Figure 1 A traditional Hartley oscillator's resonant circuit consists of a tapped inductor and resonating capacitor (a). Allowing for mutual coupling between windings produces an equivalent circuit containing a negative inductance (b). Replacing the negative inductance with a capacitor yields an easily modeled equivalent circuit (c).



NOTES:
L_1, L_2: SIX TURNS AWG #22 WIRE ON A FAIR-RITE 2643002402 CORE.
L_3: FIVE TURNS AWG #26 WIRE ON A CWS BYTEMARK FT-23-61 CORE.
L_B: 11 TURNS AWG #22 WIRE AIR CORE, 0.450-IN. AVERAGE DIAMETER, LENGTH=0.450 IN.
L_C: SEVEN TURNS AWG #22 WIRE AIR CORE, 0.300-IN. AVERAGE DIAMETER, LENGTH=0.275 IN.
AVERAGE DIAMETER IS THE DIAMETER OF THE CORE PLUS ONE WIRE DIAMETER.

Figure 2 This buffered-output, 18-MHz oscillator features a resonant circuit that doesn't rely on mutual coupling for operation.

in parallel with a resistance of about 3.5 kΩ, which results in a very-low-Q choke. Provided that its inductance and reactance approximate L_2's original values, you can substitute a physically smaller inductor for L_2. Inductor L_1's properties are less critical, but it should present a low Q of 4 to 6 and a dc resistance of approximately 5Ω or less. You can use a standard-value choke for L_1 if it meets these requirements.

Source follower Q_2 drives the output stage, which uses a pi-matching network to transform the 50Ω output load to 285Ω at the collector of Q_3. Bootstrapping Q_2's Gate 2 by one-half of the stage's output voltage increases the source follower's gain and dynamic range and reduces its input capacitance.

You can use potentiometer R_{15} to adjust the circuit's output level from about 0.9V p-p to approximately 1.5V p-p across a 50Ω load. At a constant room temperature of about 23°C, the frequency remains stable, and the circuitry that controls output level remains stable even with no load on the output. For a fixed-frequency application, the output circuit's loaded Q of 4 provides adequate bandwidth to eliminate retuning of the output circuit for small changes in frequency.

To set the output level to a safe maximum, connect a 50Ω load to the output, and then adjust the output to 1.5V p-p. The drain-to-source voltage applied to Q_1 will remain at a safe level for all loads from 50Ω to no load, even though the output-voltage level increases as the load resistance increases. To avoid exceeding Q_1's specified maximum 12V drain-to-source-voltage rating, do not exceed an output-voltage setting of 1.5V into a 50Ω load. Note that zener diode D_1 reduces Q_1's drain voltage to provide an additional safety margin.

In a previous Design Idea, an operational amplifier and a diode-rectifier circuit set the oscillator's gain through a control voltage applied to Q_1's Gate 2 (**Reference 3**). In this design, a simple passive circuit serves the same purpose. A portion of the signal at Q_3's collector drives a voltage doubler consisting of D_2, D_3, C_{20}, and C_{21}. Part of the negative voltage developed by the voltage doubler drives the junction of R_{18} and C_{19}, the control-voltage node, which also receives a positive voltage from variable resistor R_{15} through R_{17}, and the resultant voltage sets the output signal level. At start-up, only a positive voltage is present at Q_1's Gate 2, and Q_1's maximum gain easily starts the oscillator. When the output reaches a steady state, the control voltage reduces and maintains oscillation at the signal level determined by the output level control. **EDN**

REFERENCES

1. Reed, Dana G, Editor, "Calculating Practical Inductors," *ARRL Handbook for Radio Communications, 82nd Edition*, American Radio Relay League, 2005, pg 4.32.
2. "Practical FET Cascode Circuits, Designing with Field-Effect Transistors," Siliconix Inc, 1981, pg 79.
3. McLucas, Jim, "Stable, 18-MHz oscillator features automatic level control, clean-sine-wave output," *EDN*, June 23, 2005, pg 82, www.edn.com/article/CA608156.