



NOTE:

ABM312: LIMIT $((6.28m \times F_U / SR) \times (V(IN_1, IN_2) + (V(IN_1) + V(IN_2)) / (2 \times CMRR)), -1m \times V(IN_3) / (2 \times IB), 1m \times V(IN_3) / (2 \times IB))$.

Figure 2 These op-amp model input stages model the input-bias currents of NPN (a) and PNP (b) transistor inputs.