



BY PALLAB CHATTERJEE, CONTRIBUTING TECHNICAL EDITOR

## The wheel goes 'round again

**R**ecent technology and product announcements remind me of the saying, “Everything old is new again.” This phrase has been popping into mind more frequently as industry pundits herald new bottlenecks and incremental solutions to process- and design-tool issues as revolutionary. For design and EDA veterans, again hearing these discussions jogs the memory a bit.

Leading issues in design-verification tools have changed from those involving specialized hardware platforms with software, to hardware emulation, to just software tools on stand-alone stations. The first generation of EDA comprised hardware-and-software vendors, such as Daisy Systems and Mentor, which were promoting optimized hardware platforms to effectively use their software. Today's designs run on general-purpose hardware, but, due to data size, specialized hardware is still sometimes necessary to meet schedules. The most recent entries in this area are Brion's OPC/PSM (optical-proximity-correction/phase-shift-masking) products and Mentor's Calibre nmOPC product, which can now support hyperclusters of multicore-cell processors. As with the past models, hardware and information-technology costs can exceed the costs of the software running on them.

The advent of 45-nm processes returning to metal-gate CMOS; the industry's embrace of immersion lithography; the emergence of machine-specific, model-based OPC; and the use of topology- and orientation-based design rules are reminiscent of the greater-than-10-micron, metal-gate-MOS days. Those were the days of machine-

specific contact-printing rules; serif and notch insertion for critical-layer imaging; and pre-EPI (epitaxial-silicon), pre-implant (spun on dopants) wafer processing. Breakthroughs stabilized these flows, and, given time, the same should result for 65-nm and smaller processes.

Process modeling and characterization are also undergoing a spin of the wheel. Due to the costs of running and testing the cells, engineering is shifting from kit parts or silicon-proven macro-cells, primitive cells, and blocks to simulation-verified designs. This scenario results in a perception that the entire process window can't adequately cover multiple views of the design, including timing, power, noise, ac performance, and leakage. The reality is that most designers have long dealt with the uncertainty of device and macro models, and they have always had to deal with nonstandard views as part of a specification. The short time during which the abstracted models and reduced view analysis were sufficient to complete a design was the exception, not the rule. Thus, the industry is not facing a new design crisis; it's just returning all design engineers to the same task list.

Another crisis the industry's waving around is on-wafer variation. This is

the same issue that existed in the transitional days of 2-in. metal-gate wafers to exotic, 4-in. silicon-gate wafers and at the start of widespread use of EPI on the wafers. Equipment manufacturers spent a lot of time and money on research and development to address these issues, and, with the chip-design groups, they found solutions, so that they have been nonissues for more than 20 years. There is no reason to believe *this* issue is unsolvable.

On the design-verification side, the proliferation of SOCs (systems on chips), with their limited access to internalized signals compared with partitioned systems, has started to shift. This shift is moving from Stage 2, hardware emulation, to Stage 3, a pure software base, with the current generation of hardware/software co-verification, mixed-mode-simulation, and ESL (electronic-system-level) tools. The last big breakthrough in this area was the widespread adoption of scan and BIST (built-in self-test) to improve verification coverage. I am not sure whether ESL is strong enough to completely turn the wheel to its next stop, but it is certainly causing some movement. The industry is still debating the direction of this movement.

Engineers solved everything in the past through a combination of good engineering and perseverance, and they will do so again. Design and manufacturing groups should continue their course of innovation and development through collaborative research and development. And the EDA community should stop declaring every little problem a crisis and every minor product release a revolutionary development. EDA is just one aspect of the engineering chain; it's not the driver for all technology. As soon as the equal collaboration of design, manufacturing, EDA, and IT/communications comes together, we can get on with discussing the impact of product innovation and its benefit to a global society. **EDN**

Contact me at [pallabc@siliconmap.net](mailto:pallabc@siliconmap.net).