



NOTE: CLOCK SIGNAL IS COMMON FOR ALL FLIP-FLOPS.

Figure 1 This circuit implements a 10-bit parallel-output PRBS generator defined by the polynomial equation $x^{31} + x^{28} + 1$. To reduce clutter, the schematic shows only one of 10 exclusive-OR gates that generates the register's feedback signals. A common clock source (not shown) drives all 31 flip-flops' clock inputs.