

2007

EDN DSP DIRECTORY

ARE YOU TRYING TO KEEP TRACK OF THE CONSTANT CHANGES IN THE WORLD OF DIGITAL-SIGNAL-PROCESSING OFFERINGS? THE 2007 DIRECTORY CAN HELP.

THE BEST OF BOTH WORLDS

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www.edn.com/dspdirectory



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elcome to the 2007 *EDN* DSP Directory, which again groups an ever-expanding list of digital-signal-processing resources into a single repository. The number of companies, devices, cores, and offerings in the directory continues to evolve and grow.

A few companies have dropped out due to the closing of business or spin-offs, but the company roster and table of devices are always expanding. This steady growth are a testament not only to the variety of available processing options, but also to the tremendous variation among requirements, features, and applications for which designers use these devices and cores.

Last year, we proposed the term DSC (digital-signal controller) to describe the growing number of hybrid or unified architectures that consist of a microcontroller core with DSP-architecture features and structures. This year, we'd like to highlight this growing segment of the digital-signal-processing universe. DSCs differ from pure DSPs and microcontrollers in that they combine essential features of each type of processor into a single architecture, instruction flow, and device. They support more frequent and faster context switching by including a richer set of on-chip peripherals and interrupt controls than you find on pure DSPs. They also incorporate a richer bus structure and set of arithmetic-execution units for minimizing the chance of computational stalls that a pure microcontroller could suffer when processing a continuous stream of data, such as while processing context switches.

DSCs are making a range of new applications feasible as optimized devices with the right mix of peripherals and data processing integrated into application-specific devices. An early application target for these devices has been the power-supply controller. The balance between the dual nature of DSCs suits them for applications that need to be able to perform complex control functions and perform signal processing at the edges of a system or in small- or portable-system applications. Expect to see more application-specific DSCs for smart-building (automation) applications and portable devices—especially for portable home-medical equipment.

The directory continues to aim to provide designers and system architects enough visibility into processor options to quickly narrow the list of candidate processors for each project. This print version offers a quick and high-level overview of the digital-signal-process-

ing industry by identifying what is new at each company and what applications each company's product lines target.

The DSP Directory is available online at www.edn.com/dspdirectory. There, the "Where did they go?" section helps you find companies that we no longer list because they are out of business, other companies have acquired them, or they've failed to supply us with the updated information we needed for this year's directory. The section also includes data from previous years to make tracking this type of data easier without having to locate earlier versions of the directory.

Further, the Web version expands greatly on the print edition. It offers not only the print material, but also device tables and detailed pages dedicated to each company's devices, cores, development tools, and other product offerings. The detailed device pages support a top-level taxonomy that allows you to find the devices by vendor and by application. These pages also include architectural block diagrams, if available, for each vendor's offerings.

If you cannot find a company in the directory or if a company did not participate in the update, please let the company and *EDN* know that you missed reading about it in the directory. Likewise, if this directory helps you find or choose a device or core, please let the vendor know how you found its part. Help us continue to make the directory better by visiting us at www.edn.com/dspdirectory or by sending your comments and feedback to dspdirectory@edn.com.



ACTEL CORP, WWW.ACTEL.COM

Actel offers single-chip, nonvolatile FPGA technologies along with signal-processing capabilities, such as filtering and domain conversion. The company's Direct-Core system-level IP (intellectual-property) blocks target use with its FPGAs, such as the RTAX-S and ProASIC3 device families. When implemented in Actel's flash- and antifuse-based FPGAs, the flexible IP cores are immune to firm errors and tolerant of radiation. The company's devices support live-at-power-up, which allows them to target military, communication, aerospace, and medical applications that require no power-up delay.

The CoreCORDIC (coordinate-rotation-digital-computer) algorithm, which Actel introduced last year, calculates hyperbolic and trigonometric functions. It also performs coordinate transformations between rectangular and polar coordinates. The tool supports RTL generation, which enables designers to build configurable digital-signal-processing systems. CoreCORDIC supports three architectural options, including a small, bit-serial architecture, a word-serial architecture for moderate performance and size, and a parallel-pipelined architecture for high-performance applications. The CoreCORDIC generator creates a user-defined testbench and RTL model that easily integrates into larger designs. Actel also supports core generation with its CoreFIR (finite-impulse-response) and CoreFFT (fast-Fourier-transform) offerings.

ALTERA, WWW.ALTERA.COM

Altera's portfolio of FPGAs, structured ASICs, and CPLD products targets many traditional electronics markets. Building on the Stratix device family, the new 65-nm Stratix III FPGAs incorporate features, including dedicated DSP blocks, to combine high performance with the lowest possible static- and dynamic-power consumption; these new devices deliver as much as 50% better power performance than the previous-generation high-end FPGA devices. Stratix III FPGA features include Programmable Power Technology, selectable core voltage, process and circuit technologies, and support from the Quartus II PowerPlay power-analysis and -optimization technology. Stratix II GX FPGAs with transceivers feature superior signal integrity and jitter performance, along with the ability to sup-

port optimal protocol implementations.

Altera's recently announced 65-nm Cyclone III FPGAs with 288 embedded multipliers for DSP applications target high-volume applications requiring low power, high performance, and low cost. Hard-Copy II devices give volume-driven-application designers the ability to seamlessly migrate their designs from high-end Stratix series FPGAs to low-cost structured ASICs. The company offers a library of IP (intellectual-property) cores, including the Nios II embedded processor. The Quartus II design software supports all Altera products for FPGA, structured-ASIC, and CPLD designs.

AMI SEMICONDUCTOR, WWW.AMIS.COM

AMI Semiconductor supplies integrated mixed-signal and structured-digital products that target the automotive, medical, industrial, communications, and military/aerospace markets in North America, Europe, and the Asia Pacific region. The company's BelaSigna product family supports high-fidelity, programmable, and ultralow-power systems for portable-audio applications. The company offers a new, miniaturized version of the BelaSigna 200 audio-processing chip that targets small-form-factor, precision-audio products for the consumer and industrial markets.

Innovations for the BelaSigna 200 and BelaSigna 250 DSP-based audio-processing systems include an echo-cancellation algorithm that provides high-quality, echo-free communication in office-telecom headsets and Bluetooth mono and stereo headsets. The company also introduced an acoustic-shock algorithm to mitigate the problems of acoustic shock in products such as communication headsets. The hardware/software combination allows manufacturers to design products that protect users from injury and help employers conform to workplace-safety legislation. The AMIS RPM (Rapid Prototyping Module), featuring the BelaSigna 250 audio processor, enables audio-device developers to evaluate the DSP and subsystems.

ANALOG DEVICES, WWW.ANALOG.COM

Analog Devices' DSP offerings include the Blackfin, SHARC, and TigerSHARC fami-

lies of processors. Development tools for all of the company's processors include VisualDSP++, VisualAudio, and Ez-Kit Lite, as well as tools from SigmaStudio, uClinux, and Green Hills Software. The Blackfin processor family combines a 32-bit RISC-like instruction set with 16-bit dual MAC (multiply/accumulate) units and targets convergent applications with audio-, video-, and data-processing requirements. The devices' dynamic power management enables lower power consumption by supporting the simultaneous adjustment of system operating frequency and voltage under application control.

The new Blackfin ADSP-BF54x family features increased I/O and memory bandwidth; increased on-chip memory; and the integration of high-bandwidth multimedia peripherals, including a 24-bit LCD. The BF54x family also supports CAN (controller-area-network) and MOST (media-oriented-systems-transport) system peripherals for industrial and multimedia/networked in-vehicle-automotive applications, and it embeds new Lockbox secure technology to protect designers' intellectual property: The Blackfin ADSP-BF52x family targets portable applications, including PMPs (portable media players), VOIP (voice-over-Internet Protocol) phones, IP (Internet Protocol) cameras, and mobile TV. The Blackfin family requires as little as 0.16-mW/MHz core power at 250 MHz, and it incorporates Lockbox secure technology for implementing DRM (digital-rights-management)-content protection.

The SHARC processor family targets applications ranging from consumer, automotive, and professional audio to industrial, test and measurement, and medical equipment. Based on a 32-bit floating/fixed-point core architecture, SHARC-family processors implement a sophisticated memory- and I/O-processing subsystem.

The TigerSHARC processor family offers high floating- and fixed-point performance. It supports glueless-multiprocessor scalability targeting wireless-communications-infrastructure, medical- and industrial-imaging, and military applications.

Analog Devices also offers a line of precision analog microcontrollers with ARM7 or 8052 cores that integrate analog components, such as converters, voltage references, and temperature sensors with the processor core and embedded flash memory. New to the portfolio are



the ADuC703x family of precision battery monitors for automotive applications and the ADuC7128 precision analog microcontroller for motor-control and smart-sensing applications in industrial- and automotive-system designs.

Analog Devices SigmaDSP audio processors provide a single-chip audio system with a 28/56-bit audio DSP, ADC, DACs, and microcontrollerlike control interfaces. Signal-processing elements include equalization, crossover, bass enhancement, multiband-dynamics processing, delay compensation, speaker compensation, and stereo-image widening. You can use this feature to compensate for the real-world limitations of speakers, amplifiers, and listening environments.

ARC INTERNATIONAL, WWW.ARC.COM

ARC International licenses configurable media subsystems as well as ARC 600 and ARCCPU/DSP cores that enable SOC (system-on-chip) designers to target a range of embedded-system applications. ARC has nearly 140 customers that collectively ship almost 200 million ARC-based units per year to high-growth markets, such as consumer electronics, wireless communications, voice/data networking, and storage.

The ARC 600 ultralow-power cores implement a five-stage pipeline, and the family of cores targets battery-operated and cost-sensitive consumer, networking, and automotive applications. The ARC 700 high-performance cores implement a seven-stage pipeline, which targets computationally intensive graphic, media-codec, and packet-processing applications. The ARC 700 cores support high-end embedded operating systems.

ARM, WWW.ARM.COM

The ARM OptimoDE data-engine licensable IP (intellectual property) has an associated tool environment that combines the efficiency of fixed logic with the benefits of software programmability. Designers can optimize the data-engine architecture to support classes of applications; for example, the AudioDE is tuned for digital-audio processing. Designers can program the architecture to support multiple algorithms with similar requirements using the same

data-engine hardware. The devices can accommodate incremental design changes or alternative algorithms with software changes without altering the underlying hardware architecture.

ATMEL, WWW.ATMEL.COM

Atmel bases its DSC (digital-signal-controller) families on its new AVR32 UC3 core, its AVR32 AP7 core, and ARM's ARM926EJ-S core, as well as on a family of dual-core VLIW (very-long-instruction-word) floating-point DSPs that it bases on its mAgic core. The AP7000 DSCs implement a seven-stage pipeline that supports out-of-order execution and SIMD (single-instruction-multiple-data) instructions. Atmel's ARM9-, AVR32 AP7-, and AVR32 UC3-based DSCs implement the same peripheral set, which includes DMA on all peripherals, Atmel's peripheral DMA controller, a multilayer high-speed-bus architecture, an Ethernet MAC (media-access controller), a USB host/device, an ADC, serial-communication peripherals, and an optional external bus interface.

The new UC3 Series A family of 32-bit flash DSCs delivers 80 DMIPS (Dhrystone millions of instructions/sec) at 66 MHz and consumes 40 mA. It has 220 freely intermixable 16- and 32-bit extended instructions that include single-cycle MAC operations, multipliers, atomic memory manipulation, and load/store instructions with on-the-fly data manipulations, such as load-and-insert bit fields, load and swap, and store and swap. The three-stage pipeline integrates single-cycle read/write SRAM with a direct interface to the CPU or AHB (Advanced Microcontroller Bus Architecture high-speed bus). The execution stage's three subunits are an ALU, a multiplication unit, and a load/store unit. UC3 Series A DSCs have 256 to 512 kbytes of on-chip, dual-bank flash that can output one word every clock cycle with or without a wait state.

CAMBRIDGE CONSULTANTS, WWW.CAMBRIDGE CONSULTANTS.COM

Cambridge Consultants' expertise ranges from semiconductors, wireless communications, radar systems, advanced sensors, and control systems in automotive electronics, medical devices, and con-

sumer goods. The company has extensive IC-design capabilities, particularly in high-precision analog-, mixed-signal, and RF systems.

The company's portfolio of IP (intellectual-property) and development tools includes a library of analog, digital, mixed-signal, and wireless IP cores along with embedded-software-development and debugging tools, protocol stacks, and design platforms for ASICs and FPGAs. The IP cores are portable and flexible, and designers can tailor them to their specifications with flexible licensing contracts that can be royalty-free. Cambridge Consultants' silicon-IP offering includes 16- and 32-bit XAP processor cores and the APE2 configurable-data-path DSP.

CEVA, WWW.CEVA-DSP.COM

Ceva shipped more than 190 million customer chip sets in 2006 with Ceva IP (intellectual property), a 45% increase over units shipped in 2005. Last year, Ceva introduced the Ceva-X1622 DSP core and the Ceva-XS1102 system platform. Ceva also introduced the Ceva-X1641 as the first Quad-MAC (multiply-accumulate)-unit DSP core in the scalable Ceva-X family, which executes highly computationally intensive tasks that require substantial data throughput and high memory bandwidth.

Ceva continues to offer products it bases on the Ceva-TeakLite-II DSP core. The low-power, low-cost, programmable Xpert-TeakLite-II DSP subsystem targets 2/2.5G-wireless, portable-multimedia-player, consumer- and professional-audio, VOIP (voice-over-Internet Protocol), VOP (voice-over-cable), VODSL (voice-over-digital-subscriber-line), and VOFTH (voice-over-fiber-to-the-home) applications. The Ceva-VOP (voice-over-packet) platform targets cost-sensitive residential and consumer VOIP products. The Ceva-Audio fully synthesizable soft IP targets high-performance, low-power audio applications, such as portable audio players, cellular handsets, and home-entertainment systems. Ceva implements its Mobile-Media2000 platform, which it based on the Ceva-X1620 DSP, on a 130-nm process from United Microelectronics Corp with operating speeds that exceed 400 MHz.

Ceva also offers the Ceva-X-, Ceva-X1620-, Ceva-XS1100-, and Ceva-XS1200-based DSP cores and platforms



for licensing. The multipurpose Ceva-X architecture enables multiple derivative cores targeting 2.5/3G multimedia phones, PDAs, digital cameras and camcorders, DTVs (digital televisions), set-top boxes, and HD-DVD. The Ceva-X1620 is the first implementation of the Ceva-X architecture family. The low-power Ceva-XS1100 SOC (system-on-chip) platform targets 3G wireless-baseband designs. The low-power Ceva-XS1200 SOC platform targets high-performance applications, such as multimedia, communications, VOIP, and storage.

CHIPWRIGHTS, WWW.CHIPWRIGHTS.COM

ChipWrights did not provide an update to this year's directory. The fabless-semiconductor company offers video-processing technology to reproduce lifelike imagery in mobile personal-entertainment products, digital-video/digital-still "dual cams," and high-demand video applications, such as security cameras and digital television. The CW5521 SIMD (single-instruction-multiple-data) processor combines a RISC processor; a parallel processor with 16 32-bit datapaths; enhanced video-sensor features; and USB, audio-codec-compact-flash, and secure-digital-card interfaces.

CIRRUS LOGIC, WWW.CIRRUS.COM

Cirrus Logic offers DSPs for audio applications. The company's portfolio includes single-core and multicore DSPs for consumer markets, as well as CobraNet audio-system processors for professional, commercial, and consumer markets. These devices feature the vendor's CobraNet technology for delivering uncompressed digital audio over Ethernet networks. The company offers a comprehensive library of audio algorithms, including THX Ultra2, DTS ES (digital-theater-system extended surround) 96/24, Dolby Surround Pro Logic IIx, and a modular programming environment for easy customization. The framework includes state-of-the-art decoders, virtualizers, surround simulators, and audio-enhancement algorithms.

Cirrus Logic this year introduced the CS48520/40 DTV (digital-television) au-

dio processors, which offer a set of audio features and improved performance for DTV applications. To assist in the programming of this and other 32-bit audio DSPs, the company released a graphical programming tool that enables quick custom programmability of the basic audio parameters.

CLARKSPUR DESIGN, WWW. CLARKSPUR.COM

Clarkspur Design did not provide an update to this year's directory. The company offers 16-, 24-, and 32-bit DSPs. Clarkspur's emulator boards support USB-cable controls, and the company offers license-free audio-compression programs, such as OggVorbis.

CRADLE TECHNOLOGIES, WWW.CRADLE.COM

Cradle Technologies is a fabless-semiconductor company that develops multicore DSPs targeting next-generation multimedia applications. Cradle delivers high-performance scalable DSP-programmable platforms for video and imaging in security and surveillance, high-performance imaging, and broadcast and IPTV (Internet-Protocol-television) infrastructure applications. The CT3616, Cradle's flagship multicore system, can provide real-time encoding of Main Profile H.264 at standard-definition resolution on one chip.

Cradle's new Janus PCI DVR, a production-ready, low-cost reference design, features the high-performance CT3616. Janus distinguishes itself in the surveillance-DVR market with the ability to simultaneously encode as many as 16 channels of video and audio using a single CT3616 multirate DSP and also reserves headroom for intelligent video-content-analysis applications or playback.

Cradle recently released the latest version of its multicore-development tools. The software-tool suite comprises Cradle's Eclipse-based IDE (integrated development environment), supporting project-management automation and code development in C, C++, and C-like assembly; the Inspector graphical-debugging environment; the graphical runtime-analysis multicore-profiling tool; and an extensive library of modules for video, image, and I/O processing.

EVATRONIX, WWW.EVATRONIX.PL

Evatronix offers IP (intellectual-property) cores and electronic-design services, including a range of processor, USB, serial-interface-controller, data-communication, and networking cores. The company offers two families of programmable DSP cores. The 16-bit C32025 family targets industrial, home, and consumer applications, and the 24-bit C56000 core targets more complex and accurate applications, such as audio compression and image processing.

FREESCALE SEMICONDUCTOR, WWW.FREESCALE.COM

Freescale Semiconductor offers programmable DSPs that target audio, mobile-handset devices, and advanced communications-infrastructure equipment. The company's MXC architecture separates the two primary domains of a cell phone into a modem core that communicates with the base station and an application core that drives the user interface. The MXC family includes platforms targeting 2.75G and 3G mobile applications. The Symphony family of DSPs targets high-fidelity professional-, consumer-, and automotive-audio applications. Freescale continued to enhance and expand its 16-bit DSC (digital-signal-controller) portfolio, which it built on its flagship 56F8000 DSC family.

Last year, Freescale introduced the quad-core MSC8144, which it based on the SC3400 third-generation StarCore architecture.

HYPERSTONE, WWW.HYPERSTONE.COM

Hyperstone's E1-16XSR/32XSR RISC/DSPs provide seamless, integrated RISC/DSP functions for applications requiring a high-speed microprocessor and a high-performance DSP. These processors feature dual RISC/DSP execution units in a pipelined architecture sharing the same registers. Designers can freely mix RISC- and DSP-specific programming. To support high throughput, the system executes the RISC/DSP instructions with a high degree of parallelism. These processors target telephony, VOIP (voice-over-Internet Protocol) telephony, video,



digital cameras, and general signal-processing applications.

Hyperstone built the HyNet series of HyNet32XS/32S networking processors around the E1-32XSR core. The company then added integrated peripherals supporting Ethernet, real-time-Ethernet, serial, and ATM (asynchronous-transfer-mode) communications; additional internal RAM; video interfacing; PCI support; and DMA. These processors target industrial and wired/wireless-communication applications that require high-speed signal processing, communications, or both, including real-time Ethernet.

Hyperstone's new E2 RISC/DSP incorporates the E1-32XSR RISC/DSP 0.18-micron core with a high-speed serial-communication engine, 32 kbytes of internal SRAM, an SDRAM interface, a multiplexed-input ADC, and interrupt and DMA controllers. This processor is low-cost and highly integrated for cost-sensitive applications. Its target applications are audio, consumer, and general-purpose signal processing. Hyperstone also introduced a development-tool set for its processor line, basing it on the Eclipse IDE (integrated development environment), including the GNU tool set.

IMPROV SYSTEMS, WWW.IMPROVSY.COM

Improv offers the Jazz PSA (Programmable System Architecture) platform, which is a configurable, multiprocessor architecture. Rather than use a fixed processor and instruction set, designers can create their own application-optimized processor cores for their products or application domains. Improv's Jazz Processor VLIW (very-long-instruction-word) architecture provides high performance through parallel execution of operations, targeting computationally intensive applications, such as media processing, digital-signal processing, and communication applications. The Jazz DSP cores are also general-purpose, fixed-point DSP cores for general DSP programming.

The Jazz PSA standard tool suite provides a robust and complete development environment for creating optimized DSP software. Central to this environment is the Jazz PSA compiler, targeting VLIW and DSP optimization. The Jazz PSA standard tool suite is retargetable to any con-

figuration of the Jazz PSA platform. The Jazz PSA composer tool suite, a graphical environment for creating designer-defined DSP cores, enables designers to create these configurations.

Improv offers preconfigured cores that are complete hardware and software implementations for high-growth emerging markets. Jazz Media cores include video-, audio-, image-, and speech-processing implementations targeting consumer-electronics devices ranging from mobile handsets to portable media players to high-definition digital displays. Jazz Voice cores address the needs of the voice-over-packet market, including all points of the voice network.

INFINEON TECHNOLOGIES, WWW.INFINEON.COM

Infineon Technologies offers families of 8-, 16-, and 32-bit microcontrollers, with each family offering digital-signal-processing capabilities. The 8-bit XC800 family offers the on-chip Vector Computer, which is a set of coprocessors that includes a hard CORDIC (coordinate-rotation-digital-computer) module for trigonometric/rotational calculations. The CORDIC module supports Park transforms, angle calculation, and determination of multiply accumulates. The Vector Computer includes an MDU (multiply-divide unit), which performs 16- and 32-bit math independently of the 8051 core. With the CapCom6E (enhanced PWM) and fast ADC, these peripherals redefine the capabilities of an 8-bit controller for motor-control schemes, such as for sensorless field-oriented control.

The 16-bit XC16x family of digital-signal microcontrollers contains a MAC (multiply-accumulate) unit and receives support from a functional DSP library available online from Infineon. The XC16x family is available with onboard flash ranging from 32 to 256 kbytes. It has the same CapCom6E unit as the 8-bit XC800 family, which the ADC may trigger independently of the CPU. These devices target motor-control schemes such as constant-VF, frequency slip, and field-oriented control.

Infineon bases the TC116X family of 32-bit microcontrollers on the TriCore unified-microcomputer/DSP architecture, which operates as a single multitasking engine with fast context switching. Target

applications include servo control, audio-domain digital-signal processing, data communications, modems, automotive systems, and portable systems.

IPFLEX, WWW.IPFLEX.COM/EN

IPFlex offers dynamically reconfigurable processors and design-tool platforms targeting imaging and video, communication/wired, medical, and automotive applications. The company's DAPDNA (digital-application-processor/distributed-network-architecture) incorporates a RISC processor as a controller with a heterogeneous matrix of 300 to 1000 processing elements. The DNA architecture can reconfigure within one clock cycle to deliver to designers flexible, field-programmable, and high-performance processing. IPFlex offers the DAPDNA-2 and DAPDNA-IMS product lines. DAPDNA-IMS products target imaging and video applications, and DAPDNA-2 products target multiple purposes for various applications.

IPFlex offers tools and evaluation boards for developing DAPDNA-based high-performance systems. The DAPDNA-FW II design tools include a Data Flow C compiler that enables developers to describe their algorithms in a C-like syntax, which is partly based on Handel-C, and automatically generates hardware code. IPFlex also offers application IP (intellectual property) to optimize the performance of DAPDNA and assist designers with their end applications.

LATTICE SEMICONDUCTOR, WWW.LATTISEMI.COM

Last year, Lattice Semiconductor introduced two second-generation families of low-cost, 90-nm FPGAs that include dedicated DSP blocks. These families, the LatticeECP2 and LatticeECP2M devices, include hard-DSP blocks that designers can program to implement functions such as multiply, multiply-accumulate, and multiply-add/subtract. The families provide as many as 100,000 LUTs (look-up tables), 168 18×18 multipliers, 5.3 Mbits of block memory, and 16 channels of 3.125-Gbps SERDES (serializer/deserializer). These low-cost FPGAs provide both DSP and SERDES functions.

Lattice also released a number of IP



(intellectual-property) cores that allow the implementation of DSP functions within the LatticeECP2 and LatticeECP2M devices. They support functions including FFT (fast-Fourier-transform) compilers, FIR (finite-impulse-response)-filter generators, Reed-Solomon encoders and decoders, convolution encoders, Viterbi decoders, and turbo-coding functions. The Lattice IP-express tool includes all of these IP cores, allowing users to parameterize and generate IP on their desktops. The IPexpress tool also allows the trial use of IP cores in the design before purchase. Lattice's ip-sLever suite of design tools includes the IPexpress tool.

LSI LOGIC, WWW.LSILOGIC.COM

The LSI Zevio 1020 application processor from LSI Logic targets electronic toys, navigation systems, portable media players, and other mobile products. The chip integrates an ARM9 processor for general-purpose processing; a DSP for multimedial processing, such as H.264 video decoding; a 3-D-graphics processor for enriched content development; and a 2-D/3-D sound processor for MIDI playback and 3-D sound effects. It also integrates video-DAC for direct TV- or LCD-screen output, and an SDIO (secure-digital-input/output) card slot for data storage or peripheral expansion.

The Zevio 1020 uses a multiprocessor architecture that provides the flexibility to use dedicated processors optimized for a variety of tasks. The Zevio 1020 consumes less than 200 mW for 3-D-graphics processing and H.264 video decoding. By distributing the tasks among multiple processors that run at optimal frequencies, the Zevio 1020 optimizes cost, power, and performance. LSI supports custom-SOC (system-on-chip) developments based on the Zevio architecture with a menu of preverified IP (intellectual-property) blocks.

MICROCHIP TECHNOLOGY, WWW.MICROCHIP.COM/DSPIC

Microchip's 16-bit (data) dsPIC DSC (digital-signal-controller) modified-Harvard-RISC machine combines the control advantages of a high-performance, 16-bit microcontroller with the high computational speed of a fully implemented DSP

to produce a tightly coupled, single-chip, single-instruction-stream implementation for embedded-system design. All of Microchip's 16-bit DSC and microcontroller families share the same core instructions (with the DSCs adding DSP instructions to the set), peripherals, and development tools and have compatible pinouts. Microchip released five more devices in the dsPIC30F family, along with 19 members of the newer dsPIC33F family. The cumulative total of dsPIC DSCs in production stands at 43. The dsPIC33F family is growing, with flash memory ranging from 12 to 256 kbytes and pin counts of 18 to 100, in a number of peripheral configurations.

The standout products this year were the dsPIC30F1010/2020/2023 family for SMPSs (switched-mode power supplies) and digital-power conversion, which couples a flexible DSC core with peripherals for the task. The devices' digital PWM, ADC, and analog-comparator modules tie together to form an Intelligent Power Peripheral. The digital PWM provides 1-nsec resolution over seven PWM modes. This configuration is essential for SMPS applications and enables a broader range of applications, including isolated dc/dc converters, power-factor correction, uninterruptible power supplies, and digital lighting. The onboard 2M-sample/sec ADC can be precisely timed. The onboard analog comparators can terminate the PWM pulse early for "cycle-by-cycle current limiting"—a key feature for current-mode and next-generation power supplies. Finally, the DSCs are available in packages with 28 to 44 pins and as small as 6×6 mm, including the internal flash memory and including the peripherals necessary for single-chip operation.

A new feature Microchip introduced for all dsPIC DSCs is CodeGuard secure-segmented-memory protection, which allows multiple parties in a collaborative-system design to share the memory, interrupts, and peripherals of one chip, without compromising their IP (intellectual property). This memory segmentation reduces system costs for OEMs and their design partners by eliminating the need to store programs on separate chips. These features enable code protection in a secure-memory segment, separate from upstream code, that tailors the code to an application. Alternatively, you can use



CodeGuard security for secure firmware updates.

MIPS, WWW.MIPS.COM

MIPS Technologies offers embedded-processor architectures and cores targeting digital-consumer, networking, personal-entertainment, communications, and business applications. The company licenses its 32- and 64-bit RISC-IP (intellectual-property) architectures and 32-bit processor cores to semiconductor companies, ASIC developers, and system OEMs. Industry-standard tools, software, and services support the MIPS architecture; more than 120 companies have licensed MIPS IP processors for inclusion in their SOC (system-on-chip) designs.

The MIPS32 24KE and MIPS32 34K core families feature DSP extensions for improved signal-processing performance. The 34K cores are the first to integrate the MIPS MT (multithreaded) ASE (application-specific extension). The architecture improves processing throughput by feeding additional threads into the pipeline as one thread stalls for memory accesses or for other shorter-term pipeline stalls.

MORPHO TECHNOLOGIES, WWW.MORPHOTECH.COM

Morpho Technologies did not provide an update to this year's directory. The company focuses on processing engines for software-defined radio. Morpho Technologies offers MS2, a platform for ultralow-power software-multimode radio, targeting applications such as handsets. In addition, Morpho licenses a WiMax (worldwide-interoperability-for-microwave-access)-system product through integrated hardware and software IP (intellectual property), and it includes the MS2 PHY (physical-layer) communications engine.

NXP SEMICONDUCTORS, WWW.NXP.COM

Last year, Philips spun off its semiconductor business to form NXP Semiconductors. The new company retained ownership of the Nexperia family of media processors, which targets connected multimedia products in the mobile wireless, audio, imaging and video, and consumer markets. Forming the DSP component of the Nexperia brand

is NXP's Adelante technology, which includes the classic 16-bit RD1602x and 24-bit RD2412x DSP cores with a user-definable VLIW (very-long-instruction-word) architecture. The high-performance Adelante VD3204x Embedded Vector DSP family rounds out NXP's offering. With its innovative vector-processing architecture, which minimizes power consumption, the VD3204x targets highly computationally intensive functions in communication and broadcast-reception applications. Adelante provides its DSP technology with the Adelante software-development kit, a verification environment for multicore SOC (system-on-chip) architectures.

ON DEMAND MICROELECTRONICS, WWW.ODM.AT

ODM (On Demand Microelectronics) offers IP (intellectual property) and SOCs (systems on chips) targeting the upcoming global digital-video revolution. The basis for ODM's product portfolio is the silicon-proven VSP (vector-signal processor)—a scalable, configurable, and fully software-programmable processor. The VSP is most suitable for handling applications of DSP with extremely high-performance demands, such as digital video. One of the primary IP cores the ODM offers is SVEN (Scalable Video Engine). SVEN can handle high-definition, multistandard-compliant video-codec implementations for resolutions as high as 1080i/720p. Supporting SVEN, ODM offers Pictor, a high-end image-processing platform, and Samba, the first IP for multistandard baseband processing on the market. The latest implementation is SVENm, a 90-nm multimedia chip targeting mobile applications.

PICOCHIP, WWW.PICOCHIP.COM

PicoChip did not provide an update to this year's directory. The company offers multi-core-signal-processing products targeting wireless systems and software-defined-radio designs. The company offers a family of processors having 200G-instructions/sec and 40-GMAC (giga-multiply-accumulate)-operation performance with a suite of software-development tools and reference designs. The picoArray is easy to program in a standard, familiar development environ-



ment. The company supplies standards-compliant protocol stacks and software-certified, upgradable reference designs for the WCDMA/HSDPA (wideband-code-division-multiple-access/high-speed-down-link-packet-access) and WiMax/WiBro (worldwide-interoperability-for-microwave-access/wireless-broadband) protocols. The company's PC102 processor is available in volume production.

PIXELWORKS, WWW.PIXELWORKS.COM

Pixelworks did not provide an update to this year's directory. The company designs, develops, and markets semiconductors and software for the advanced-display industry, including advanced TVs, multimedia projectors, digital-streaming-media devices, and LCD panels. Pixelworks' line of programmable BSPs (broadband-signal processors) can handle multiple codecs for high-quality IPTV (Internet Protocol-TV) video and other digital-video applications. The company offers the DreamStream application-reference software for designers using the BSP chips. Pixelworks also offers devices ranging from single-purpose discrete ICs to SOCs that can process and enhance the video signal throughout the entire path in the system.

PHILIPS SEMICONDUCTORS

See the "Where did they go?" section in the online version of this directory at www.edn.com/dspdirectory.

RENESAS TECHNOLOGY, WWW.RENESAS.COM

Renesas Technology's SuperH family includes a series of high-performance 32-bit RISC processors with DSP capabilities. The SH-2A and SH-4A employ a superscalar architecture with a built-in FPU (floating-point unit) for higher performance, delivering as much as 1080 MIPS. The SuperH architecture integrates both DSP and FPU capabilities into a single RISC CPU core to save power and overall system cost. These devices are compatible with the previous-generation devices. Development tools, operating systems, on-chip debugging controllers, emulators, and other tools from third parties support all SuperH processors.

Last year, Renesas introduced three new groups of SH-2A series microcontrollers with an FPU capability. The SH7211F supports an operating speed of 160 MHz and 512-kbyte flash memory, targeting office-automation and consumer products. The SH7263 offers 480 MIPS performance at 200 MHz. Its built-in USB-host interface enables seamless connectivity to digital-audio players and an integrated LCD controller for QVGA-size color screens. The SH7652, which operates at 200 MHz, is the first device to incorporate both a copyright-protection function for IP (Internet Protocol) broadcasting and the DTCP (Digital Transmission Content Protection)-IP standard for high-definition DTVs (digital TVs).

For high-end multimedia, Renesas rolled out two new groups of microprocessors that use the top-end SH-4A CPU core. The SH7764 multimedia processor incorporates a 2-D-graphics engine, an Ethernet controller, a USB-host/function controller, an ATAPI hard-drive controller, and an LCD controller. The SH-MobileR addresses a multimedia need beyond mobile phones, delivering a video- and DTV-enabled technology to car-navigation systems, portable media players, and VOIP (voice-over-IP) video phones.

RC MODULE, WWW.MODULE.RU

The RC (Research Center) RISC/DSP-architecture design center provides silicon IP (intellectual property) for VLIW/SIMD (very-long-instruction-word/single-instruction-multiple-data) processors with a flexible and high-performance, 1- to 64-bit vector-matrix engine. RC Module offers mixed-signal SOC (system-on-chip) design service and application-software development for industrial radio-navigation, consumer standard- and high-definition TV, and other math-intensive applications. Software- and hardware-development tools, as well as real-time signal- and video-image-processing systems are available from RC Module. The company develops smart devices for intelligent-transport systems, such as the TrafficMonitor, a real-time traffic-data-collection and -analysis video system.

This year, RC Module presents the new NeuroMatrix NM6404, a 0.25-micron, high-performance DSP targeting real-time data-flow processing. The company based



the processor, which includes 2 Mbits of on-chip memory, on the advanced VLIW/SIMD NMC2 core. It also supports new software-development tools for the Neuro-Matrix DSP family. The NMServer software provides service access to the boards with NM640x processors from a remote PC.

RF ENGINES, WWW.RFENGINES.COM

RF Engines did not provide an update to this year's directory. The company's cores and SOC (system-on-chip) designs primarily target Xilinx and Altera FPGAs for applications in wireless-communications systems, electronic warfare, spectrum analysis, and medical instrumentation. The standard range of cores includes the HyperSpeed cores for applications requiring 6.4G-sample/sec performance. The HyperLength cores support a 1 million-point transform running at complex sample rates as high as 200M samples/sec on a Xilinx Virtex-II 3000. The Matrix cores include a set of different-length DFT (discrete-Fourier-transform) cores that combine to allow the configuration of an FFT (fast Fourier transform) to match the number of points an application requires.

The ChannelCore64 can extract as many as 64 narrowband channels from one or two wideband ADC inputs. The PFT (pipelined-frequency transform) multi-channel-filter bank targets use in real-time applications. The Polyphase DFT, or WOLA (weighted overlap and add), is a method of implementing a uniformly distributed multichannel-filter bank. The tunable PFT supports on-the-fly reconfiguration to any frequency plan as a digital front end for the telecommunications, defense, and instrumentation markets. The SpectraChip cores provide a digital replacement for analog intermediate-frequency filtering; the digital implementation includes standard features, such as resolution-bandwidth filtering, video-bandwidth filtering, and conversion to log power.

SENSORY, WWW.SENSORYINC.COM

Sensory did not provide an update to this year's directory. The company's RSC family of devices performs recognition, speech synthesis, and general-purpose product control. The RSC line supports speaker-

independent recognition, speaker-dependent recognition, speaker verification for voice biometric security, 2400-bps speech compression for speech playback, and music synthesis.

The RSC-4x family provides on-chip feature integration, including a microphone preamplifier, twin-DMA units, a vector accelerator, and a hardware multiplier that allows you to build a system with little more than a battery, a speaker, a microphone, and a few resistors and capacitors. Multiple ROM options are available.

Sensory's SC-6x series of DSPs offer multiple options for introducing speech and music-synthesis abilities into consumer products. Members of the SC-6x line can store as much as 37 minutes of speech on-chip and include as many as 64 I/O pins for external interfacing.

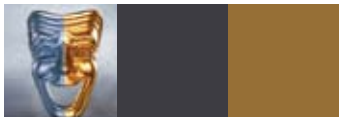
SILICON HIVE, WWW.SILICONHIVE.COM

Semiconductor-IP (intellectual-property) supplier Silicon Hive designs, builds, and licenses application-specific products for communications and media processing, tuned processor cores, and program-development tools with application libraries. Silicon Hive cores target specific application requirements, and they are high-level-programmable from ANSI C.

The company's processor lineup includes the Avispa-CH1, a high-performance, C-programmable data processor for communications-signal processing. The Avispa-IM2 is a general-purpose C-programmable data processor. These processors are scalable to a high level of operations per cycle, with multiple options for precision, I/O, and memory configurations. The C-programmable Moustique-IC2 SIMD (single-instruction-multiple-data) processor targets image-signal processing, with multiple options for SIMD-vector dimension, I/O, and memory configurations. All processors come with a software-development environment, application libraries, and SOC (system-on-chip) integration and verification packages.

STARCORE

See the "Where did they go?" section in the online version of this directory at www.edn.com/dspdirectory.



STMICROELECTRONICS

See the "Where did they go?" section in the online version of this directory at www.edn.com/dspdirectory.

STREAM PROCESSORS, WWW.STREAMPROCESSORS.COM

SPI (Stream Processors Inc) is a fab-less-semiconductor company that offers parallel processing to enable demanding signal-processing applications. The company's technology addresses how to make parallel processing easily accessible to programmers. SPI last year began shipping its Storm-1 family of stream processors, targeting video and image processing in applications such as high-definition videoconferencing, intelligent video surveillance, and multifunction printers.

STRETCH, WWW.STRETCHINC.COM

Stretch offers a family of software-configurable processors with embedded programmable logic within the processor to target imaging and video, mobile/wireless, security, and industrial applications. Using familiar C/C++ programming tools, system developers can automatically configure Stretch's processors to flexibly address diverse markets with changing application needs. Stretch's new S6000 family of software-configurable processors targets high-performance video and wireless-signal processing. The S6 architecture offers three technology innovations that include a second-generation ISEF (instruction-set-extension fabric), a processor array, and a programmable accelerator.

Stretch and its partners offer reference hardware and software applications for main-profile standard-definition- and high-definition-resolution MPEG 2 and H.264 video encoding. Many of the core modules from these applications are available in source code as optimized extension instructions. Stretch and its partners also offer hardware and software applications for WiMax (worldwide-interoperability-for-microwave-access) base-station equipment. A number of the physical-layer modules, including FFTs (fast Fourier transforms), FEC (forward-error-correction) functions, and CRC (cyclic-redundancy check), are available in source code as optimized extension instructions.

Stretch enhanced its IDE (integrated development environment) with the Slickedit text-editor tools and improvements in the compiler and instruction-set simulator. A library of code supporting DSP, wireless-signal-processing, and video- and image-processing functions is available.

TENSILICA, WWW.TENSILICA.COM

Tensilica offers several DSP choices within its Diamond Standard processor line. The new Diamond 38xVDO video engines target D1 (standard-definition) resolution and offer H.264 Main Profile encoding, decoding, or both, as well as VC-1/WMV (Windows Media Video)-9, MPEG-4, and MPEG-2 decoding. The Diamond 330HiFi audio processor includes dedicated audio instructions to decrease frequency requirements. Vendors have ported more than 20 popular audio encoders and decoders to the Diamond 330HiFi. The three-issue, VLIW (very-long-instruction-word), eight-MAC (multiply-accumulate)-operation, SIMD (single-instruction-multiple-data) Diamond 545CK is Tensilica's fastest licensable DSP core. Other Diamond Standard processors, including the 212GP and the 570T, incorporate 16-bit MAC operations for easier DSP tasks.

Tensilica's Xtensa processors are configurable, extensible, and synthesizable. Designers can select and configure predefined elements of the architecture and invent instructions and hardware-execution units to maximize performance. Tensilica's Xtensa LX2 processor core with the Vectra DSP engine supports wide datapaths and traditional DSP tasks. The system can deliver RTL-equivalent I/O through a ports-and-queues mechanism that directly connects to the processor's execution unit to bypass the load/store operation. The Vectra LX DSP engine uses 64-bit instruction words containing three-issue slots for ALU (arithmetic-logic-unit), MAC (multiply-accumulate), and load/store operations.

TEXAS INSTRUMENTS, WWW.TI.COM

Texas Instruments offers a broad portfolio of programmable DSPs. The TMS-320C6000 DSP platform comprises high-performance fixed- and floating-point DSPs targeting video, imaging, broad-



band-infrastructure, and performance- audio applications. TI announced the lowest cost TMS320C6720 floating-point DSP for \$5.75. It introduced the cost-effective, high-performance TMS320C6454 DSP for infrastructure applications, which is an ideal migration path for current C6416 and C6455 DSP developers.

The TMS320C5000 DSP platform offers low standby power and advanced automatic power management. TI announced the TMS320C5506 DSP that requires only 0.12 mW at 108 MHz in standby mode and 1.2V. TI also introduced the audio-optimized TMS320C54HFK DSP for the Hands Free Kit reference design to allow for differentiating features, including audio streaming and speech recognition.

DaVinci technology consists of scalable, programmable DSP-based SOCs (systems on chips), software, tools, and support for developing digital-video end equipment. The latest processors based on DaVinci technology include the TMS320DM643x processors, priced as low as \$9.95 and tuned for automotive vision, video surveillance, and video telephony. TI also recently released the TMS320DM6441 for portable video- and audio-system applications, which require additional power-management features.

The TMS320C2000 DSC (digital-signal-controller) platform combines as much as 150 MIPS of TI's DSP technology with the control-peripheral integration, C-language efficiency, and ease of use of a microcontroller. C2000 DSCs target digital-power supplies, digital motor control, and advanced sensor control in industrial, automotive, medical, and white-goods applications. TI has announced four new hardware- and software-compatible flash and custom ROM-based devices in the C2000 portfolio and four new, low-cost, 32-bit TMS320F280xx devices, offering as much as 60 MHz of performance, with prices starting as low as \$3.25 (1000).

TI's new TMS320F28044 controller targets multichannel POL (point-of-load) applications, such as telecommunications and networking-infrastructure equipment, servers, laptops, and industrial equipment. With 100 MIPS of 32-bit DSP performance, the F28044 programmable controller can manage as many as 16 dc/dc-converter channels for multichannel POL applications. The F28044 controller implements as many as 16 channels of TI's patent-pending high-

resolution pulse-width-modulation technology, each with 150-psec resolution.

TI also introduced new low-cost digital-power-development kits targeting power-factor correction and dc/dc applications. The kits provide off-the-shelf platforms that work seamlessly with the free DPS (digital-power-supply) software library, which offers reference software for key functions in ac/dc, complex POL, dc/ac inverters, and uninterruptible-power-supply applications.

The single-chip, 3-GHz-performing TMS320TCI6487 wireless-infrastructure baseband processor drives down the cost of GSM (global-system-for-mobile-communications)-based base stations and supports emerging WiMax (worldwide-interoperability-for-microwave-access) and TD-SCDMA applications. Targeting pico to macro base stations, the TCI6487 incorporates three DSP subsystems, each with a 1-GHz, C64x+ DSP core.

3DSP

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XILINX, WWW.XILINX.COM

Xilinx offers PLDs and FPGAs. The company's XtremeDSP product includes a portfolio of DSP devices that target high-performance signal processing with software tools that support design development in Matlab, Simulink, and C/C++, along with development kits and reference designs in wireless and video applications. XtremeDSP application-optimized products are available for medical-imaging, military/aerospace, mobile/wireless-base-station, imaging, and video systems.

Xilinx DSP devices include the Virtex-4, Virtex-5, and Spartan-3 family of FPGAs that feature as many as 640 18×25 DSP slices capable of operating as fast as 550 MHz. Software tools such as System Generator for DSP and AccelDSP Synthesis suites make it easier for designers who are unfamiliar with FPGAs to port their algorithms. These tools come with a library of parameterizable DSP algorithms, such as FFTs, a filter compiler, FEC (forward-error-correction) algorithms, and video codecs. Xilinx also provides technical support with a dedicated team of DSP field-applications engineers and a hotline.