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Exploring the foundation under smartphones

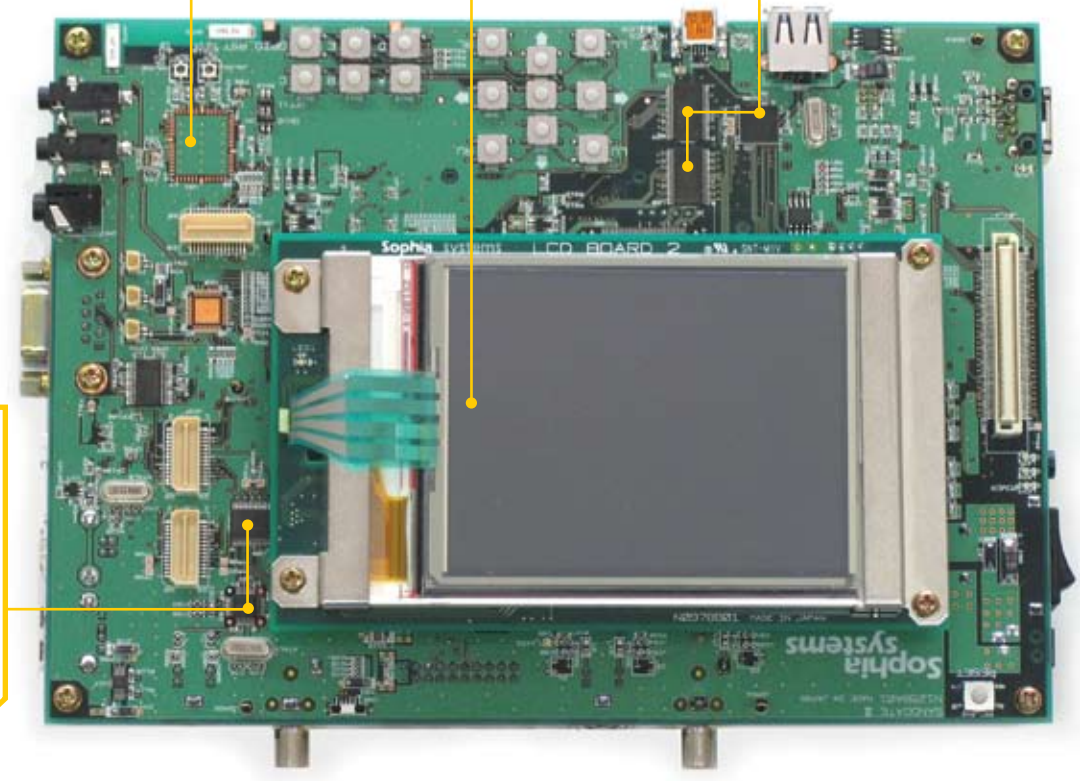
The next generation of smartphones and PDAs will rely on unprecedented integration to deliver their features at the lowest possible bill-of-materials cost. But that doesn't mean they will be single-chip devices. Far from it: Radio chips, baseband processors, and application processors are likely to remain in separate packages. Around that core, a community of memory, support, and interface chips threatens to spring up and choke off the hope of cost control. To get an idea of the complexity of these hardware platforms and the challenge that integrators face, *EDN* looked into a smartphone/PDA reference-design board from Sophia Systems, which the company based on the Marvell PXA320 (codename, "Monahans") integrated application processor. Remember: This board contains no radio or baseband hardware, and the chip it uses contains L2 cache, a DDR DRAM controller, a 2-D-graphics engine, a 768-kbyte frame buffer, an LCD controller, a camera interface, and a host of I/O controllers.

Despite all the I/O capabilities of the Monahans, the board still requires an Epson USB2.0/IDE controller, this pair of NXP 74ALVC164345 3/5V translators, and several other large packages of translation logic. Using multiple voltages saves power, but it quickly populates a motherboard with voltage shifters.

Monahans still requires an external Ethernet controller—in this case, an SMSC 9118 and a Pulse H1066 on the back of the board. There's a landing for a Murata WLAN module, as well.

The board comes with an LCD and touchscreen. Underneath the panel lies the heart of the design: the PXA320 Monahans CPU chip, 64 Mbytes of NAND flash, and 128 Mbytes of DRAM.

Power management is complex. This system provides a CPLD (on a daughtercard on the back of the board) to handle the complexities of power sequencing.



A TI TVP5150 decodes NTSC or PAL video to BT.656 digital data, and a Chrontel 7013 encoder provides the complementary function. More bus translation is necessary here, too.