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Comparator detects position of peaks and valleys in a waveform

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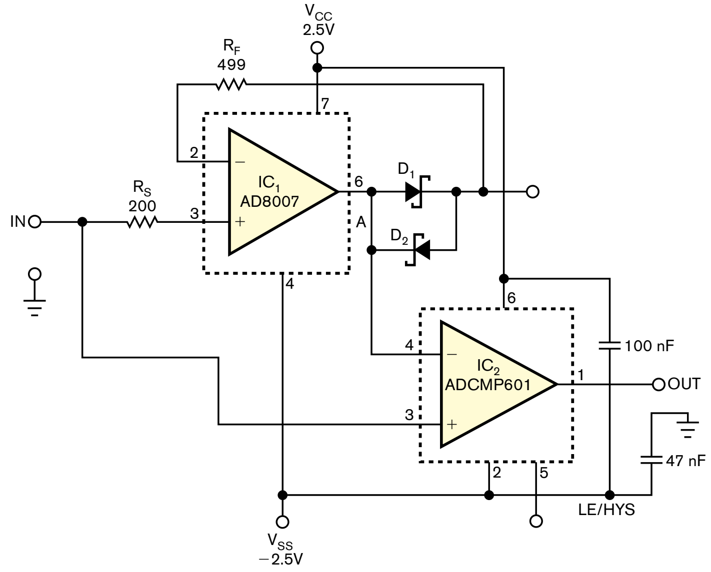
The recent advent of Analog Devices' (www.analog.com) ADCMP60x family of comparators has filled a gap between the less-than-1-nsec-response comparators consuming 100 to 200 mW and those exhibiting approximately 1-μsec response, requiring about one-thousandth that power. The ADCMP60x comparators exhibit a low value of the product of propagation-delay-by-supply-current drain; possess rail-to-rail input and output operation; and offer a variety of options for hysteresis, latch-mode operation, and shutdown mode. Some of them also have inherent level-translating capability. Moreover, the ratio of propagation delays for the positive and negative transitions at the output is close to the ideal value of 1 within 8% tolerance for the ADCMP600, ADCMP601, ADCMP602, and ADCMP603 and with in a 6.7% tolerance for the ADCMP608 and ADCMP609 members of the family (**Reference 1**).

This ratio is important in applications in which both positive- and negative-output-level transitions are equally significant. **Figure 1** shows one such circuit. Voltage-level transitions at the output of the detector indicate changing of the sign of the first derivative of the input signal; in other words, the circuit detects time positions of peaks and valleys in the input-voltage waveform. The detector circuit uses an ADCMP601 for IC$_2$, and IC$_1$ is an Analog Devices AD8007 current-feedback amplifier. IC$_1$ connects as a voltage follower with an antiparallel combination of Schottky-barrier switching diodes, D$_1$ and D$_2$, between the output and the inverting input of the amplifier. Comparator IC$_2$'s inputs connect to the source of the input voltage and to the output of the current-feedback amplifier. This configuration enhances the voltage difference of $V_{IN}-V_A$ between inputs of the comparator. It performs this enhancement in a steplike manner at the instant, or region, at which the sign of slope of the input signal changes. This voltage difference is a measure of the double-forward voltage of diodes D$_1$ and D$_2$ at their forward current, which you derive from V_{IN}/R_F.

You use a current-feedback amplifier as IC$_1$ because a dynamic current flows into its inverting input even when you



NOTE: D$_1$ AND D$_2$ ARE HSMS-282Ls OR HSMS-282Cs.

Figure 1 Comparator IC$_2$ produces an output that switches state at the positive and the negative peaks of the input-voltage waveform.

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connect it as a voltage follower. The values of the R_S and R_F resistors are those that **Reference 2** recommends for a gain of 1. You needn't worry about instability due to the presence of antiparallel diodes in the feedback path of the current-feedback amplifier. These diodes increase the value of feedback resistance to more than 499Ω. Whenever the input voltage is only approximately 0V, the frequency-gain response of IC_1 for an R_F value greater than 499Ω remains flat.

An analysis of the response of the voltage follower in **Figure 1** to a harmonic input voltage uses ω/ω_T and $\omega=2\pi f$, where f is the input-voltage frequency and ω_T is the radial transition frequency of the amplifier. At the radial-transition frequency, the ratio of Z_M (the magnitude of the amplifier's transimpedance) to R_F drops to one. This simplification leads to an **equation** for the delay, t_D, in **Figure 2**:

$$\Delta\varphi = 2\sqrt{\frac{V_F}{V_m}\times\frac{R_F}{r_{m0}}},$$

where V_F is the forward voltage of diode D_1, V_m is the amplitude of input voltage, R_{m0} is the dc transresistance of the current-feedback amplifier, and $\Delta\phi$ is the electrical-error angle in radians. The period of input harmonic voltage, T in **Figure 2**, represents 2π radians. The final error of the detector is $\Delta\phi$, which decreases by a factor of $\sqrt{2}$. This reduction occurs because the necessary operating overdrive over the midpoint of the steplike transition in the $V_A(t)$ voltage that the comparator requires is more than an order of magnitude less than the value of V_F. **EDN**

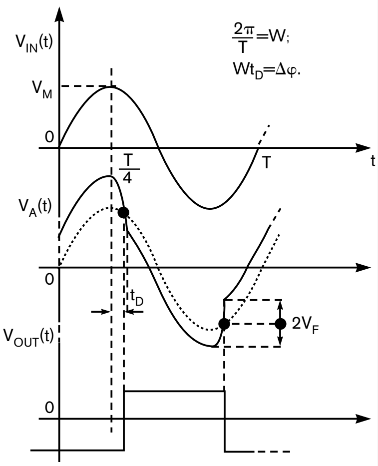

Figure 2 The output of comparator IC_2 switches a slight time delay, t_D, after the positive and the negative peaks of the input voltage.

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Precision integrator sparks current-ratio-to-frequency converter

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The Design Idea in **Figure 1** uses the S_1 switch of the Texas Instruments (www.ti.com) IVC102 precision integrator to select between a single input current or the superposition of two input currents. This function allows you to obtain an output signal whose characteristics directly relate to the ratio between the two input currents. The circuit achieves high accuracy independent of most of the system parameters. In addition, you can enhance accuracy if you let a digital counter control the IVC102-based circuit (**Figure 2**). In this case, the system's output is a number in the BCD (binary-coded-decimal) format proportional to the input-current ratio, realizing a true digital conversion.

The circuit divides into two phases. The first phase begins when the output voltage of the IVC102 becomes slightly greater than the threshold voltage of the LM311 comparator. The comparator generates a falling-edge signal, and the 555 monostable starts a pulse, which closes S_1. In this case, the total input current, I_2-I_1, generates a negative-going ramp if I_2 is greater than I_1. In the delta-time period, ΔT_A, the integrator's output voltage reaches the final voltage value. Hence, $|V_{FIN}-V_{TH}|=(I_2-I_1)\Delta T_A/C_{INT}$, where C_{INT} is the value of the IVC102's integrating capacitor. When the 555 monostable's output pulse ends, the second phase starts: S_1 opens, and input current I_1 discharges C_{INT}. The ΔT_B for the output voltage to assume the threshold voltage's value is then $C_{INT}|V_{FIN}-V_{TH}|/I_1$, and the comparator generates a new trigger command to the monostable so that a new cycle can start. Manipulating the previous **equations** yields: $I_1/I_2=\Delta T_A f$, where $f=(\Delta T_A+\Delta T_B)^{-1}$. This **equation** states that the generated output signal, a train of pulses, has a frequency, f, proportional to the I_1/I_2 current ratio. The accuracy of the monostable directly affects the accuracy of the system. Conversely, the integrating capacitor's and threshold voltage's values do not influence the accuracy if they maintain constant values at least in the 1/f time scale.

You can increase the accuracy of the circuit in **Figure 1** by modifying the section that generates the constant, ΔT_A-wide pulse. The circuit in **Figure 2** generates a ΔT_A-wide pulse using three

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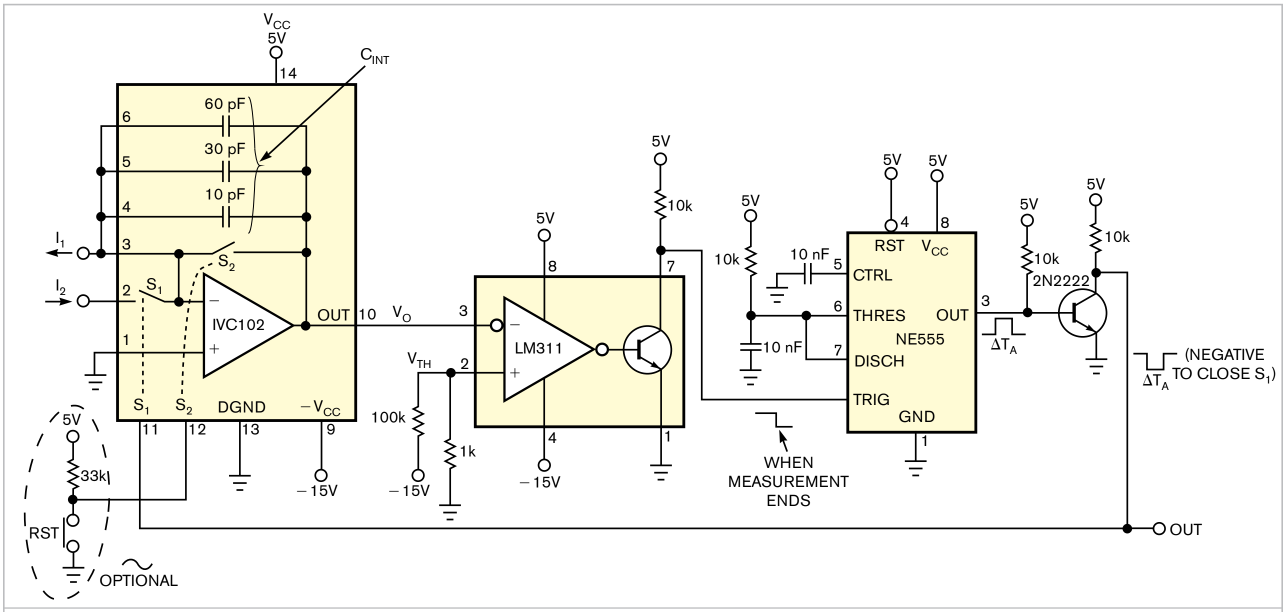

Figure 1 This circuit allows you to obtain an output-signal frequency that directly relates to the ratio between the two input currents.

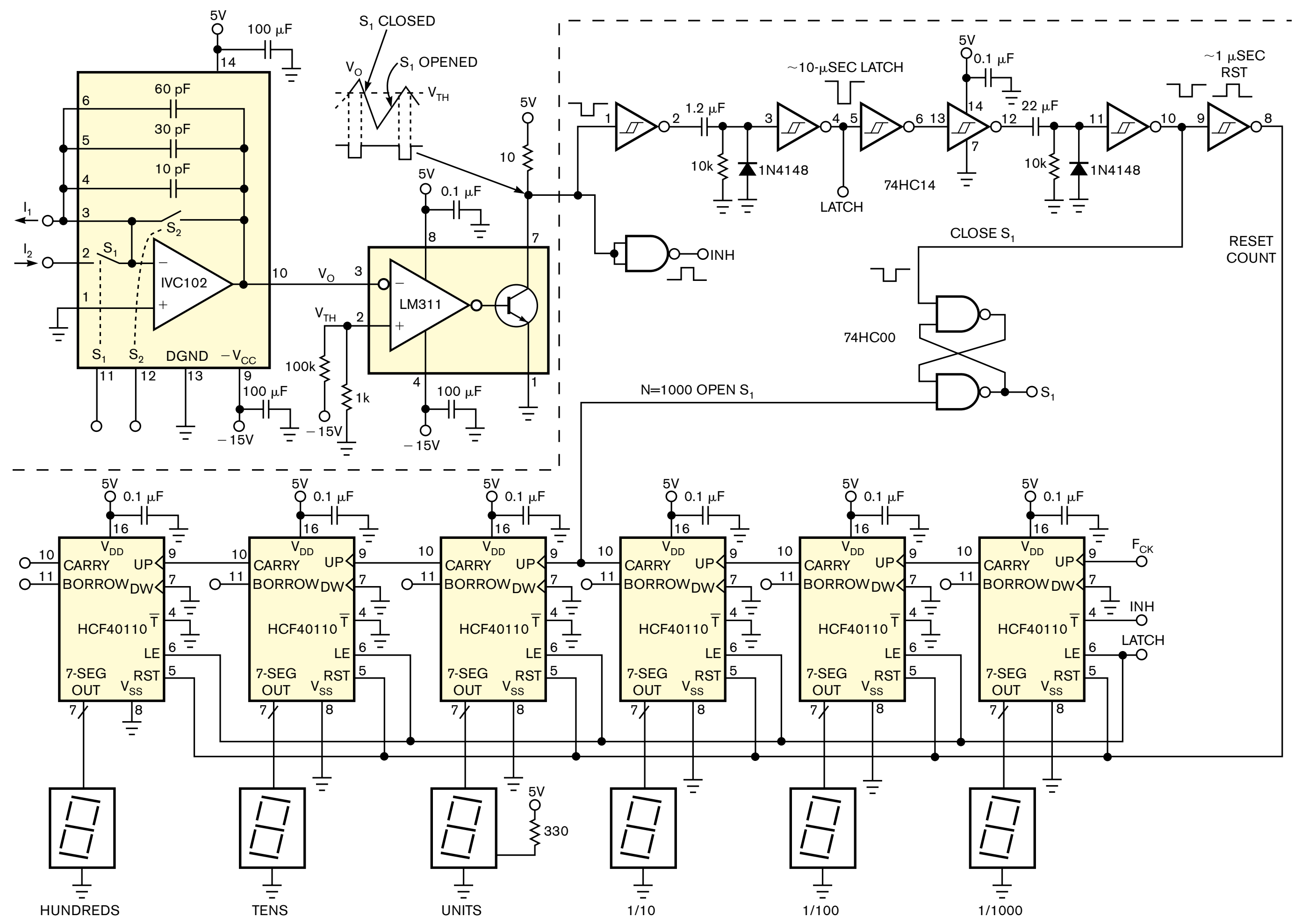

Figure 2 To the circuit in Figure 1, this design adds a BCD counter to obtain direct readouts on seven-segment LED displays.

HCF40110 BCD counters. When the third counter generates a carry, 1000/f_{CK} seconds have elapsed. In **Figure 2**, a set/reset flip-flop controls S_1's state, and the 74HC14 hex inverter with a Schmitt-trigger input generates the pulses that reinitialize the system. A brief description of the measurement cycle follows. When the IVC102's output voltage becomes greater than the threshold voltage, the INH (inhibit) signal connected to the toggle input of the first HCF40110 inhibits counting. At the same time, the negative-going edge of the comparator output generates a negative-going pulse of approximately 10 μsec, which latches the counters' values at the output to display the actual result. After this step, a negative-going pulse sets the SR flip-flop to close S_1. A corresponding positive-going pulse resets the counters. The latch-enable lines of the 40110s are tied high, so the counters' reset doesn't affect the displayed value. When the reset pulse ends and the comparator's output goes high, the HCF40110s can count up. When the third counter generates a carry (negative-going pulse), the 1000th clock period has elapsed, and the SR flip-flop resets to open S_1. The cycle ends at the next falling edge of the comparator's output. The time period in which I_2-I_1 charges C_{INT} is $N_A/f_{CK}(N_A=1000)$, and the I_1 requires for discharging is N_B/f_{CK}. Manipulating the integrator-related relationships yields $I_2/I_1=N/N_A$, where $N=N_A+N_B$. **EDN**

Accurate USB 2.0 temperature sensor needs only a handful of parts

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This Design Idea presents a simple, accurate, and reliable design to measure temperature using the USB. **Figure 1** shows the complete circuit of the temperature-sensor device. The heart of the sensor device is an FT232RQ USB-to-serial converter from FTDI (Future Technology Devices International, www.ftdichip.com). In addition to using the FT232 in its default UART mode, the FT232 works in a so-called bit-bang mode (**references 1**, **2**, and **3**). This mode changes its I/O lines into a bidirectional data bus, which the user can fully control. The connection with the USB takes place in a standard manner, and the back end of the chip interconnects to an AD7814 digital temperature sensor from Analog Devices (www.analog.com, **Reference 4**).

The temperature sensor uses a four-wire SPI but only three pins: SCK (serial clock), SS# (slave select), and SDO (serial-data out). To avoid any malfunction of the sensor, the SDI (serial-data-in) line must be grounded. The FT232 acts as an SPI master and emulates the protocol for the AD7814 by setting or clearing the appropriate port pins for SS# and SCK. The data from the sensor gets read back together with all the other bus lines. This process occurs simultaneously with the write process.

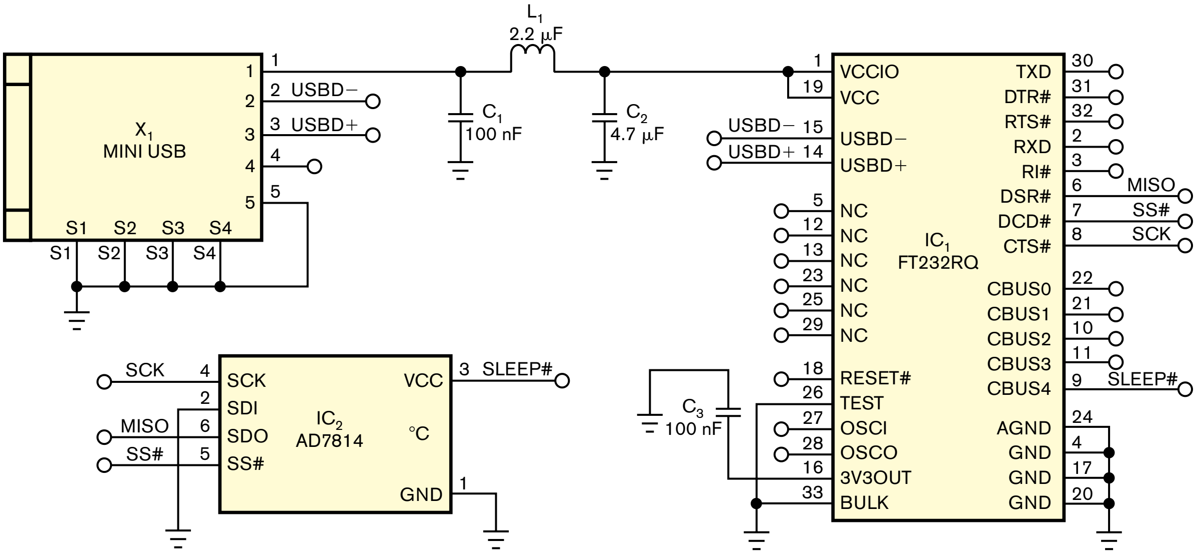

Figure 1 This circuit for a USB temperature sensor works in default UART and bit-bang modes.

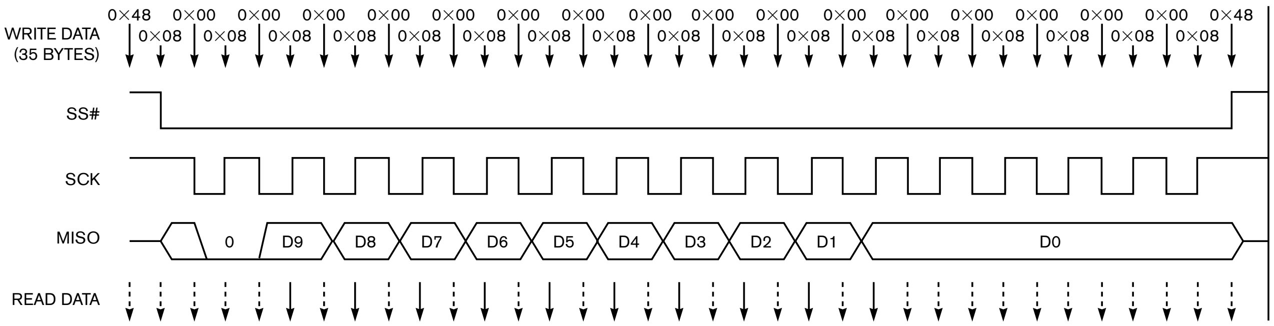

Figure 2 The timing diagram for the AD7814 shows considerable data overhead to download 10 bits of temperature data.

Figure 3 Two sample circuits (left and center) are smaller than a USB Type A plug (right).

To comply with the USB specification, you power down the temperature sensor using the sleep signal while the USB logic is in suspend mode. The sensor device receives its power through the USB and draws only about 20 mA. On the software side, you need only to open the device and switch the chip into the bit-bang mode. After that action, you can send the fixed pattern to emulate an SPI master from the host PC to the FT232 (**Figure 2**). The software returns a data array of the port samples of both the PC and the FT232, whose ports are inputs and outputs.

Because the FT232 chips come with a unique serial number, you can identify the correct device within a multichip environment. So, you can put more than one FT232-based sensor onto a computer. The core of this Design Idea is not limited to measuring temperature. You can use other sensors with digital interfaces, as well.

To get the current temperature, you must write 35 fixed bytes into the port register. The sensor expects 16 clock pulses on the SCK line while the SS# is low. The clock frequency is 1 MHz. The device samples sensor-read data during the write operation. After the protocol on the back end finishes, you can retrieve the data from the host PC for further processing. To get just 10 bits out of the sensor involves considerable data overhead (**Figure 2**). The dashed-line arrows mark the bytes, which need no further evaluation.

This Design Idea realized two sample circuits on a two-layer PCB (printed-circuit board) measuring only 18×12 mm (0.7×0.47 in.) and 7.6×30.5 mm (0.3×1.2 in.). **Figure 3** shows them in comparison to the size of a USB Type A plug. **EDN**

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Integrator enables simple ohmmeter with gigohm range

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The Texas Instruments (www.ti.com) IVC102 precision integrator has high-quality internal capacitors. The circuit in **Figure 1** allows you to measure very-high-resistance values of R_X. A precision difference amplifier, a TI INA105, applies a reference voltage to R_X. During integration, a negative voltage ramp, V_O, is generated at the output of the IVC102. The two LM311s compare the amplitude of V_O with two fixed thresholds and generate the two digital signals: start and stop. The delta time between two such events relates to the system parameters by the expression: $\Delta T=C_{INT}[(V_A-V_B)/V_{REF}]R_X$, where ΔT is the delta time and C_{INT} is the internal integrating capacitance of the IVC102, which external connections on pins 4, 5, and 6 select. (Note: when S_1 is open, $C_{INT}=10$ pF, whereas, when S_1 is closed, $C_{INT}=100$ pF.) The V_A threshold allows the circuit to see the output ramp without any offset on the V_O signal. Because of the INA105 difference amplifier, $V_{REF}=V_A-V_B$, so the previous **equation** reduces to: $\Delta T=C_{INT}R_X$. Also note that the precision of resistors R_1, R_2, and R_3 is not critical. The difference amplifier guarantees the precision of the ohmmeter.

External digital-control circuitry can measure delta time by counting the clock periods between the start and the stop events. At the end, the control circuit can generate a reset signal for the IVC102 to perform a new measurement.**EDN**

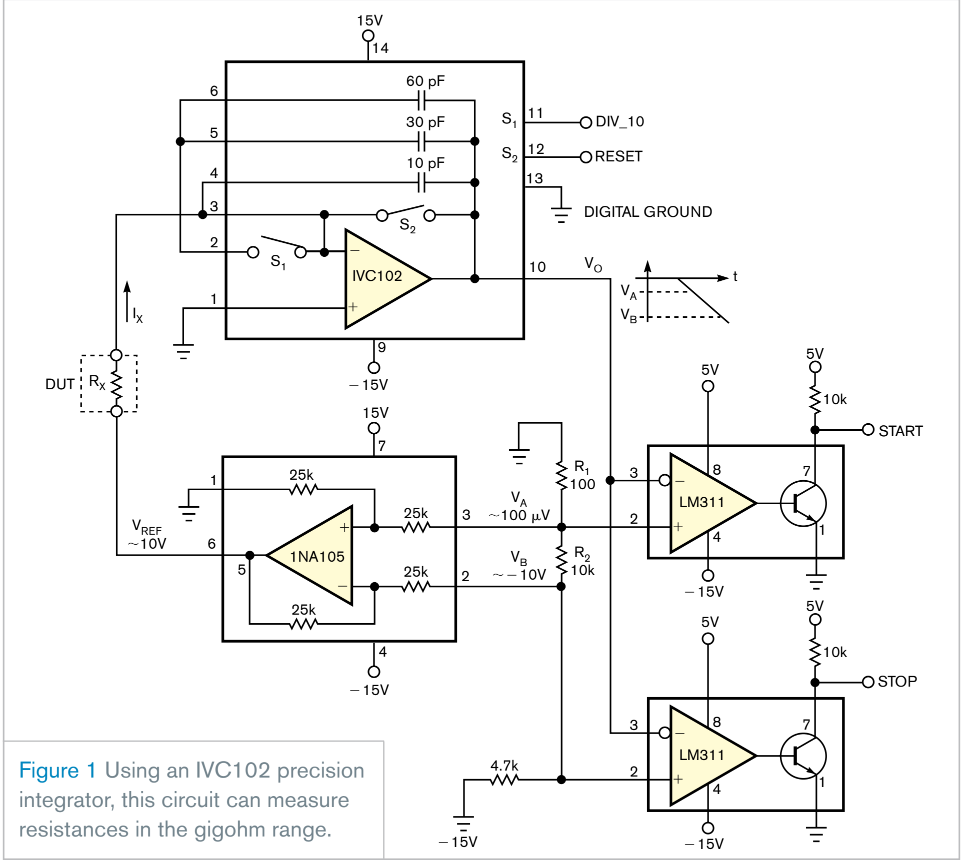

Figure 1 Using an IVC102 precision integrator, this circuit can measure resistances in the gigohm range.