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Confer for continuing education

Early in this decade, popular wisdom had it that professional conferences in the electronics industry were going the way of the dodo bird. Internet Web sites, videoconferencing, and e-mail would put live events out of business.

So much for popular wisdom: Despite the high cost of jet fuel and the high impedance that governments present to air travelers, attendance appears robust at the better professional

conferences in our field. For example, this year, the ISSCC (International Solid-State Circuits Conference) attracted a nearly record-breaking attendance of more than 3600. APEC (Applied Power Electronics Conference and Exposition) *did* break its attendance record with nearly 2800 attendees from 32 countries and more than 1000 organizations.

More important than the numbers, the conference experience is rich, particularly for those of us who are interested in analog and power technologies. Both conferences are IEEE affiliates and are duly famous for the quality of their paper presentations, which make up their schedules' core. Strong educational programs, less-formal panel discussions, and *rap sessions* complement the paper tracks and give attendees opportunities to learn from and interact with peers and leaders in technical innovation.

Though the conferences take different approaches to organizing and presenting their educational programs, educational sessions at both events were at or near capacity this year. I haven't space to fully describe these offerings—see www.isscc.org/isscc/ and www.apec-conf.org for more

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information and announcements of 2008 events—but I'd like to point out one series from each.

ISSCC offered 10 two-hour tutorials scheduled so that attendees could choose as many as two. Attendees received prints of the presentation slides for the sessions they attended and prices were à la carte. Of the 10 tutorials, eight featured analog topics. The strong analog component does not indicate that the ISSCC ignores digital technologies and design challenges. On the contrary, some of the most vexing problems digital designers must face, particularly when designing for 90-nm and smaller process nodes, derive from the awful reality that digi-

tal, though a useful abstraction, is only that: Increasingly, analog effects deriving from fundamental physics limit the performance of digital topologies.

APEC's professional-educational-seminar program comprised 18 three-and-a-half-hour sessions in three blocks. In contrast to the ISSCC's à la carte approach, APEC offers its seminars as a package. Attendees receive the printed slides for all 18 seminars—nearly 2000 in all—and can attend any session they wish without declaring their preference in advance. APEC charges nearly three times the ISSCC's single-session price, which does make negotiating the expense with one's organization a bit tougher. However, the ability to peruse the slides from all of the presentations allows attendees to better compare and assess the value of competing sessions.

Both conferences schedule evening panel discussions or rap sessions. These sessions usually start with position statements from each member of the panel but, with luck and audience participation, rapidly devolve in formality and evolve in depth and breadth. Standouts this year included "Digital RF—Fundamentally a new technology or just marketing hype?" at ISSCC, which Stanford University Professor Thomas Lee moderated, with panelists from UCLA, Infineon, Intel, Texas Instruments, Hitachi, and Silicon Labs, and "If it ain't broke, why go digital?" at APEC, which Darnel Publisher and President Jeff Shepard moderated, with panelists from Microchip, Primarion, Coldwatt, Maxim, and Tyco. Ironically, though the titles of both sessions suggest digital topics, discussions largely centered on analog effects and realities. More surprising was that though power and RF are literally opposite ends of a spectrum, both sessions hit upon a few topics in common.**EDN**

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