BY BONNIE BAKER

Transimpedance strikes again

Multiplying DACs (MDACs) and their postamplifiers bridge the digital and analog worlds. MDACs generate a current proportional to an input digital code (**Figure 1**). The postamplifier converts the DAC's current-output signal to a voltage level. A simple current-to-voltage conversion seems easy to implement with a DAC, amplifier, and resistor. However, this circuit presents stability issues.

For the application, the output model of the MDAC contains a variable current source, resistor, and capacitor (**Figure 1a**). The value of the output resistance and capacitance depends on the input code to the DAC. In general, programming the MDAC to zero scale causes the output resistance, R_D, to be near infinite. When you program the DAC to full-scale or all ones, this resistance is equal to the feedback resistance, R_F. (See the manufacturer's data sheets.) The DAC's output capacitance, C_D, also varies with input code according to the number of internal gate-source junctions across the MDAC output. At full-scale, the MDAC output capacitance equals the data-sheet specification. At zero, the MDAC output capacitance is equal to about half the full-scale value. For stability calculations, use the full-scale output values of R_D and C_D.

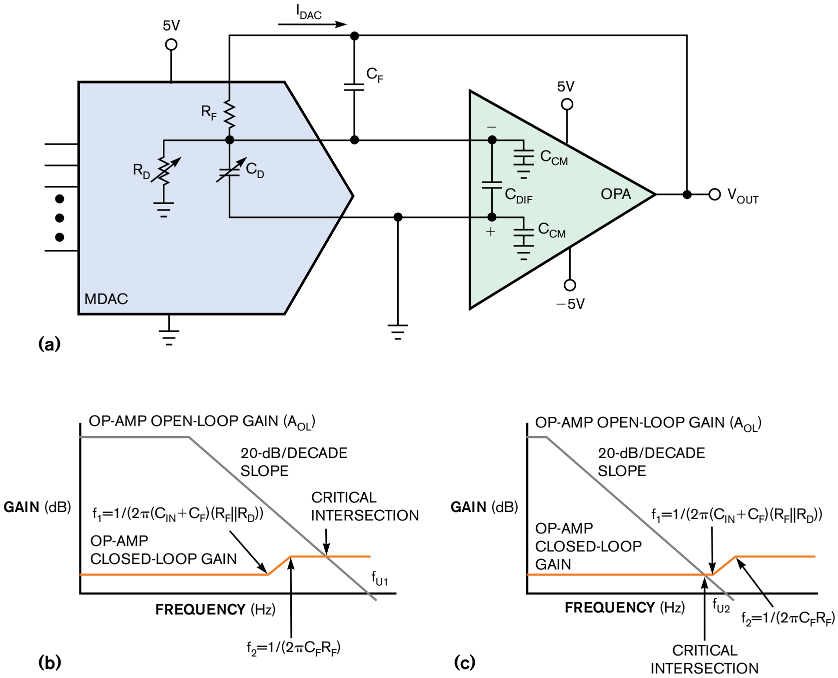

Figure 1 An MDAC output model (a) has a current source, resistor, and capacitor. Frequency responses use high- (b) and low-bandwidth amplifiers (c).

The second subnetwork is the amplifier-feedback network. To maintain precision, most MDACs have a feedback resistor on-chip. The feedback capacitor, C_F, is discrete.

Finally, op amps have a range of specifications, but only a few affect the MDAC circuit's stability: unity-gain bandwidth, f_U; input differential capacitance, C_{DIF}; and common-mode capacitance, C_{CM}.

In this system, total capacitance at the amplifier input is equal to $C_{IN}=C_D+C_{DIF}+C_{CM}$. In **Figure 1b** and **1c**, the closed-loop zero is equal to $f_1=1/(2\pi(C_{IN}+C_F)(R_D\|R_F))$. The closed-loop pole is equal to $f_2=1/(2\pi C_F R_F)$.

You ensure system stability if the rate of closure between the open- and closed-loop-gain curve equals 20 dB/decade. To do so, select an amplifier with unity-gain bandwidth of less than f_1 or greater than f_2.

It is easy to design a stable circuit if f_1 is higher than the amplifier's bandwidth:

$$C_F \geq (1+\sqrt{(1+8\pi C_{IN} R_F f_U)})/2\pi R_F f_U.$$

Alternatively, if f_2 is lower than the intersection of the open- and the closed-loop-gain curve, use:

$$C_F \leq -C_{IN}+1/(2/\pi(R_F\|R_D)f_U).$$

Use these calculated values of feedback capacitance as starting points for your test circuit. Circuit parasitics, device-manufacturing variations, and other factors can encourage you to modify the feedback-capacitor value.

Stabilizing the MDAC's analog signal is critical. However, also consider amplifier noise, input bias current, offset voltage, MDAC resolution, and glitch energy. EDN

Bonnie Baker is a senior applications engineer at Texas Instruments. You can reach her at bonnie@ti.com.