

LISTING 2 CHANGE TO RAM WRAPPERS

```
-- Use port names that make sense (i.e. not library names).
-- Doing so will also make porting libraries easier
COMPONENT ram2048x8
  PORT(
    Q      : out   STD_LOGIC_VECTOR(7 downto 0);
    ADDR   : in    STD_LOGIC_VECTOR(11 downto 0) ;
    D      : in    STD_LOGIC_VECTOR(7 downto 0);
    WRITE_EN : in   STD_LOGIC;
    READ_EN  : in   STD_LOGIC;
    CLK     : in   STD_LOGIC;
    -- BIST
    BIST_IN  : in   std_logic_vector(15 downto 0);
    BIST_OUT : out  std_logic_vector(15 downto 0)
  );

END COMPONENT;

...

u0_ram2048x8 : ram_2048x8
  PORT MAP(
    Q      => data_out_0,
    ADDR   => address_0,
    D      => data_in_0,
    WRITE_EN => write_enable_0,
    READ_EN  => read_enable_0,
    CLK     => clk_0,
    -- BIST
    BIST_IN  => BIST_IN_0,
    BIST_OUT => BIST_OUT_0
  );

#####
# Inside RAM wrapper ram2048x8.vhd for ASIC

xxxx02505008161_instance_0 : xxxx02505008161
  PORT MAP(
    Q      => Q,
    A      => ADDR,
    D      => D,
    -- Best to keep all signals active high until one gets
    -- the library definition.
    WZ     => NOT WRITE_EN,
    RZ     => NOT READ_EN,
    CLK    => CLK,
    -- BIST
    BIST_IN  => BIST_IN_0,
    BIST_OUT => BIST_OUT_0
  );
```