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## Where is the BOM in IC design?

**A**s ICs have progressed to becoming full systems, such as SOCs (systems on chips), they have been mirroring historical development and design issues that occur in PCB (printed-circuit-board) designs of complex systems. These issues include interconnect and power-supply noise, signal coupling between layers, inductance of the interconnect, limitations in size and reliability of interlayer vias,

and stacking issues on multiple layers of interconnect.

EDA tools have faced similar issues, with netlists, physical design, software/hardware-cosimulation requirements, mixed-mode (analog/digital)-simulation requirements, I/O simulation and loading, and autoplacement and routing tools. The industry has optimized the magnitude of devices and the algorithms for each market, but, on a high level, they are similar in function.

For the most part, even the design methodologies have a great deal of overlap in circuit design, design verification, physical design, physical-design verification, and application-interface verification and testing. Traditionally, there has been one major discrepancy in the flows that the industry should correct. BOM (bill-of-materials) costs, along with approved vendor and provider lists, drive PCB-design tools and flows; IC-design flows have no such automated drivers.

Current SOC designs comprise mostly premade parts or component IP (intellectual property). This assembly technique is similar to PCB design for full-system assembly. Rather than a real part, a “phantom” part, such as a symbol or an outline of the part that

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indicates its size, pinout, and functional model, manages the IP in physical design in both areas. Some of the custom-IC parts go down to the individual-device level. For example, rather than have formal outlines, automated routines, such as pcells, create passive components and diodes at physical-design runtime. The IC-design world, however, has no mechanism for visual inspection or validation of the BOM to ensure the replacement of phantoms with the correct real part.

According to a number of high-volume board-design and -manufacturing/assembly companies, the incidence of incorrect vendor parts or missing parts on the board is less than 0.01%. Engineers find most of these problems by optical inspection before the expense of electrical testing and debugging. In stark comparison, more than 20 major IC houses and a large number of major

start-ups report the problem of incorrect component placement or missing devices in a physical design more than once per division, with occurrence rates of greater than 15%. On the IC side, because of the large number of devices, optical checking is impossible; instead, engineers use automated LVS (layout-versus-schematic) tools. The LVS environment has two major drawbacks. First, the tools cannot check nondevice objects that form critical parts of the design. Second, LVS uses black-box methodologies that verify and sign off a design based on an implementation of a phantom that the vendor provides after sign-off.

For some reason, officials at the new generation of semiconductor companies think it is acceptable to design a project, which may cost \$10 million to \$100 million and use \$1 million to \$50 million in tools; work on it for years; and then allow some blind, automated tool the companies don't control to finish the design. The PCB community tends to lack the level of trust in tools and third-party operators.

On a positive note, most of the major IC companies have implemented mandatory *written* sign-off procedures to validate correct linking to approved IP blocks and to make sure that generated devices instead of big shiny spots of bare silicon actually appear on the wafers. These procedures, with rudimentary automation, have resulted in an average schedule reduction of 22%. Most smaller companies have not yet implemented such procedures. One can only estimate the schedule reduction and yield improvement that would be possible if automation methods for the PCB community were available to the IC world. Unless customers require tool and IP providers to support this feature, we remain in a semiconductor chain that maximizes profit for the foundries, test vendors, and tool providers, rather than for the design and end-customer-support side. **EDN**

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