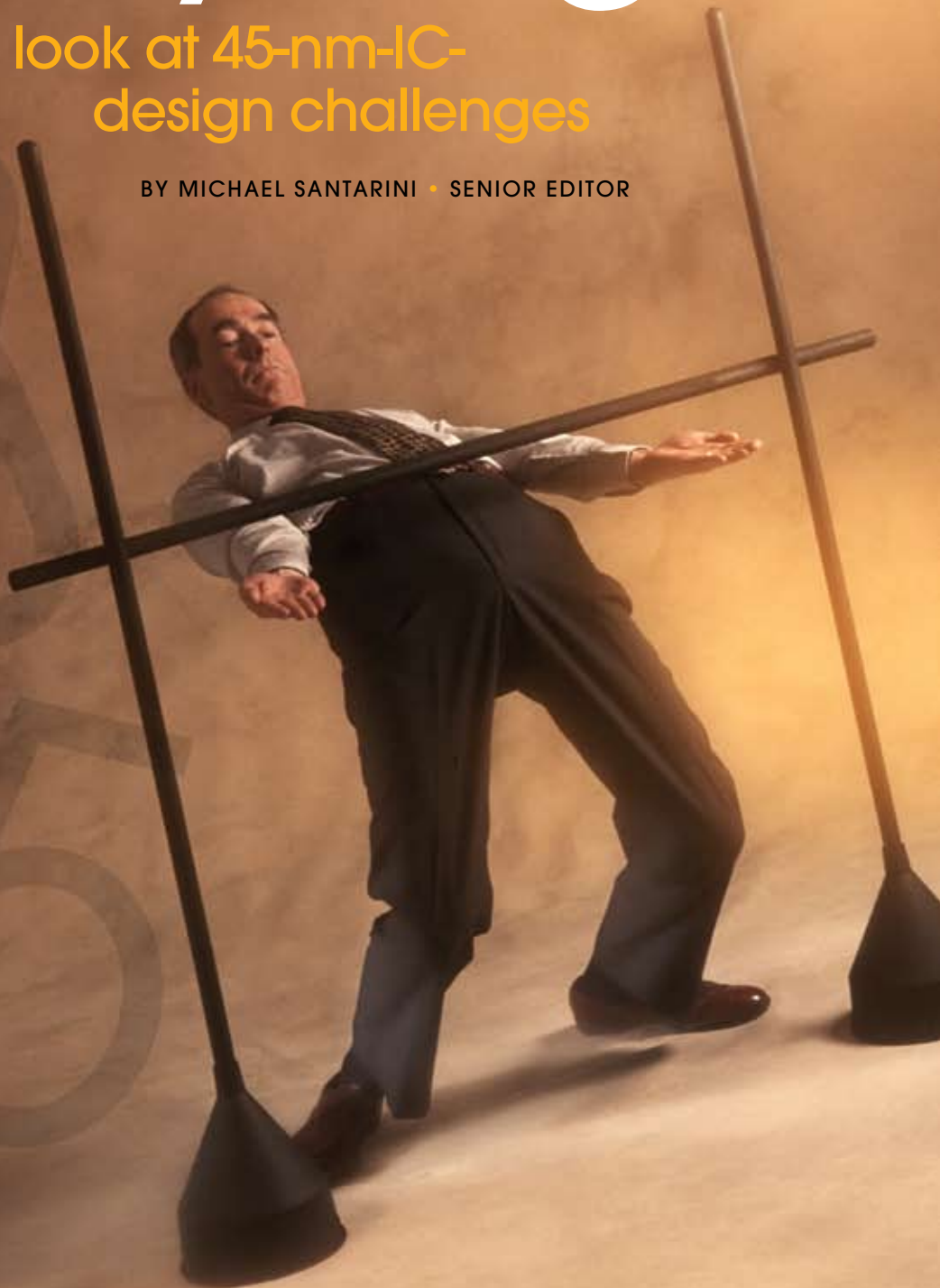


# How low can you go?

A look at 45-nm-IC-  
design challenges

BY MICHAEL SANTARINI • SENIOR EDITOR



**T**he 45-nm node promises SOC (system-on-chip) designers either a 40% increase in transistor counts over 65 nm or a 40% reduction in die size, but mask costs for 45-nm processes will run, at least initially, in the multimillions of dollars. Some designers—especially those with experience designing in either the 65- or the 90-nm nodes and that are familiar with low-power-design techniques—will find the transition to the 45-nm process fairly straightforward. That experience may help to alleviate some of the cost burden of the transition, according to some

foundries, IDMs (integrated-device manufacturers), and EDA vendors. “To design at 45 nm, you will need a better methodology, but it’s not like you will need a brand-new set of tools,” says Tom Quan, deputy director of design-service marketing at TSMC (Taiwan Semiconductor Manufacturing Co). “You’ll just need a better methodology to use those tools.”

With the introduction of 45-nm processing, foundries are now introducing RDRs (restrictive-design rules) for bulk-CMOS processes, mandating the use of advanced low-power-design techniques, and requiring the use of DFM (design-for-manufacturing) tools. Some foundries are also recommending that designers use probability-analysis tools, such as those for SSTA (statistical-static-timing analysis) and static statistical-power analysis to help reduce timing and power problems. Some hold that probability-analysis tools, although promising, may still be immature.

### NO BIG CHANGES

All the big foundries say that manufacturing at the 45-nm node does not differ greatly from manufacturing at 65 nm. The two most significant changes are the 45-nm node’s use of immersion lithography and its use of ultralow-k materials. Immersion, or “wet,” lithography uses liquid between the projection lens and the wafer surface to enhance resolution and numerical apertures. Using the technique essentially ensures that the lithographic features of 45 nm have the same optical clarity as features at 65 nm, which means that the move to wet lithography will have little or no impact on the design flow.

It will raise mask costs, however.

Top foundries TSMC; UMC (United Microelectronics Corp); and the CPTA (Common Platform Technology Alliance) of Chartered Semiconductor, IBM, and Samsung are initially introducing bulk-45-nm processes using ultralow-k-dielectric material, mainly because the processes require no vast retooling or risky process changes. But the lack of an adventurous process change also means that, as transistors shrink, so does the amount of gate oxide in those transistors; thus, leakage is worse at the 45-nm process (**Reference 1**). As a result, the large foundries working at the 45-nm node are delaying the introduction of potentially leakage-stopping materials, such as high-dielectric constant (k), into their manufacturing flows, which means that customers must do their part and, some would argue, more than their part to deal with power management.

TSMC, UMC, and the CPTA will likely have high-k materials ready for their 32-nm processes or perhaps even sooner in second-generation, high-performance, 45-nm processes. Foundries have become wary of any material changes in their processes after experiencing severe setbacks when they introduced 130-nm processes that employed both low-k and copper materials. First, designs at that node had tremendous yield problems and failure rates and essentially drove a retooling in the EDA industry to timing-closure-tool flows, which proved good for EDA vendors but bad for users and chip manufacturers. “As you might expect, foundries are also holding their high-k developments close to the vest because they believe they can use them

IF YOU HAVE TOOLS FOR THE 65-NM OR EVEN THE 90-NM NODE, MOVING TO THE 45-NM NODE REQUIRES NO RETOOLING. BUT DESIGNERS MOVING TO THIS NODE MUST ADOPT SOME ADVANCED DESIGN TECHNIQUES AND BE AWARE OF SOME NEW DESIGN RULES THAT FOUNDRIES HAVE IMPOSED TO ENSURE THAT SOC DESIGNS YIELD ACCEPTABLE RESULTS.

as competitive advantages,” says Walter Ng, senior director for design solutions at Chartered Semiconductor.

In the meantime, however, foundries TSMC, UMC, and the CPTA plan to have 45-nm processes with ultralow-k in pilot or even mass production by year's end and say that they have been working with the major EDA vendors over the past 18 months to ensure that the vendors' tools can handle leakage and other design challenges. Foundries and EDA vendors have high hopes for the 45-nm node. For example, EDA vendor Synopsys had 17 customers doing 65 45-nm designs, and five customers had 10 45-nm tapeouts, according to John Chilton, the company's senior vice president of marketing and strategic development. “It is spookily like 65-nm design two years ago,” he says. “Those numbers were the same, and they tracked quarter after quarter. Right now, there are 425 active 65-nm designs and about 190 tapeouts. So, that tells you that, in the next two years, we'll see about another 180 tapeouts at 45 nm, so things will be pretty

**AT A GLANCE**

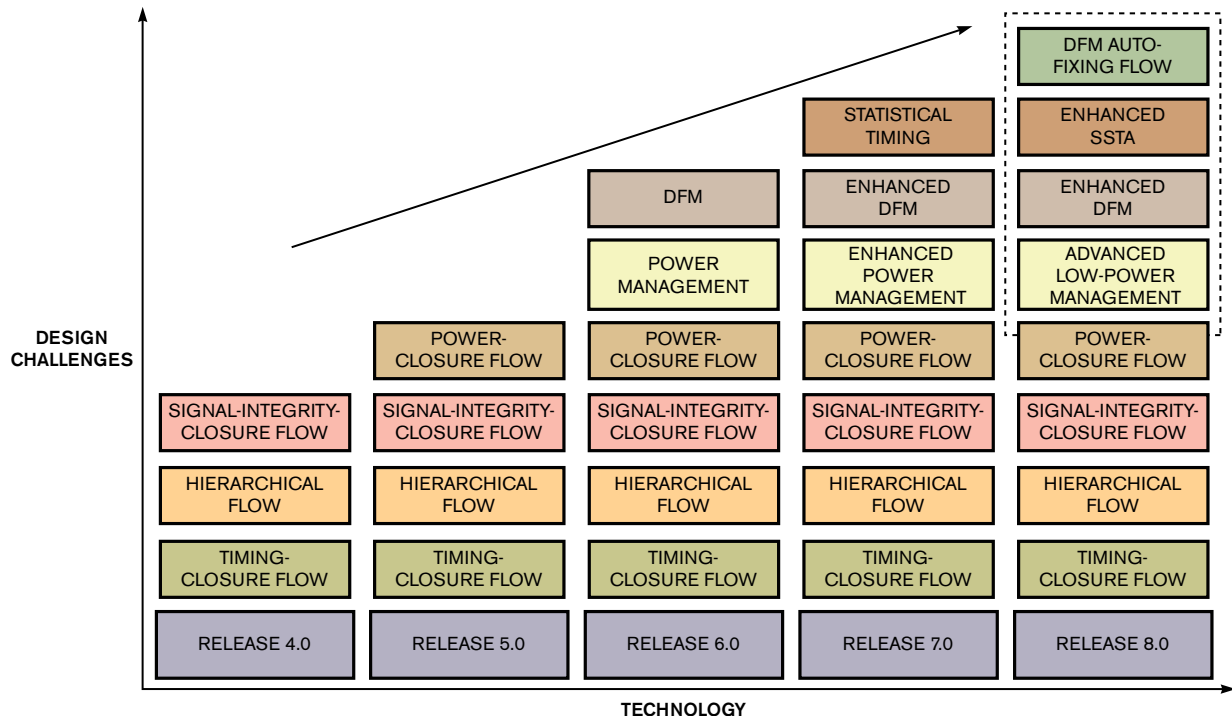
- The 45-nm node offers a 40% reduction in die size or a 40% increase in gate counts over the 65-nm node.
- Active and standby leakage accounts for 60 to 65% of a 45-nm IC's overall power consumption.
- Low-power techniques are necessary at the 45-nm node.
- DFM (design-for-manufacturing) tools are musts at the 45-nm node.
- Foundries are starting to use RDRs (restrictive-design rules) for bulk-CMOS processes at 45 nm.
- Maturing probability-analysis tools will be “nice-to-have” features rather than “must haves” for the 45-nm process.

active.” Some foundries hope that the 45-nm process will become even more active than the 65-nm process and that most chip designers now doing 130-nm design will be tempted to skip the 90- and 65-nm nodes and jump right into

the 45-nm process, noting that these incremental, rather than abrupt, changes in manufacturing mean that the design flow should also change incrementally.

**CHALLENGES AT 45 NM**

Foundries, design teams, and EDA companies say that the 45-nm process presents three major challenges for design teams: mandatory low-power design, mandatory use of DFM tools and methods, and increased deployment of RDRs and probability analysis. As was the case at the 65-nm node, the foundries' first process lines for the 45-nm node are for low power, rather than high performance. Rather than bite the bullet and employ new materials, such as high-k, foundries are not making drastic changes. This decision means that leakage continues to be a first-order concern at the 45-nm node. At the 65-nm node, dynamic and static, or standby, leakage accounts for 40% of an IC's overall power consumption and forces all SOC designers, regardless of their targeted end application, to employ low-power-de-



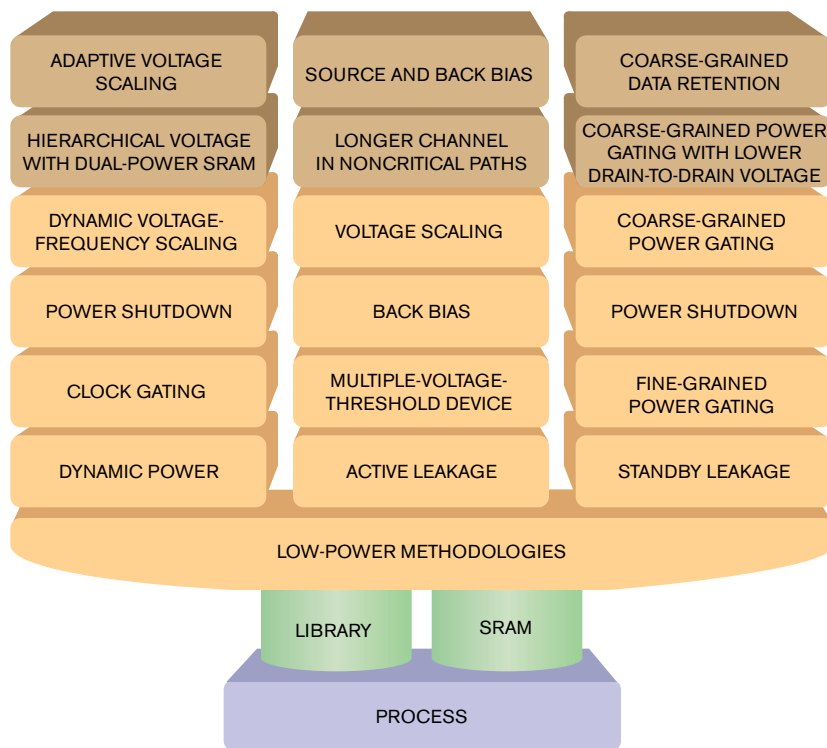
TSMC has issued reference flows for the last five generations of products. Each successive generation has called for more tools illustrating the rising complexity in design requirements.

sign techniques (Reference 2). At the 45-nm node, the problem becomes immense: Leakage consumes 60 to 65% of a device's overall power. This leakage necessitates the use of low-power-design techniques, according to foundries. "We're seeing a lot more use of voltage islands, for example," says Chartered Semiconductor's Ng. "And customers aren't employing voltage islands to simply group devices by power-supply requirements; they are using them to shut down entire sections of devices when they are not in use. Those are drastic techniques for power management, and we're seeing a lot more of that."

Gregg Bartlett, vice president of CMOS technology at Freescale, says that Freescale's networking and wireless groups are designing at the 45-nm node, and both are employing low-power techniques. "I would describe the transition from 65 to 45 nm as nonrevolutionary," says Bartlett. "In power-management-design techniques, we have been doing dynamic-voltage-frequency scaling, gate-retention power gating, and other power-saving techniques for a few nodes. They are not new to us at 45 nm, but we are applying more of them." Bartlett notes that Freescale's wireless group, which has specialized in low-power design for several process nodes, is spending more time doing sophisticated power modeling and is also starting to use thermal modeling for its 45-nm tool flow.

"Locating hot spots and points of intradie thermal variations and knowing where your points of power dissipation are the strongest are areas we see as emerging requirements," says Bartlett. "Although these techniques and tools are not mainstream yet, they give you the comfort of better understanding the product space your products are going to go into." He notes that Freescale has been using IBM's SOI (silicon-on-insulator) processes for its last few generations of chip sets. "We're constantly evaluating processes, but we've had great results with SOI," he says. "We've seen a double-digit improvement in both power and performance in SOI over bulk-CMOS processes."

But foundries offering bulk CMOS have been doing a lot of work to manage power in their new ultralow-k processes, and they've also been working close-



Power management remains a top priority for 45-nm design. TSMC has added more power-management features to an already-long list of power-management techniques.

ly with EDA vendors to give customers more tools to help them manage power with the 45-nm process. For example, in its 8.0 reference flow, TSMC has added "enhanced low-power-technique recommendations" to help customers achieve further power savings. The foundry rec-

**"THESE TECHNIQUES AND TOOLS ... GIVE YOU THE COMFORT OF BETTER UNDERSTANDING THE PRODUCT SPACE YOUR PRODUCTS ARE GOING TO GO INTO."**

ommends the use of advanced voltage scaling and hierarchical voltage with dual-power SRAM blocks to deal with dynamic-power management, the use of source- and back-biasing, and the use of longer channels in noncritical paths to reduce active leakage. It also recom-

mends the use of coarse-grained data retention and power gating with lower drain-to-drain voltage to minimize standby-power leakage.

"Most of these techniques are about gating a clock or simply shutting down blocks when you are not using them," says TSMC's Quan. "There are a multitude of techniques here that our customers can now employ when they start designing in the 45-nm node." There is also a multitude of low-power commercial tools now available to customers. TSMC, UMC, and the CPTA have qualified all of the large vendors' power and low-power point tools from privately held companies. Cadence, Synopsys, and Magma all field low-power tools, and each is diligently working to create an all-in-one low-power flow to capture seats as designers target IC designs to run on leakage-prone 65- and 45-nm processes.

Foundries are eager to accommodate EDA companies in this task. For its 8.0 reference flow, TSMC has validated the Cadence-backed CPF (Common Power Format), which is under the auspices of the Si2 (Silicon Integration

Initiative). The format promises to allow tools from across the design flow to work from a single power format. Quan notes that TSMC is also working with Accellera's UPF (Unified Power Format) group to validate the format for its 45-nm process.

### DFM BECOMES A MUST

At the 65-nm node, foundries were recommending but not requiring their customers' use of DFM tools (Reference 3). However, the 45-nm node will require the use of DFM tools for two of three categories the foundries have defined: LPC (lithography-process checking) and CAA (critical-area analysis). However, foundries will recommend but not require the use of DFM tools for a third category, CMP (chemical-mechanical-planarization) simulation. "We haven't seen many customers using DFM tools at the 65-nm node," says Chartered's Ng. "I'd be surprised if any customer tries to tackle 45 nm without using some amount of DFM." He notes that foundries used the 65-nm process as a proving ground for DFM tools. "We were just starting to become familiar with DFM issues and tool requirements," says Ng. "Now, at the 45-nm node, we have a better idea of what is truly needed."

Most large EDA companies now have the required DFM tools and are trying to integrate them into technologies. Over the last year, most filled out their tool lineups either through internal development or through mergers with and acquisitions of DFM companies. In many cases, the vendors are diligently integrating DFM technologies into tools so that users won't even know they are employing these tools. The major foundries have been helping the EDA companies in this endeavor and have taken note that EDA vendors are now integrating DFM technologies into their flows and making implementation tools correct by construction or at least DFM-compliant. This scenario is similar to the way routers became DRC (design-rules-checking)-compliant during the era of the 90- and 130-nm processes.

Correct-by-construction DFM, or "in-the-loop-design verification," as Magma Design Automation calls it, is somewhat of a necessity, says Dwayne Burek, senior

## MOST LARGE EDA COMPANIES NOW HAVE THE REQUIRED DFM TOOLS AND ARE TRYING TO INTEGRATE THEM INTO TECHNOLOGIES.

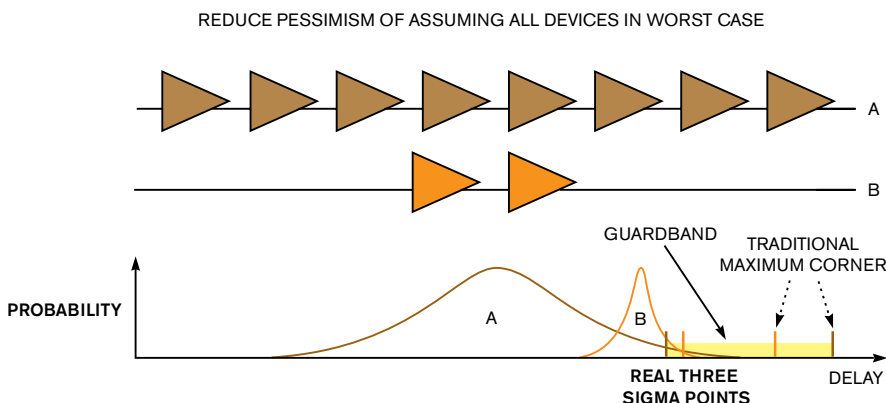
product director of the company's design-implementation-business unit. The 45 nm-node's massive layouts require a great number of DFM decks and models on top of the ever-growing number of DRC/LVS (layout-versus-schematic) physical-verification decks and models. Burek notes that Magma's Talus platform has an in-the-loop-design-verification capability, which includes DRC, LPC, and CMP simulation. "You can run checks within the implementation flow natively or with an integrated physical-verification capability," says Burek.

Both Magma's and Cadence's tool flows have built-in LPC, CMP simulation, and CAA. Cadence recently announced the addition of Aura lithography technology and space-based routing to its Encounter tools and gained LPC and CAA tools from its August acquisition of Clear Shape Technologies. Synopsys' and Mentor Graphics' flows also incorporate LPC and CAA tools, but the two companies use CMP simulators from foundries. TSMC and UMC traditionally work with all EDA ven-

dors interested in validating their tools on the foundries' new processes. TSMC has validated all the large tool vendors' flows and many privately held companies' DFM tools, because this validation makes TSMC's fabrication data available to partner companies in an encrypted format. Quan says that making this data available eases tool vendors' ability to offer the company's customers what TSMC calls DFM-autofixing flows.

UMC also creates a reference flow for every design, but Mort Bamdad, senior director of the corporate marketing division at the company, says UMC doesn't dictate how designs must be done. "As far as 45 nm goes, the baseline flow doesn't change much," he says. "We are talking to EDA vendors to implement DFM changes in their tools so designers will not need new tools but may need some new features."

As with the 65-nm node, the CPTA hand-picked DFM-vendor tools for its 45-nm DFM flow. For CAA, the CPTA has qualified tools from Ponte Solutions and Mentor Graphics. For CMP simulation, the company has qualified Cadence's CMP Predictor, which it obtained when it acquired Praesagus. For detailed, block-level LPC/simulation, the CPTA has qualified Mentor's LFD (lithography-friendly-design) tool, and, for chip-level LPC, the CPTA has qualified Cadence/Clear Shape's InShape tools. Ng notes that the CPTA also recommends Blaze DFM's MO to reduce leakage and improve yield and recom-



SSTA holds promise in improving performance and lowering power. The technology is maturing, but it remains to be seen whether the 45-nm node will broadly adopt it.

mends Mentor's Calibre Yield Analyzer for its checking-deck capability.

### RDRs: NICE TO HAVE?

Over the last few years, industry luminaries have been warning that, with the increase in design size, number of design-rule files, number of DFM issues—especially lithography—and increase in mask costs, foundries would soon need to start enforcing more RDRs to help design teams produce good IC yields. At the 45-nm node, some foundries are seriously considering enforcing these rules. For example, UMC has for two years been developing its 45-nm process. It debuted its first 45-nm test vehicle in the first quarter of 2006 and expects to have introduced its first five early tapeouts by the third quarter of this year and have its 45-nm LL (low-leakage) process ready for pilot production by year-end. UMC's Bamdad says that, in ironing out the process, the company has seen great promise for the use of RDRs to help customers quickly get high-yielding designs to market. "For example, the orientation of poly-

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+ For more on SSTA (statistical-static-timing analysis), see "Characterization tool aids SSTA-library creation" at [www.edn.com/article/CA6407294](http://www.edn.com/article/CA6407294).

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silicon is becoming one of the big issues," says Bamdad. "We're still working on all the details, but it might become mandatory that customers lay polysilicon in the same direction they are laying SRAM and standard cells ... horizontally rather than vertically. Also, if you are going to have an L shape in your design, you'll have to change layers—go horizontally [with the] via and contact and then go vertically. These are rules we expect to enforce."

Chartered's Ng says that, although the company's process-alliance partner IBM has enforced RDRs for its SOI process, the CPTA's customers are now requesting these rules for the CPTA's bulk-CMOS offerings. Many hope that the proper use of RDRs could increase the chance that design teams will be able to create "right-the-first-time" designs and not incur heavy re-spin or ever-more-painful extra mask costs.

Joe Sawicki, vice president and general manager of Mentor's design-to-silicon division, says that, because immersion lithography produces essentially the same quality of results as dry lithography for the 65-nm node, the 45-nm node may not yet require RDRs. "If you were doing without RDRs at 65 nm, you can probably do without them at 45 nm," he says. "The entire impetus behind RDRs is that 2-D features are [difficult to implement]. If you just look at the mathematics, what's going to happen when you go from 45 nm to 32 nm and 22 nm is that features inevitably go from being [difficult to implement] to your having no idea how to make them happen."

When you hit 22 nm, if you believe that you can do [those 2-D features] with a single etch or a single mask process, [you will] have to change the laws of physics.” RDRs are ways to help foundries introduce processes at new nodes without radically changing the manufacturing equipment and flows, he says. He notes, however, that some other advances in lithography and manufacturing may make RDRs less necessary at the 32- and 22-nm nodes.

Synopsys’ Chilton says that his company has yet to hear of any customers using RDRs. “So far, people seem to be sticking to classic design rules, though it’s moving to model-based rather than rules-based approaches,” he says. RDRs are somewhat controversial and have spurred a debate in the industry about whether they will help alleviate some of the complexity in design flows or will overtax commercial routers that must deal with massive DFM rules and models on top of ever-increasing DRC decks for ever-larger-gate-count designs.

Foundry reps indicate that, in qualifying implementation flows even without

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RDRs, some commercial routers—but they decline to say which ones—that worked for the 65-nm node struggle with the large designs and more complex rules and models at 45 nm. For-

tunately, EDA vendors are addressing these problems. Mentor and Cadence both claim to have new router technology that they created to handle the complexities of 45 nm. Mentor Graphics acquired Sierra Design Automation in June and is currently working with foundries to qualify its router for 45-nm flows and further integrate its Calibre lineup into the flow, and Cadence this month added technology from its custom digital-space-based-router technology to its standard-cell Encounter routing platform. “The 65- and especially the 45-nm nodes are separating the great routers from the OK routers,” says Eric Filseth, vice president of digital-IC implementation at Cadence.

## PROBABILITY ANALYSIS

Although the academic and EDA communities have predicted that probability-analysis tools—notably SSTA (statistical-static-timing-analysis) tools—would replace traditional static-analysis tools at advanced nodes, that scenario hasn’t occurred at the 65-nm node, according to foundries. But EDA vendors,

early adopters of 45-nm technology, and foundry reps from TSMC and UMC say that 45 nm may mark the first node to broadly adopt probability analysis. SSTA tools promise to replace worst-case-timing models (traditional wire-load models) with more realistic and accurate analysis of circuit behavior using statistical techniques. Using statistical models to characterize standard-cell-process libraries, designers run analysis of the behavior of circuits, blocks, or entire designs and derive timing parameters of circuit performance. They then use those results to fine-tune the performance of their designs and even reduce power or toggle off unneeded transistors or blocks.

With the increasing size and complexity of 45-nm designs, SSTA tools have proved useful for some designers, including those at Texas Instruments, according to Mike Fazeli, the company's worldwide-EDA-strategy manager, and Clive Bittlestone, TI's ASIC-backplane manager. Despite the tools' usefulness, however, foundries have been slow to approve them for timing sign-off, slowing their adoption. Other designers have found commercial SSTA difficult to use. "Variation is tricky because it calls into question things in sign-off and where you should set the variation points," says Synopsys' Chilton. "It is hard to figure out. So, it's a big move from traditional rules-based sign-off to something softer; there's a culture to figure out—not a technical problem."

Chartered Semiconductor's Ng is skeptical about whether SSTA tools will be in wide use at the 45-nm node. "It's an area that everyone agrees has a lot of promise; the problem is in implementation," he says. However, EDA companies and some foundries, including TSMC and UMC, say that the predictability-analysis tools are maturing. EDA companies, such as Extreme DA, Magma, and Synopsys, have been fielding SSTA tools for more than a year, and Cadence also jumped into the game this month with its Encounter Timing System GXL SSTA tool. TSMC's Quan says that SSTA standard-cell-library-characterization tools, such as Altos Design Automation's Variety, have helped solidify the flow because the tools can help foundries and users characterize li-

braries for better use of statistical-analysis tools. TSMC has added Altos Design to its 8.0 reference flow and is now offering customers statistical models of its 45-nm process. Designers can extend TSMC's statistical models and methods to leakage issues, and TSMC has added statistical leakage analysis to its 8.0 reference flow, although EDA vendors, such as Magma, are just starting to offer these types of tools.

## MORE CHALLENGES

Overall, foundries expect the transition to the 45-nm node to be fairly easy for designers familiar with the challenges of 65-nm and even 90-nm design. The node will require designers to implement low-power-design techniques and to use DFM tools and may require the use of RDRs and probability-analysis tools, too. Foundries hope that the 45-nm node will prove so unthreatening to mainstream-IC designers that a large chunk of them working at the 130-nm node will consider skipping right over 90 and 65 nm and go straight into 45 nm. But, before you face the 45-nm test, you should also consider the ongoing challenges inherent in every new design process: The 45-nm node will present significant challenges in developing chip architectures, software development, logic design, and logic verification. **EDN**

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