

## LISTING 1 FPGA OUTPUT

```
module pwm(Clk, Reset, Enable, Value, Out);  
parameter CountBits = 8;  
  
input Clk, Reset;  
input Enable;  
output Out;  
input [CountBits-1:0] Value;  
  
reg [CountBits-1:0] Count;  
  
assign Out = Count < Value;  
  
always @(posedge Clk or posedge Reset)  
    if (Reset)  
        Count <= 0;  
    else  
        if (Enable)  
            Count <= Count + 1;  
  
endmodule
```