

Single op amp achieves double-hysteresis-transfer characteristic

Herminio Martínez, Encarna García, and Juan Gámiz,
Technical University of Catalonia, Barcelona, Spain

In process-control applications requiring discontinuous controllers, the most elementary choice is a two-position-mode or on/off controller. A typical example of such a con-

troller is a space heater. If the temperature drops below a setpoint, the heater turns on, and, if the temperature rises above the setpoint, it turns off. In the analog domain, the basis for the ba-

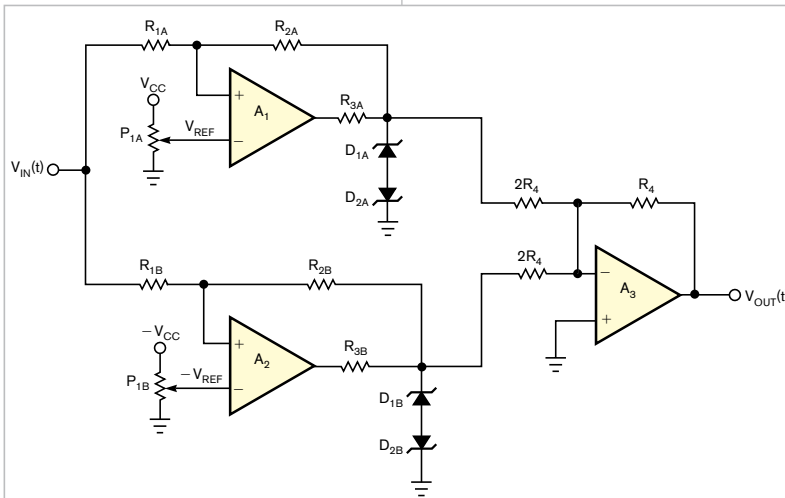


Figure 1 One straightforward way of obtaining a double-hysteresis-transfer characteristic uses three op amps with voltage references and zener diodes.

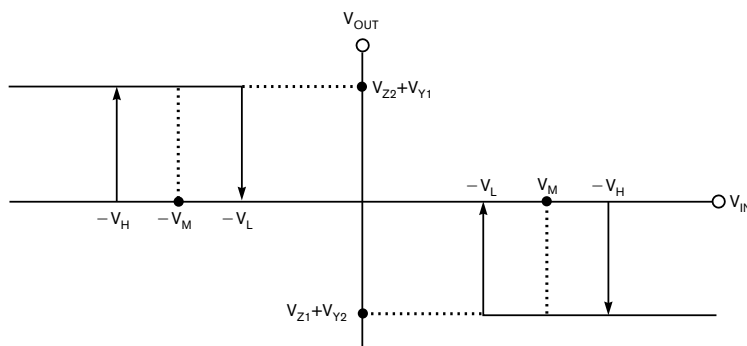


Figure 2 The I/O-transfer characteristic of the circuit in Figure 1 exhibits two hysteresis bands.

DI Inside

70 Integrator ramps up/down, holds output level

72 Switcher adds programmable-PWM-duty-cycle clamp

74 Circuit provides low-cost QAM mapping and translation

► What are your design problems and solutions? Publish them here and receive \$150! Send your Design Ideas to edndesignideas@reedbusiness.com.

sis implementation of a two-position controller is an analog comparator or an open-loop operational amplifier. However, to avoid false switching, the typical implementation uses the well-known Schmitt trigger.

A logical extension of the two-position control mode is to provide several—rather than two—intermediate settings of the controller's output. You can use this discontinuous-control mode to reduce the cycling behavior, overshoot, or undershoot inherent in the two-position mode. The most common example is the three-position controller. Figure 1 shows one simple way to implement this controller. In this configuration, the Schmitt triggers around the operational amplifiers, A_1 and A_2 , which implement the negative and positive hysteresis, respectively. You can replace A_1 and A_2 with analog comparators, such as an LM311 or similar. Figure 2 shows the I/O-transfer characteristic of the circuit in Figure 1:

$$V_M = V_{REF} \frac{R_1 + R_2}{R_2}$$

$$V_H = V_M + (V_Z + V_Y) \frac{R_1}{R_2},$$

and

$$V_L = V_M - (V_Z + V_Y) \frac{R_1}{R_2}.$$

V_Z and V_Y are, respectively, the breakdown and the forward voltages of the four zener diodes.

Figure 3 shows a more efficient way to implement a three-position controller. The circuit's basis is a single operational amplifier, and it needs no reference voltages. The input and output diodes determine the upper high-voltage and lower low-voltage switching-threshold levels and the hysteresis of the comparator. Putting $V_{IN}(t)$ in the middle band eliminates the input diodes from the circuit, and the circuit is essentially a voltage follower with positive feedback. The output voltage follows $V_A(t)$, but the positive feedback establishing $V_A(t)$ sets this voltage at some fraction of the output voltage. So, two constraints define the output level in this circuit state: $V_{OUT}(t) = V_A(t)$, and

$$V_A(t) = V_{OUT}(t) \frac{R_1}{R_1 + R_2}.$$

The only condition satisfying these two constraints is that V_{OUT} and $V_A = 0V$; so, the output remains at $0V$ when the input diodes are reverse-biased. A $0V$ output state continues until input voltage increases with positive or negative values. Then, one of the two input zener diodes conducts, driving the amplifier output positive or negative at an input voltage of $\pm V_H$. In this condition, when absolute input voltage decreases, the amplifier output again goes to $0V$ at an input voltage of $\pm V_L$. Thus, the design equations for V_H and V_L are $V_H = V_{Z1} + V_{Y1}$, and

Figure 4 shows the I/O-transfer characteristic of the circuit with the values in **Figure 3**, where D_{1A} and D_{1B}

$$V_L = (V_{Z1} + V_{Y1}) - (V_{Z2} + V_{Y2}) \frac{R_1}{R_1 + R_2}.$$

are 6.8V 1N4099 zener diodes and D_{2A} and D_{2B} are 3V 1N5225 zener diodes.

Figure 5 shows the output voltage when you apply a triangular waveform at the circuit's input. **EDN**

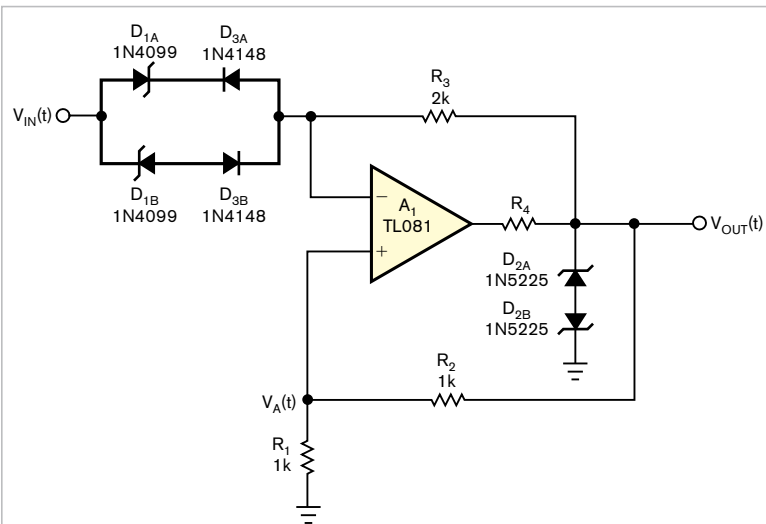


Figure 3 This circuit achieves dual hysteresis using only one op amp.

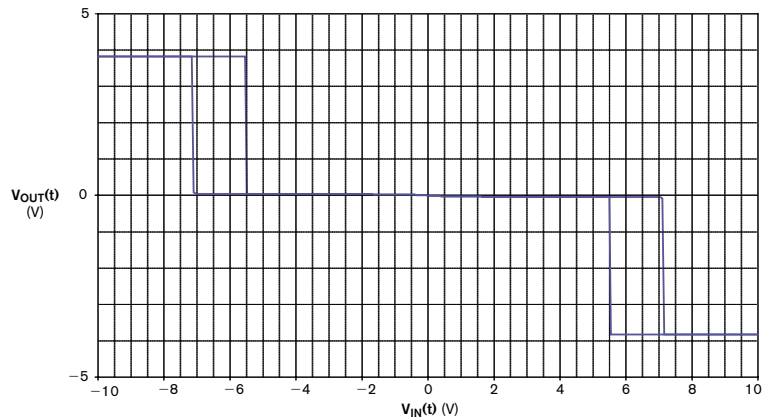


Figure 4 This oscilloscope trace shows the transfer characteristic of the circuit in **Figure 3**.

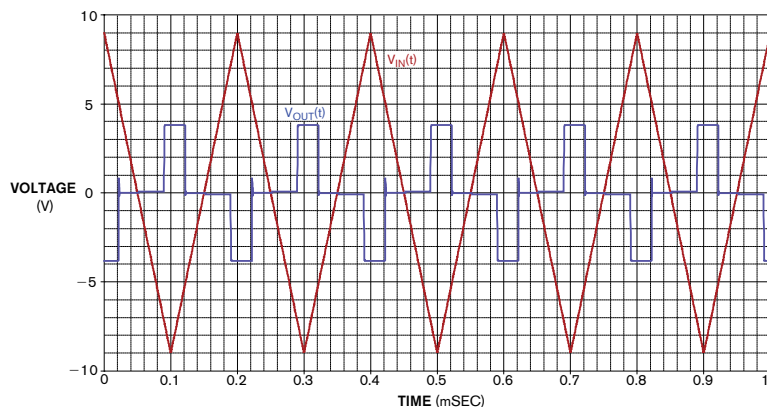


Figure 5 This oscilloscope trace shows the response of the circuit in **Figure 3** to a triangular input waveform.

Integrator ramps up/down, holds output level

Glen Chenier, TeeterTotterTreeStuff, Allen, TX

Op-amp integrators can ramp to saturation, and a capacitor-discharge switch can reset them. Alternatively, you can input-switch them to ramp up and down in triangle-wave-form-generator applications. Much searching through online “cookbook” circuits turned up no means of ramping an op-amp integrator to hold at a preset constant voltage level. This Design Idea describes a single-supply op-amp circuit that outputs a rising or falling linear-voltage ramp in response to a step change of a positive dc-input voltage of 0V to V_{CC} . The output ramp’s dV/dt slope is adjustable to 1V/minute with the values in **Figure 1**, is independent of the input-step amplitude, and terminates at a constant dc level approximately equal to the input-step voltage. Any further change in the dc-input voltage causes the output to ramp up or down at the preset dV/dt to the new dc-input voltage. In effect, this circuit is an amplitude-bounded constant-slope integrator.

The circuit uses a rail-to-rail I/O quad

op amp, the National Semiconductor (www.national.com) LMC6484. The rail-to-rail feature makes it easy to use, the low input leakage is great for long-time-constant integration, and the 3-mV maximum input-offset voltage is respectable. Potentiometer R_1 , a linear taper, sets the input voltage for final output voltage after the ramp ends. IC_{1A} ’s output is in saturation at V_{CC} or ground while the output is ramping down or up, respectively.

Nonpolarized capacitor C_1 and potentiometer R_2 , a linear taper, determine the time constant of integrator IC_{1B} . The adjustment range is 0.5V/msec to 1V/minute. The reference bias for IC_{1B} is 108 mV, which you derive from IC_{1D} as a unity-gain buffer for divider R_7 and R_8 . R_6 ensures that you do not exceed IC_{1B} ’s input current when you turn off the power, that C_1 discharges through IC_{1B} ’s input and output diodes, and that IC_{1B} ’s output does not excessively load back into IC_{1D} ’s output with R_2 at a minimum.

R_3 and R_4 divide the saturated IC_{1A} ’s

output to approximately 100 mV unloaded above or below the 108-mV bias. This division causes approximately 20 mV to drop across R_3 to slew IC_{1B} upward or downward at the integration rate that C_1 and R_2 set; 20 mV is comfortably above the op amp’s possible 3-mV input-offset voltage to minimize offset effects. When IC_{1B} ’s output-voltage ramp reaches that of the input voltage from the R_1 wiper, IC_{1A} comes out of saturation and rests at approximately 2.5V, providing the loop-negative feedback to maintain integrator IC_{1B} ’s output equal to the input voltage. This action sets the boundary on the integration ramp’s terminal voltage. IC_{1C} can be spare, or, as the **figure** shows, you can drive it with a triangle-wave signal to convert IC_{1B} ’s dc level or ramp to a corresponding PWM (pulse-width-modulated) signal for a motor-drive circuit (not shown).

R_5 eliminates differential errors arising from bias-resistor tolerance, and it provides a compromise between IC_{1B} ’s 3V maximum input-offset voltage at 25°C and 20-mV input amplitude to allow the slowest dV/dt. The values in the **figure** result in a maximum time of approximately 1V/minute, or 5 minutes at V_{CC} of 5V to reach full speed. If you require longer times,

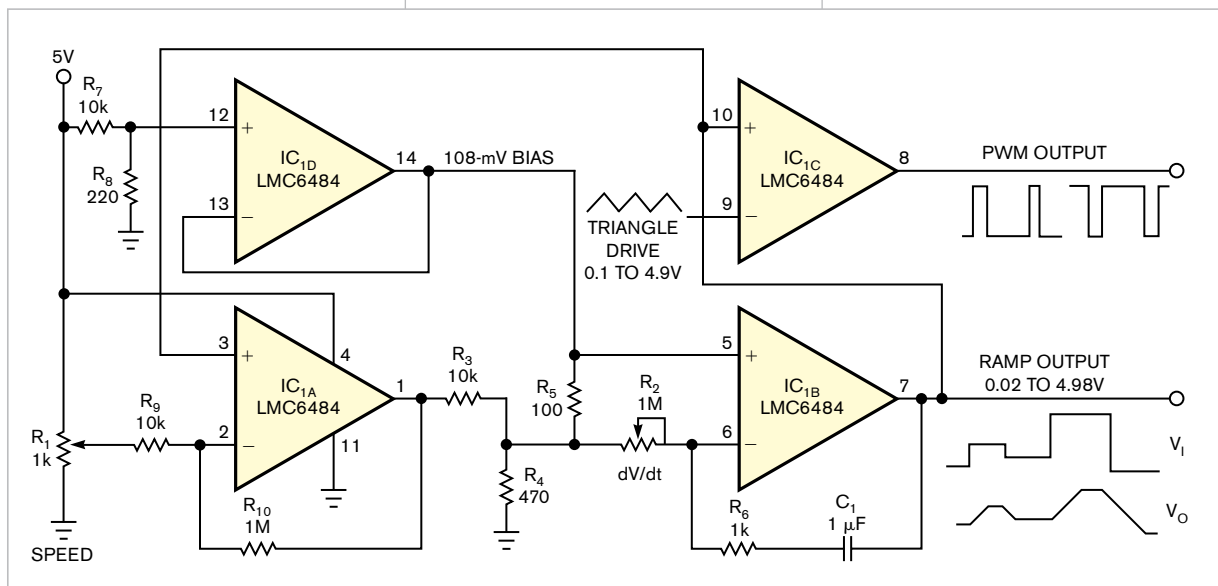


Figure 1 This op-amp integrator ramps up or down at a preset rate, holding a final value equal to the input-voltage dc level.

you can raise V_{CC} to 15V with adjustments to the bias resistors or raise C_1 's value by using parallel nonpolarized capacitors. Alternatively, you could raise R_2 's value, although selection is sparser for potentiometers with values greater than 1 M Ω .

If your application does not require a long time constant or if you use the aforementioned methods to increase

the time constant, you can eliminate R_5 at the expense of a higher level differential input to IC_{1B} and correspondingly faster integration. You could also eliminate IC_{1D} and the R_7 - R_8 resistive-bias divider that connects directly to IC_{1B} 's Pin 5, but resistor tolerance becomes more critical to minimize differential error (**references 1 and 2**). **EDN**

REFERENCES

- 1 "Tractive effort, acceleration, and braking," The Mathematical Association, 2004, www.brightlemon.com/ma/what_use/TractiveEffortAccelerationAndBraking.doc.
- 2 Woof, Tony, "Kilo newtons, kilo watts, kilometres per hour," 2001, www.twoof.freeseerve.co.uk/motion1.htm.

Switcher adds programmable-PWM-duty-cycle clamp

Michael O'Loughlin, Texas Instruments, Nashua, NH

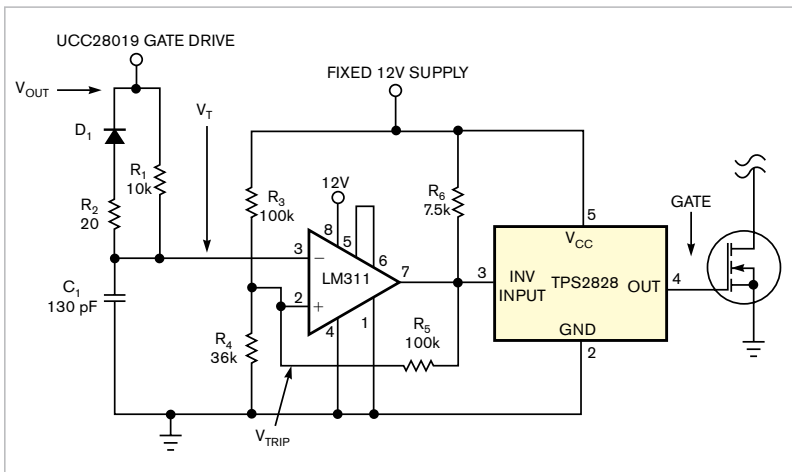


Figure 1 This simple circuit clamps the duty cycle of a switching regulator to 90%.

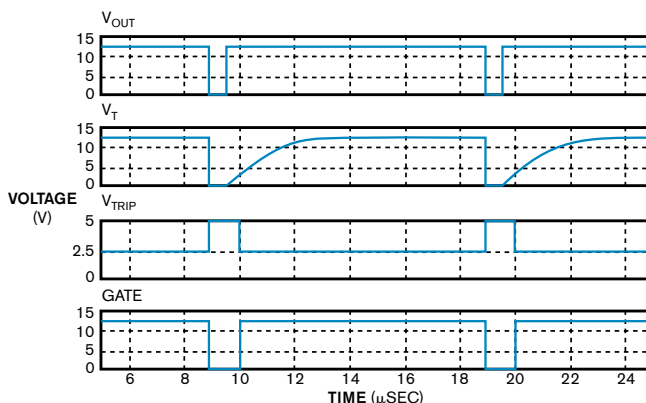


Figure 2 A SPICE simulation of the circuit in Figure 1 shows the clamping action cutting in at 90% duty cycle.

Power-supply applications require the use of a duty-cycle clamp. Such applications include those using current-sense transformers and two-switch forward converters. If a duty-cycle clamp is not present, the transformers could saturate, causing a catastrophic failure in the system. However, to drive down the cost of the design, many power-supply designers use inexpensive, eight-pin PWM controllers that have no duty-cycle clamp. This Design Idea shows how to add an inexpensive duty-cycle clamp to these PWM controllers.

You can add the circuitry to most PWM controllers to provide a programmable duty-cycle clamp (**Figure 1**). The circuitry comprises a few passive components, a hysteretic comparator, and a gate-driver IC. Resistor R_1 and capacitor C_1 program the duty-cycle clamp's dead time. Resistor R_2 and diode D_1 reset the timing circuitry when the output of the PWM controller goes low. Resistors R_3 , R_4 , and R_5 set the comparator's trip point, V_{TRIP} , at 5V. Resistor R_5 adds $-2.5V$ of hysteresis to the comparator to ensure circuit stability.

The following example shows how to set the circuitry in **Figure 1** for a maximum duty cycle, D_{MAX} , of 0.9. The PWM controller operates at a switching frequency, f_s , of 100 kHz. Most PWM controllers cannot reach 100% duty cycle and have a specified dead time. For this example, the dead time is 300 nsec. To set the timing capacitor also requires knowing the maximum output of the PWM output voltage, V_{OUT} . In this example, the maximum output voltage is 12V. The timing ca-

capacitor is roughly 130 pF. The design uses a standard, 120-pF capacitor. The following equations describe the calculations: $t = (1 - D_{MAX}) / f_s$ - dead time = 700 nsec, and


$$C_1 = \frac{-t}{\ln\left(1 - \frac{V_{TRIP}}{V_{OUT}}\right) R_1} \approx 130 \text{ pF.}$$

A SPICE simulation with the circuitry in **Figure 1** ran to ensure that the duty-cycle clamp works with the circuitry. **Figure 2** shows the results of this simulation. V_{OUT} is the output of the PWM controller, V_T is the voltage at the inverting pin of the comparator, V_{TRIP} is the voltage at the noninvert-

ing input of the comparator, and gate is the output of the gate-driver IC. From the waveforms in **Figure 2**, you can see that the duty-cycle clamp appears to be working correctly, clamping the output of the gate driver to 90%. **EDN**

Circuit provides low-cost QAM mapping and translation

Pieter Demuytere, Cedric Mélange, Elena Matei, Els De Backer, Johan Bauwelinck, and Jan Vandewege, Ghent University, Department of Information Technology, Ghent, Belgium

 This Design Idea presents an efficient way to do QAM (quadrature-amplitude-modulation) mapping and translation into two's-complement values with only two inverters and no look-up tables.

Suppose you want to create a 256-level QAM signal using a microcontroller and two 10-bit DACs with a parallel input in two's-complement notation. Because you can split a 256-level QAM signal into a 16-level ASK (amplitude-shift-keying) signal for the in-phase component and a 16-level ASK for the quadrature component, a symmetrical approach is feasible. The fully symmetrical circuit performs the 16-level ASK mappings and translations (**Figure 1**). Two inverters are the only glue logic you need for the conversion. Each part of the circuit converts four output bits of the microcontroller into a 10-bit two's-complement vector, which feeds directly to the DACs (**Table 1**). The possible DAC-input values are equally distributed. The third column of **Table 1** gives the normalized DAC output after an optional current-to-voltage conversion.

For 256-level QAM signals, you need 8 input bits, which exactly fit the width of a general-purpose-I/O bank on most microcontrollers. Simultaneously setting all 8 bits ensures synchronization between in-phase

and quadrature signals. You can easily adapt this circuit for any QAM constellation or DAC resolution. Because this circuit is fully digital, you can also embed it in FPGAs or CPLDs, using the inverters available in the output buffers. **EDN**

TABLE 1 INPUT AND OUTPUT

Microcontroller output	DAC input	DAC output (V)
0000	1000 0000 10	-0.998
0001	1001 0001 10	-0.863
0010	1010 0010 10	-0.730
...
0111	1111 0111 10	-0.066
1000	0000 1000 10	0.066
...
1101	0101 1101 10	0.730
1110	0110 1110 10	0.863
1111	0111 1111 10	0.998

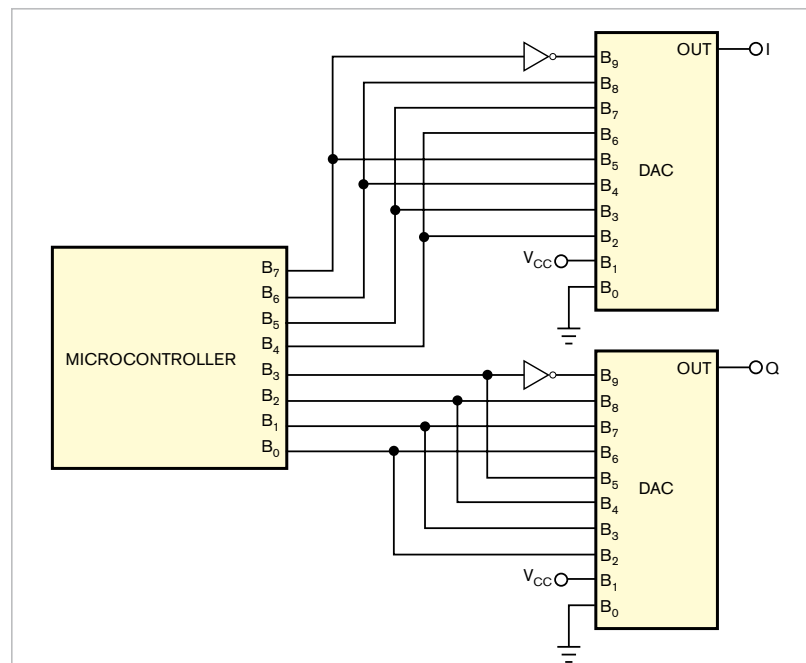


Figure 1 This circuit converts 2×4-bit outputs from the microcontroller into 2×12-bit, 16-level ASK values.