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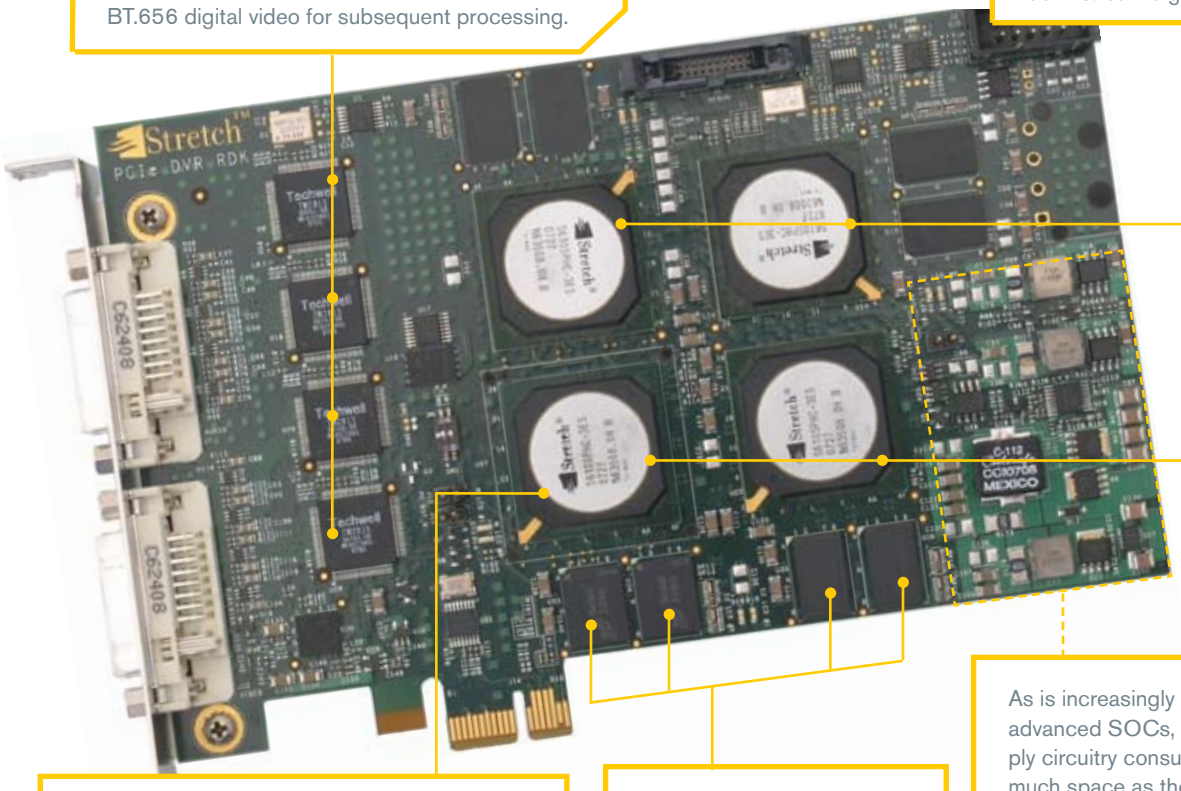
Video surveillance: It's all about computing power

Placing an area under video surveillance means setting up lots of cameras. But that's the easy part. The system must concentrate the signals from those cameras for transmission back to a central hub, using as low a bit rate as possible, especially if the link uses Internet Protocol. Often, because most of the signals will go into storage unexamined by humans, software must refine the images, select potentially important ones, and even recognize objects or persons in the incoming video stream. All of these circumstances turn the surveillance-camera-electronics job from a simple task for a JPEG encoder into a serious image-processing load worthy of an array of programmable SOCs (systems on chips). A design that can handle this transformation is just what Stretch Inc has brought to the problem with its PCI Express DVR RDK reference-design board.

The board uses four Techwell TW2815s to gather 16 video and 16 audio channels. These four-channel devices acquire NTSC/PAL composite video and analog audio, filter it, and convert it to BT.656 digital video for subsequent processing.

Four Stretch S6100s compress the incoming video using a software-based multistandard compression engine. Each device works on four channels, with one doubling as a supervisor. The chips working together are capable of H.264 D1 resolution encoding at 30 frames/sec on each channel. Significantly, there is processing room left over for video analytics that can scan images for content, adjust cameras or compression rates, or provide raw data for downstream algorithms.



Stretch designed the board to use PCI Express as its means of communication with a host processor, which would save the compressed video locally or transmit it to a remote hub. The S6100 chip directly supports the interface.

Each Stretch chip uses a pair of Micron D9GMG DDR2 DRAMs for local storage in addition to the SRAM on the S6100 dice.

As is increasingly the case with advanced SOCs, the power-supply circuitry consumes nearly as much space as the computing heart of the board. The design must support the needs of the computing chips, DDR2 DRAMs, and analog front-end devices.