

Circuits protect outputs against overvoltage

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In test-and-measurement applications, you must provide overvoltage protection for the output terminals of amplifiers, power supplies, and similar components. The conventional way to accomplish this

task is to add series resistors with the output node along with the clamping diodes to power-supply rails or other threshold voltages (Reference 1 and Figure 1). This resistor significantly reduces current-output capability and

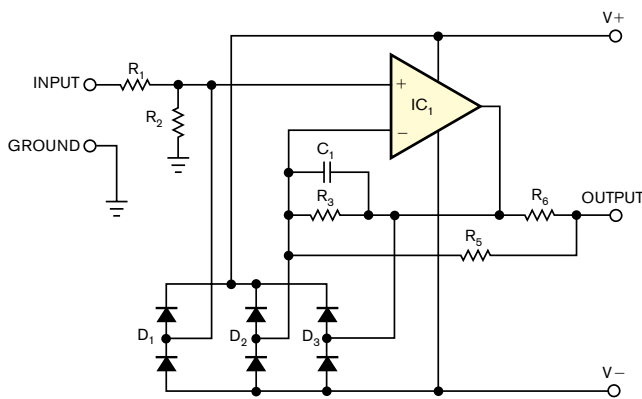


Figure 1 The conventional way to provide overvoltage protection is to add series resistors with the output node along with the clamping diodes to power-supply rails or other threshold voltages.

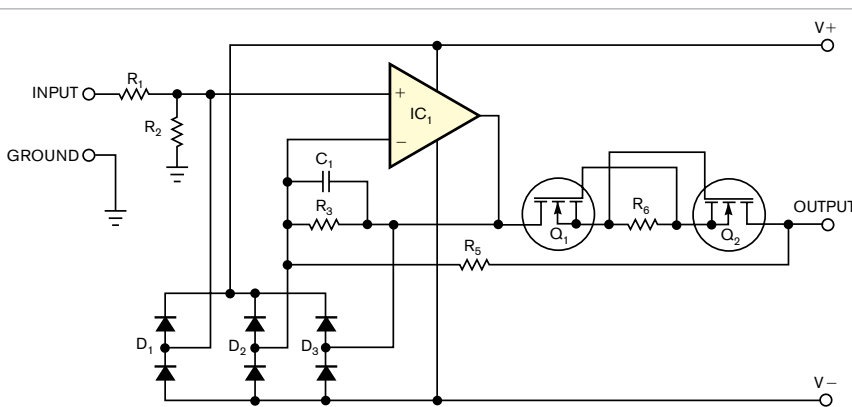


Figure 2 This circuit works as a bipolar-current source when the voltage drop across source resistor R_6 becomes larger than the gate-threshold voltage of depletion-mode MOSFETs Q_1 and Q_2 , thus limiting the current through clamping diodes.

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the output-voltage swing with low-resistance loads. The alternative approach is to use fuses or other current-limiting devices, which precede these clamps' high energy-absorption capability. The circuit in **Figure 2** works as a bipolar current source when the voltage drop across source resistor R_6 becomes larger than the gate-threshold voltage of depletion-mode MOSFETs Q_1 and Q_2 , thus limiting the current through the clamping diodes (**Reference 2**). The drawback of this approach is high power dissipation on series components during the overload condition.

A reasonable approach disconnects the amplifier-output node from the output terminals for the period when the overload voltage exists on output terminals. Engineers for decades have used such serial disconnection by means of electromechanical relays in audio power amplifiers but for a different reason: loudspeaker protection. SSRs (solid-state relays), including optoelectronic, photovoltaic, OptoMOS, and PhotoMOS devices, suit the task

of load disconnection at moderate current levels because of galvanic isolation between the control and the load pins (**Reference 3**).

The series-protection circuit of **Figure 3** disconnects the amplifier-output terminal using a series-connected, high-voltage SSR. Raising the output voltage above the positive-reference-voltage or below the negative-reference-voltage threshold causes either the IC₂ or the IC₃ comparator to change its output state and turn off SSR IC₄ through AND logic element IC₅. **Figure 4** shows the simple circuit realization of this approach.

The circuit in **Figure 4** requires only a couple of external components to use an SSR for output-overvoltage protection. Rising overvoltage turns off both transistors in IC₂, interrupting current flow through the control LED of IC₃. Relay IC₃ opens, protecting the amplifier and clamping diodes. The circuit was tested with a handful of Clare, Matsushita Electronic Works, and Panasonic (www.clare.com, www.naisis.co.jp/english, www.panasonic.com) SSRs with and without internal current protection. The power-supply rails are ±15V; R₁₀, R₁₁, and R₁₂ set the triggering levels and are equal to ±16V. Omitting R₁₁ shifts the triggering levels to ±14.5V. The SSR turn-off delay in protection-circuit operation is 100 to 200 μsec for relays with 0.5V overvoltage protection and becomes slightly shorter with higher overvoltage. Note that the peak current through clamping diodes can be rather high with low-on-resistance SSRs. **EDN**

REFERENCES

- 1 Steele, Jerry, "Protect Those Expensive Power Op Amps," *Electronic Design*, Jan 31, 1991.
- 2 "±500 Volt Protection Circuit," Application Note AN-D11, Supertex Inc, Aug 14, 2000, www.supertex.com/pdf/app_notes/AN-D11.pdf.
- 3 Stitt, R Mark, and David Kunst,

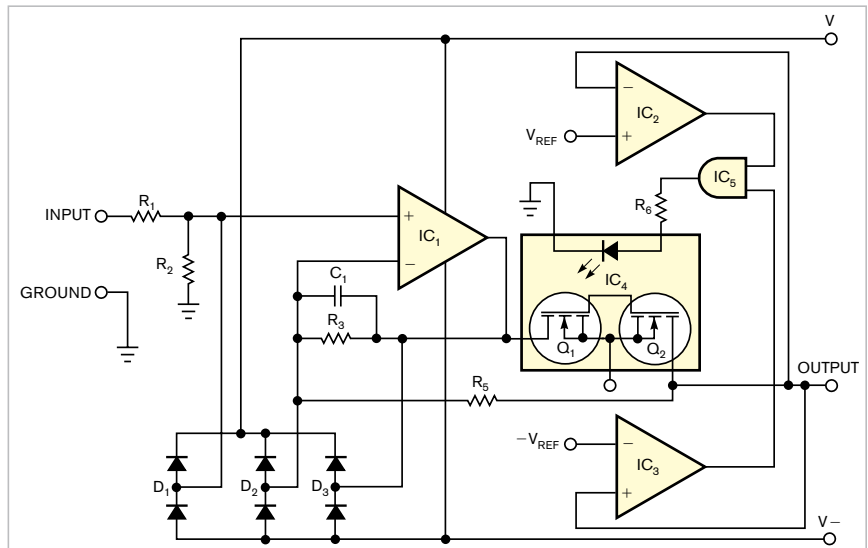


Figure 3 This series-protection circuit disconnects the amplifier-output terminal using a series-connected, high-voltage SSR.

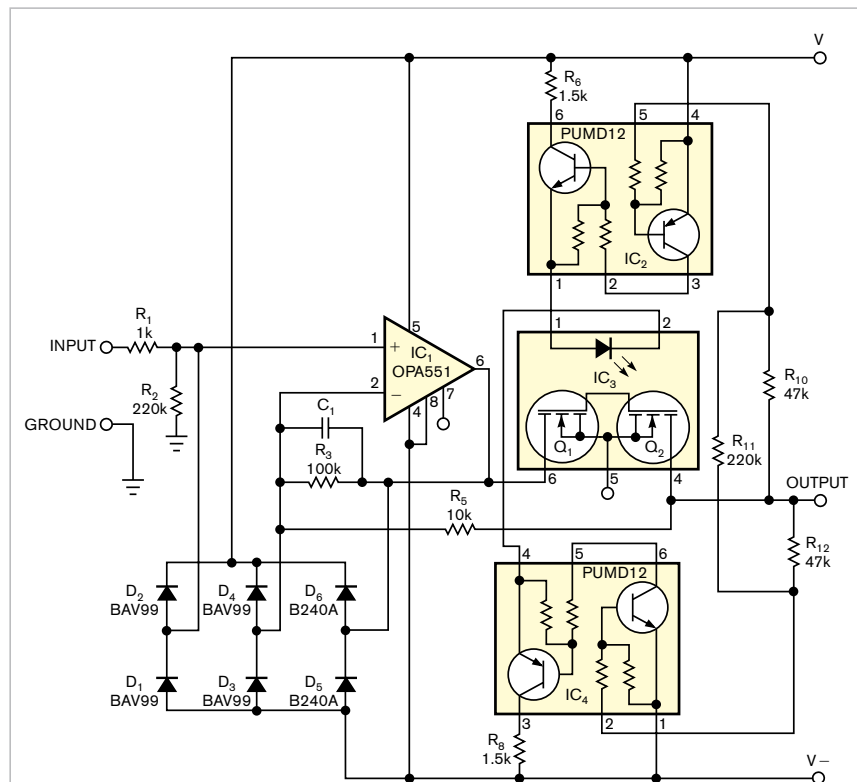


Figure 4 This circuit requires only a couple of external components to use an SSR for output-overvoltage protection.

"Input Overload Protection for the RCV420 4-20MA Current-Loop Receiver," Burr-Brown, Application Bulletin AB-013, July 1990, <http://focus.ti.com/lit/an/sbva003/sbva003.pdf>.

4 "Fault-Tolerant Analog Switches," Application Note 745, Maxim Integrated Products Inc, March 25, 2001, www.maxim-ic.com/appnotes.cfm/an_pk/745.

CPLD connects two instruments with half-duty-cycle generator

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When synchronizing two instruments' signals, it is important to make sure that the receiver can latch the sender's synchronous signal. For example, a pulse generator generates synchronizing pulses while generating the main pulse signal. For the Avtek (www.avtekkorp.com) AV-1015B, the pulse generator's duty cycle is approximately 50 nsec at TTL with a 50Ω load. The goal of this Design Idea is to increase the pulse generator's high-level width to meet the triggering spec of a lock-in amplifier. The synchronizing pulse's frequency is 10 Hz to 102 kHz, which is the lock-in amplifier's frequency range.

Because the synchronizing pulse synchronizes to the main pulse, you must minimize any delay in calculating the lock-in amplifier's synchronizing input. And, because the user can change the frequency of the pulse train from the

pulse generator, the synchronizing signal's frequency also changes. Therefore, you must make sure that the circuit properly calculates and generates the synchronizing signal, no matter how the user sets the output of the pulse generator.

Figure 1 shows the half-duty-cycle generator's algorithm. The CPLD first waits for the positive-edge trigger, then starts to count at a frequency of 60 MHz, and waits for the next positive-edge trigger. When the next positive edge comes, the synchronizing signal's period counting is complete. The counting value then gets saved in a buffer and divided by 2 to yield the value for half-duty-cycle generation.

In tests, the half-duty-cycle generator in this Design Idea worked over a frequency range of 2 Hz to 450 kHz. You can use this design not only in a pulse generator, but also in any synchronizing signal in which the pulse is too narrow for other system triggering. The half-duty-cycle generator fits into a CPLD, such as an Altera (www.altera.com) EPM570 with a 60-MHz system clock and an MM74-HCT244 buffer to output a TTL signal.

Listing 1 contains the program for the CPLD. [EDN](#)

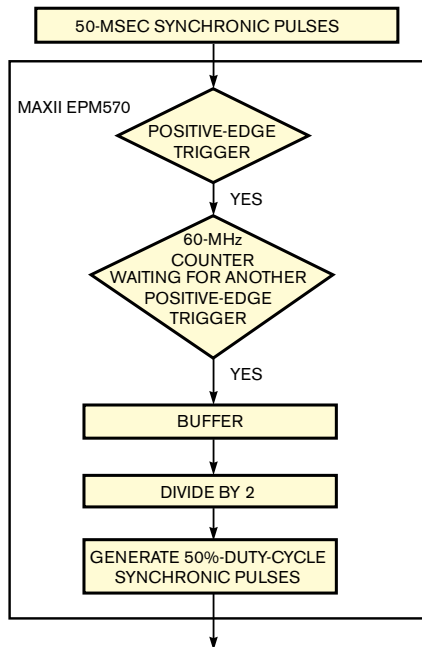


Figure 1 When programmed into a CPLD, this algorithm expeditiously generates a synchronizing signal at half the input frequency.

LISTING 1 GENERATING 50% DUTY CYCLE

```

module PulseDutyCycle (
    input iReset,
    input iClk,
    input iPPS,

    output oSynPulse
);

reg mOldPulse;
reg mState;

reg [25:0] mCount2;
reg [25:0] mCount1;
reg [25:0] mCount; //67108864

always @(posedge iClk) //trigger by 60MHz clock
begin
    if (!iReset)
    begin
        case( mState )
            1'd0:
            begin
                if( mOldPulse==0 && wClk==1 ) //postive edge trigger
                begin
                    mCount = 0; //start to count
                    mOldPulse = wClk;
                    mState = 1;
                end
            else
            begin
                mCount = mCount + 1;
                mOldPulse = wClk;
                mState = 0;
            end
        end
        1'd1:
        begin
            if( mOldPulse==0 && wClk==1 )
            begin
                mCount2 = (mCount+1)/2; //add the first flag count,
                mCount1 = mCount; //save the total end count
                mCount = 0;
                mOldPulse = walk;
                mutata = 0;
            end
            else
            begin
                mCount = mCount + 1;
                mOldPulse = walk;
                mutata = 1;
            end
        end
    endcase
end

else if( ((mOldPulse==0)&&(walk==1)) || (mCount>=mCount1) )
begin
    mCount = 0;
    mOldPulse = walk;
end

else
begin
    mCount = mCount + 1;
    mOldPulse = walk;
end
end

assign oSynPulse = (mCount<=mCount2)? 1:0; //Output the
cycle pulse
endmodule
  
```

Achieve simple IR-data transmission from a PC's serial port

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Often, you need to transmit a couple of bits or bytes of data to a microcontroller without a direct cable connection. One simple way to achieve this goal is to use a widely available IR receiver, such as a TSOP17xx or similar receiver from Vishay (www.vishay.com) that finds use in IR-remote-control applications, such as TVs and VCRs. These devices are easy to implement because they require no external parts. These receivers usually work with a pulsed 38-kHz carrier and include an amplifier, automatic gain control, and a demodulator.

The main problem for simple applications is building the transmitter, which requires a 38-kHz start-stop oscillator, additional supply voltage, and modulating pulses in the millisecond and submillisecond range. These factors are difficult to control with PC operating systems. On the other hand, a PC's serial port at a standard transmission rate of 38,400 bps can generate precise bursts of 38.4-kHz data with a simple frequency doubler and two IR LEDs (Figure 1). When transmitting bytes with an alternating zero/one pattern (hex 55), each hex-55 byte generates a burst of 18 pulses, adding the

start and stop bit, and consecutive bytes can generate longer pulses.

The receiver needs pulse trains ranging from 10 to 70 pulses with approximately equal pauses between them; you can easily meet these requirements with this setup. You can generate short pauses by sending hex-0 bytes, although two pulses will transmit for each byte because of the start and stop bits. However, the receiver eliminates these pulses. Stopping the transmission for a time can generate longer pauses. You must occasionally insert longer pauses, depending on the receiver you use. You can achieve data transmission by using short and long bursts and an appropriate protocol.

The circuit in Figure 1 forms a high-pass filter with the output impedance of the serial port and the capacitor. The positive pulses drive one IR LED; the negative pulses drive the other. Both should point to the receiver. PC ports usually provide a maximum current of 5 to 20 mA and a voltage of $\pm 15\text{V}$, thus having an output resistance in the low-kilohm range. A current-limiting resistor is usually not necessary. A value of 1 to 10 nF for the capacitor works in most cases. The receiver is tolerant. You need to adjust the capacitor's value for non-PC ports, such as the microcontroller, which have lower impedance. In practical applications, you can reliably achieve a transmission distance of 2 to 4m with a peak LED current as low as 5 mA if you point the LEDs at the receiver. A sample program for the PC is available at the EDN version of this Design Idea at www.edn.com/071011di1. **EDN**

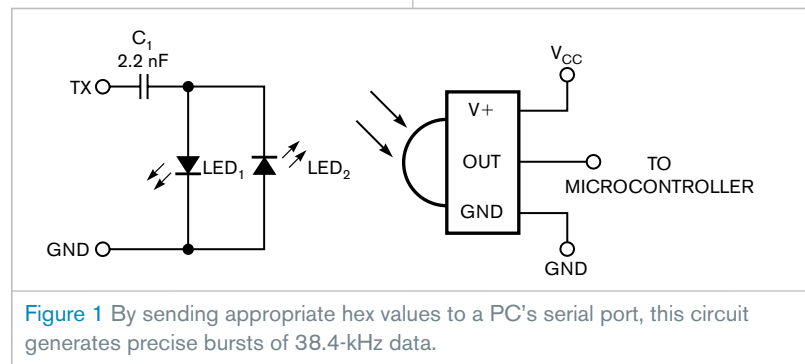


Figure 1 By sending appropriate hex values to a PC's serial port, this circuit generates precise bursts of 38.4-kHz data.

Circuit limits dV/dt and capacitor inrush at regulator turn-on

W Stephen Woodward, Chapel Hill, NC

Unusual design constraints sometimes reveal the unfriendly side of everyday components and circuits. A case in point is the design of power-supply-regulation circuitry in which the primary power source has an absolute current-limit specification, such as spacecraft photovoltaic, or "solar," panels and radioisotope-thermoelectric generators. Such appli-

cations require that you pay scrupulous attention to strict control of current consumption, including transient-current consumption, and infrequent consumption spikes, such as those that typically occur on power-up. The problem is that current-limited primary-power sources can suffer catastrophic voltage droop and shutdown in response to momentary overcurrent faults, even

when the fault is brief. Common causes of such faults are the current spikes that charge the regulator output's decoupling capacitor.

Unless the current limit of the regulator clips the resulting spikes, the spikes are equal to the regulator's output-voltage rate of rise multiplied by the sum of the parallel output capacitances: $I_{MAX} = dV/dt \times C_{OUT}$, where I_{MAX} is the maximum current, dV/dt is a differential in voltage with respect to a differential in time, and C_{OUT} is the output capacitance. The math suggests that the best strategy for limiting the regulator's turn-on maximum current is

to limit dV/dt . The circuit in **Figure 1** relies on this trick and works with industry-standard adjustable linear regulators, such as the popular low-dropout LM2941.

The basis of the dV/dt -limiting technique comprises the six added components: R_3 , R_4 , C_T , D_1 , D_2 , and Q_1 . On power-up, the control current through R_3 , C_T and D_2 delays the rise of the output voltage and thus prevents excessive maximum-current transients.

Here's how it works. When V_{IN} is on and Q_1 is off, current through R_3 , C_T , and D_2 pulls the adjust pin of the regulator to the reference. This action limits V_{OUT} 's dV/dt to the rate of C_T charging through the series resistance, $(R_3 + R_1 R_2 / (R_1 + R_2))$, and thereby limits I_{MAX} to any desired value using the design equations $R_3 = (V_{IN} - V_{REF} - 1) / V_{OUT}$, $R_4 = <20 R_3$, and $C_T = C_{OUT} V_{OUT} / (I_{MAX} (R_3 + R_1 R_2 / (R_1 + R_2)))$. For example, given the circuit constants in the **figure** and

assuming $C_{OUT} = 100 \mu\text{F}$, $dV/dt = 2500\text{V/s}$, and $I_{MAX} = 0.25\text{A}$. At the end of the modified power-up sequence, D_1 and D_2 decouple the dV/dt circuit

from the regulator's feedback network, preventing the coupling of ripple voltages from the input voltage into the output voltage. **EDN**

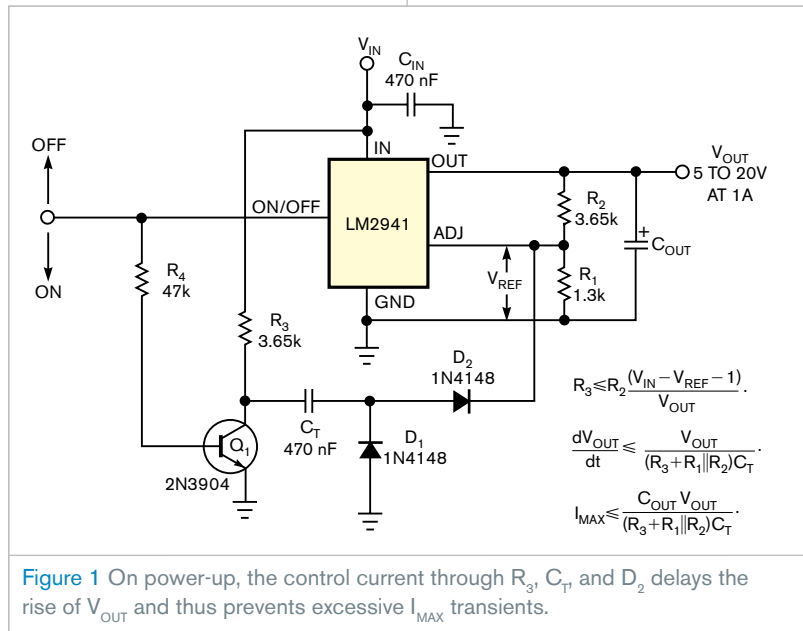


Figure 1 On power-up, the control current through R_3 , C_T and D_2 delays the rise of V_{OUT} and thus prevents excessive I_{MAX} transients.