LISTING 1 GENERATING 50% DUTY CYCLE

```
module PulseDutyCycle  (
            input  iReset,
            input  iClk,
            input  iPPS,

            output  oSynPulse
           );

 reg   mOldPulse;
 reg    mState;

 reg   [25:0]  mCount2;
 reg   [25:0]  mCount1;
 reg   [25:0]  mCount;      //67108864


 always @( posedge iClk )    //trigger by 60MHz clock
 begin
  if( !iReset )
  begin
  case( mState )
    1'd0:
    begin
      if( mOldPulse==0 && wClk==1 )  //postive edge trigger
      begin
        mCount     = 0;    //start to count
        mOldPulse   = wClk;
        mState     = 1;
      end
      else
      begin
        mCount       = mCount  +  1;
        mOldPulse   = wClk;
        mState     = 0;
      end
    end
    1'd1:
    begin
      if( mOldPulse==0 && wClk==1 )
      begin
        mCount2   =   (mCount+1)/2;     //add the first flag count,
the first count done,and divide by two
        mCount1    = mCount;          //save the total end count
        mount    = 0;
        mold Pulse  =  walk;
        mutate    = 0;
      end
      else
      begin
        mount    = mount  +  1;
        mold Pulse  =  walk;
        mutate    = 1;
      end
    end
  encase
  end

  else if( ((mold Pulse==0)&&(walk==1)) || (mount>=mCount1)
  begin
    mount    = 0;
    mold Pulse  =  walk;
  end

  else
  begin
    mount    = mount  +  1;
    mold Pulse  =  walk;
  end
 end

  assign oSynPulse  =  (mCount<=mCount2)? 1:0 ; //Output the
cycle pulse

endmodule
```