

GREENHORNS IN THE HIGH-END-FPGA MARKET, LATTICE AND ACTEL ARE SHOOTING IT OUT AGAINST OLD HANDS XILINX AND ALTERA IN THE BATTLE FOR LOW-COST DEVICES.

High noon for FPGAs: LOW-COST-VERSUS- HIGH-END SHOWDOWN

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Although the market for high-end, high-priced SRAM-based FPGAs has matured into a gentlemanly duel between FPGA veterans Xilinx Inc and Altera Corp, the emerging low-cost-FPGA market has turned into the FPGA industry's version of the *Gunfight at the OK Corral*. Companies including Lattice Semiconductor and Actel Corp are fighting it out with each other as well as with Xilinx and Altera, increasingly adding advanced functions—traditionally the province of high-end, high-priced FPGAs—to their low-cost-FPGA families. In the very-high-end-FPGA market, customers mainly have a choice between either Xilinx's Virtex devices or Altera's

Stratix family. In the low-cost-FPGA market, however, customers have many more choices and benefit from the stepped-up competition between the

many vendors fighting it out for FPGA revenue. Today, customers can buy 1 million-gate FPGAs with high-speed I/O and processor or DSP capabilities for

much less than \$100 in low volumes and for tens of dollars in high volumes.

This competition has benefited users but has—and at least temporarily—come at the expense of the FPGA industry's overall revenue. The media has widely covered the FPGA industry's success at the ASIC market's expense, replacing sockets that ASICs traditionally held. During the past year, however, the FPGA industry has had a dose of its own medicine, as the low-cost-FPGA market has quietly begun to take socket wins—and, thus, revenue—away from the high-end-FPGA market.

Bryan Lewis, research vice president with research company Gartner, notes that the FPGA industry has since 2002 sold a steadily increasing number of devices. However, Gartner predicts that

the FPGA industry will show a decline this year, due in part to low-cost FPGAs' replacement of sockets that high-end FPGAs traditionally held. "Low-cost-FPGA units are ramping fast, but their lower ASPs [average selling prices] are clearly having an impact on the dollar growth of the overall FPGA market," says Lewis. "In fact, we now forecast 2007 FPGA/PLD [programmable-logic-device] revenues to decline 1.9%." That anticipated decline is not due entirely to FPGA-industry cannibalism, he says. In 2007, the FPGA market underwent "the perfect storm," says Lewis, simultaneously experiencing inventory, customer-consolidation, and pricing issues. He expects overall FPGA/PLD-market revenue to come roaring back in 2008 to post 14.4% revenue growth (Figure 1).

But the two biggest upstarts—and, some would say, spoilers—in the low-cost-FPGA market are Actel and Lattice, which are maintaining their push to add high-end functions in their low-cost devices, putting severe price pressure on Xilinx's and Altera's high-end FPGAs. Both Actel and Lattice claim that the large FPGA vendors have traditionally deliberately withheld high-end functions from their low-cost FPGAs to force users to buy their typically three-times-more-expensive high-end FPGAs. Both upstarts claim that the high-end-FPGA vendors are starting to buckle under the pressure, and one of the first signs of this surrender is Altera's latest product introduction, the 90-nm Arria GX. The upstarts claim that Arria GX is simply a 90-nm Stratix II GX device with a different package. Although Altera concedes that it based Arria GX on a Stratix II GX architecture, the company says that the Arria GX lacks some of the features and performance of the Stratix II GX device. The company claims that it merely slimmed down the Stratix II GX to meet the right mix of performance, power requirements, and price to fulfill the needs of the market with the Arria GX. The Arria GX's price falls between the company's low-cost Cyclone and its high-end Stratix devices. "Lattice has changed the playing field for the SRAM guys," says Martin Mason, director of silicon-product marketing at Actel. "It's a market that Actel has not historically played in. But Altera and Xilinx have

AT A GLANCE

Low-cost FPGAs generally target use in products, rather than as FPGA-prototyping vehicles.

Xilinx introduced the first low-cost FPGAs in 1998 and reports that Spartan has produced \$2.1 billion in cumulative revenue with a compound-annual-growth rate of 36.2% from fiscal year 2000 through 2006.

Customers are now replacing high-end-FPGA sockets with low-cost-FPGA sockets in much the same way that FPGAs once displaced low-end ASICs.

Research company Gartner predicts that FPGA/PLD (programmable-logic-device) revenues will decline 1.9% in 2007, due in part to FPGA cannibalism.

Low-cost FPGAs are fine for some applications, but some FPGAs require extra power circuitry that may add to the overall cost of a system.

Customers should also take into account the FPGA vendor's EDA-tool set when shopping for low-cost FPGAs.

and Altera are furious over the impact that [move] is having on the high-end business."

Mason believes that the high-end-FPGA vendors are now experiencing a classic example of the innovator's dilemma (Reference 1). "You have this market, you're getting fat and happy in it, and someone comes in with a disruptive technology and starts taking market share away from you. Do you go in and try to compete with them by lowering your prices? If you do, then you actually trash the market that has gotten you where you are," says Mason. "All of us in the FPGA market have been doing that to the ASIC market, but both we and Lattice have little to lose and everything to gain by introducing disruptive technologies against the Big Two in FPGAs."

Xilinx and Lattice are not throwing in the towel, however. Neither is content to simply replace high-end-FPGA sockets with low-cost FPGAs, and neither plans to reduce the prices of their high-end FPGAs to fend off competition from low-cost FPGAs. Each instead hopes to serve markets that FPGAs have not traditionally served (see sidebar "Low-cost FPGAs seek new markets").

sold a lot of high-end devices into the market for high-speed I/O, and Lattice went in there overnight and took out one digit from the amount people could charge for high-speed SERDES [serializer/deserializer] products. I'm sure Xilinx

A LITTLE HISTORY

In 1998, Xilinx introduced the first low-cost FPGAs, the Spartan family, and aimed it squarely at replacing ASICs for production parts. Before the product's

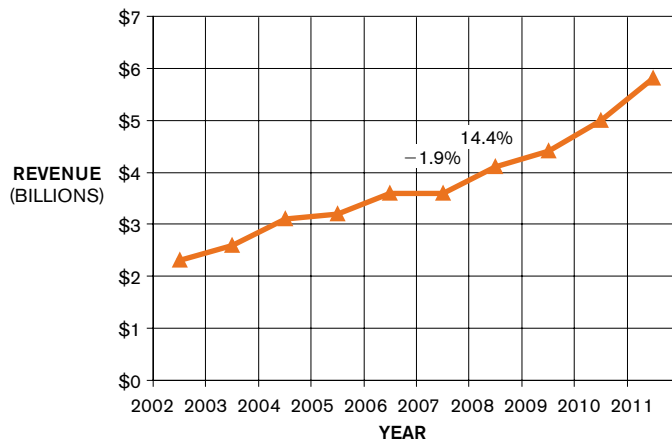


Figure 1 Research company Gartner predicts that FPGA/PLD revenue will decline 1.9% in 2007 in part because low-power FPGAs are taking market share away from high-end FPGAs. But Gartner predicts that the FPGA revenue will spring back to grow 14.4% in 2008.

release, IC-design engineers had used FPGAs mainly for prototyping ASIC designs and would ultimately implement those designs in cheaper, faster, higher capacity ASICs. In those days, PLDs lacked the performance, capacity, and power requirements for use in end products, and, more important, they were too expensive. At the time, many PLD vendors also offered low-cost CPLDs (complex PLDs), but performance and capacity limitations hampered—and still hamper—those parts. Still, some customers used them in sockets that older and less sophisticated ASIC devices traditionally held.

The Spartan family, however, opened a new market and offered formidable capacity, performance, and numbers of functions at a reasonably low price and thus started to displace midrange ASICs in end products. This scenario was especially true in applications that required versatility and reprogrammability and those requiring too few units to justify the cost of spinning an ASIC. Xilinx

THE SPARTAN FAMILY OPENED A NEW MARKET AND OFFERED FORMIDABLE CAPACITY, PERFORMANCE, AND NUMBERS OF FUNCTIONS AT A REASONABLY LOW PRICE.

has shipped more than 230 million devices worldwide, according to Mark Moran, senior strategic-marketing manager for the General Products Division at the company. Those sales have yielded \$2.1 billion in cumulative revenue with a compound-annual-growth rate of 36.2% from fiscal year 2000 through fiscal year 2006.

As foundries have introduced semiconductor processes that are more dif-

ficult to manufacture and more expensive to design, both the low-cost-FPGA and the high-end-FPGA markets have grown and have grabbed more sockets away from the ASIC market. When Xilinx jumped into the low-cost-FPGA market, Altera, Actel, and Lattice soon followed. The first devices they offered were traditional sea-of-gate devices that consisted mostly of reprogrammable logic. But, as new market opportunities opened, most of the FPGA vendors started to add hard-wired functions, such as microprocessors; DSPs; memory; high-speed SERDES; and support for popular interfaces, such as PCIe (Peripheral Component Interconnect Express), to their architectures to capture specific markets and one-up competitors in not only the ASIC market, but also the FPGA market.

The low-cost-FPGA shoot-out has indeed escalated the size, performance, low-power requirements, and number of advanced functions these devices have, yet they maintain a price that allows

LOW-COST FPGAs SEEK NEW MARKETS

SRAM FPGAs found their first big successes mainly as glue logic, helping ASIC designers add functions at the last minute that they accidentally omitted, for example, or facilitating communication between processors and memory in telecom and networking systems. FPGAs vendors then started adding RapidIO blocks to their FPGA architectures and realized further success in markets such as telecom and communications. They then added processors, DSP capabilities, and security.

You can now find low-cost FPGAs everywhere—at home, in your automobile, at work, and in various industries, according to Mark Moran, senior strategic-marketing manager for the General Products Division at Xilinx. The market for consumer products, such as set-top boxes, is now perhaps the biggest market for FPGAs. It was also one of the first segments in which Altera saw big success with its low-cost FPGAs, according to Danny Biran, senior vice president of product and corporate marketing at the company. “Customers in this market traditionally release 10 or more models a year, and they can customize FPGAs to suit not only each product line, but also each unit,” he says. For example, each TV manufacturer can use FPGAs to fix pixel, color, or shading problems on a case-by-case basis. The devices also find use in data conversion for modems and set-top boxes. “The next generation of devices in these areas will become even more integrated and re-

quire even more FPGAs,” say Moran, noting that some TV vendors are starting to include DVR (digital-video-recording) functions in their HDTVs (high-definition televisions).

FPGAs have also found great wins in the automotive market. Initially, FPGAs counted success in GPS (global-positioning-system) navigation and back-seat DVDs in a mix of after-market and OEM products. However, as vendors offer more nonvolatile devices to their lineups, low-cost-FPGA use in automobiles is expanding beyond infotainment and GPS units. For example, Actel’s products are now finding use in automotive backup-safety systems, cameras, and power-train systems. In most of these cases, FPGAs are displacing ASICs or eliminating the need for multiple discrete devices on a PCB (printed-circuit board), saving board space. In others, low-cost FPGAs are replacing high-end FPGAs.

The market for systems that operate in the ISM (industrial/scientific/medical) frequency band is probably the biggest battleground between high-end FPGAs and low-cost FPGAs. The big trend in this area is toward wireless and battery-powered systems, so the requirement for low power consumption plays a large role. “It forces customers into a value-based play because the high-end-FPGA power hogs use a lot of static and dynamic power and are unsuitable for applications that are going portable for the first time,” says Mason.

customers to justify using the devices rather than ASICs, standard-cell ASSPs (application-specific-standard products), or implementations that combine discrete functions on PCBs (printed-circuit boards). Creating low-cost FPGAs for emerging markets is difficult, and all the players offering low-cost FPGAs say it's a balancing act to keep raising the bar on performance and features in ever-more-expensive process technologies. They must achieve this goal while keeping prices low enough that customers will find their devices attractive as production parts, rather than as prototyping parts for ASICs.

It's a balancing act for FPGA customers, too. Although an FPGA may have a lower per-unit cost than an ASIC, customers must look closely at each device's system requirements. Actel's Mason, for example, is quick to point out that SRAM FPGAs remain power hogs and typically require users to add extra power-control circuitry and power bricks to their PCBs to run SRAM FPGAs.

MOST FPGA-MARKET PUNDITS WILL LIKELY AGREE THAT THE FPGA INDUSTRY AS A WHOLE IS TODAY FIELDING A BRILLIANT ARRAY OF LOW-COST DEVICES FOR A GROWING NUMBER OF APPLICATIONS AND MARKETS.

Some also need external boot-up memory, which may require users to buy an external boot device or to increase the boot-up requirements of their targeted processors. Customers for SRAM-based FPGAs must also heed the rule of 80%; that is, they must buy an FPGA that has 20% more gates than they require if they intend to hit the FPGA vendor's advertised performance grade (**Refer-**

ence 2). Altera's senior vice president of product and corporate marketing, Danny Biran, and Xilinx's Moran, also point out that EDA software is a big differentiator in this market and that the smaller vendors' design software lags behind the offerings of the big vendors. Biran also notes that transceiver-targeted FPGAs typically add complexity to users' system designs; thus, FPGA vendors attacking this market must also offer software to help designers adequately program the devices into their systems. "If you look at the vendors offering these types of devices and then you look at the software they offer with the devices, it's again a Coke-and-Pepsi market," says Biran, referring to the long-standing so-called Cola Wars between Coca-Cola and Pepsi (**Reference 3**), an analogy describing the situation when two companies—in this case, Xilinx and Altera—dominate a mature market.

Although designers should be aware of some facts when shopping for devices in the low-end market, most FPGA-market pundits will likely agree that the FPGA industry as a whole is today fielding a brilliant array of low-cost devices for a growing number of applications and markets. **Table 1**, available at the online version of this article at www.edn.com/071108df1, lists the latest low-cost-FPGA offerings from Actel, Altera, Lattice, and Xilinx. "You can get a lot of cool stuff for less than \$20," says Actel's Mason.

THE OLD-TIMERS

First, take a look at what the old hands have to offer. Xilinx offers the Spartan, Spartan-2, and Spartan-3 generations of its high-pin-count, high-density, low-cost-FPGA device. With the introduction of each successive generation, Xilinx has broadened its portfolio to capture new markets. Of the FPGA vendors offering low-cost FPGAs, Xilinx has the broadest portfolio, fielding five versions of its 65-nm SRAM-based Spartan-3 family and multiple densities and speed grades for each version. The logic-optimized Spartan-3E is a traditional sea-of-logic-gates FPGA. The Spartan-3A targets I/O for high-speed applications, and the Spartan-3A DSP targets DSP applications. The newest addition to the lineup is the Spartan-

3AN, which is essentially a Spartan-3E that Xilinx couples with a flash on an SIP (system in package) for nonvolatile-system applications. Although each device targets its own market segment, each shares flexible power-management modes for low cost, along with “device-DNA” security technology, which helps customers prevent theft of their designs.

As for the other veteran in the market, Altera offers its low-cost, SRAM-based Cyclone FPGA family, which debuted in 2002 in a 130-nm-process technology. The company in 2004 introduced the 90-nm Cyclone II and, in 2007, the Cyclone III in TSMC’s (Taiwan Semiconductor Manufacturing Co, www.tsmc.com) 65-nm LP (low-power) process technology. As of press time, Altera offered eight speed grades of its Cyclone III products ranging from 5000 to 120,000 logic elements, with as much as 4 Mbits of embedded memory and as many as 288 DSP multipliers running at 260 MHz.

This year, the company also introduced its Arria line of FPGAs to target

users needing reprogrammable devices with highly functioning, relatively low-cost transceivers. Arria GX has a higher price and better performance than Cyclone because it supports three protocols: PCIe, GbE (Gigabit Ethernet), and SRIIO (Serial RapidIO).

Arria GX and the high-end Stratix II GX use the same logic fabric, transceiver technology, and process technology, but they differ in a number of ways: Arria GX is slower and is available in lower cost packages, and its transceivers support speeds of only 2.5 Gbps and have fewer functions. For example, Arria GX devices lack support for adaptive equalization, a feature you’ll find in Altera’s high-end Stratix II GX.

ENTER THE UPSTARTS

Lattice jumped into the low-cost-FPGA market at the end of 2002 with its 130-nm ECP (Economy Plus) family. The company last year followed up that introduction with the 90-nm ECP2 family and then this year with its ECP2M family. ECP2M adds two

significant high-end features to the low-cost-FPGA market: hard-wired 3-Gbps SERDES and as much as 5 Mbits of on-chip memory, supporting DDR and DDR2 I/O, SPI (serial-peripheral-interface) 4.2 I/O, and hard-wired DSP support. Lattice also offers the XP and XP2 families, which debuted in 2005 and February of this year, respectively. The XP2 family marries an SRAM ECP2 architecture with a bank of flash memory on one die. “We are trying to make the SRAM-based FPGA plus its associated boot-flash memory about the same price as its equivalent nonvolatile product,” says Gordon Hands, director of strategic marketing at Lattice, who notes that the XP is similar to Lattice’s original ECP family and that the XP2 is similar to the ECP2 devices but with slightly smaller density.

While Xilinx, Altera, and Lattice battle it out in low-cost, SRAM-based FPGAs, Actel, which offers flash-based devices, is content to broaden its low-cost-FPGA-market reach into applications requiring security and low power

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consumption. Flash-based FPGAs have traditionally been slower than SRAM-based FPGAs, but flash-based devices consume less power and are more secure than SRAM-based devices. The company's low-cost ProASIC3 FPGA focuses on the combination of low power, security, and relatively high density and is available in seven versions, with densities of 30,000 to 1 million system gates. The company based its flash-based Igloo FPGA family, which debuted last year, on the ProASIC3 but with added modes to further reduce power. The smallest device in the Igloo family, the AGLO30, can operate on as little as 5 μ W, and the largest device operates at less than 1 mW, which is two or three orders of magnitudes lower than its SRAM competitors.

Actel also has an agreement with ARM (www.arm.com) that allows users to place a hardened ARM7 core on Actel's FPGAs for very-low-power use. "When you put an ARM processor on the device, you can get as low as 24- μ A standby current for that implementation. The business model allows Actel to provide the ARM processor to customers free of royalty, licensing, and price," says Actel's Mason.

Quicklogic no longer considers itself an FPGA vendor, but its low-power PolarPro and ArcticLink CSSPs (customer-specific standard products) are worth mentioning. The one-time-programmable devices function as extremely low-power "sandman" devices—turning off power to parts of handheld systems when they are not in use, thus conserving a given system's overall power consumption. The PolarPro devices boast 10 μ A of static-power consumption, 15 mA of active-power consumption, and 10 μ A of dynamic-power consumption. ArcticLink devices essential-

ly marry a PolarPro programmable array with hard-wired functions on a die targeting markets for low-power systems.

THE MEASURE OF SUCCESS

Overall, in recent years, the FPGA industry has done remarkably well taking share away from the ASIC market and giving users a very-low-cost and relatively stable alternative for quickly designing innovative next-generation products. Historically, customers, the media, and the financial community have measured FPGA-vendor success by a company's ability to be first to market with high-end devices on the latest silicon processes. However, as companies such as Lattice and Actel introduce low-cost devices with high-end features and increase pressure on Xilinx and Altera to follow suit, industry participants may soon define FPGA success by a vendor's ability to serve emerging markets with the right mix of features, performance, power savings, and price that customers find reasonable for production use. **EDN**

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Company	Low-cost FPGA family	Application/ features focus	Density range	Top performance (logic, I/O)
Actel Corp	Igloo/IglooE	The Actel Igloo family of reprogrammable, full-featured flash FPGAs meets the demanding power and area requirements of portable electronics.	30,000 to 3 million system gates	Maximum 616 I/Os
	ProASIC3/ ProASIC3E	The ProASIC3/E families of flash FPGAs offer performance, density, and features for consumer-automotive and industrial applications.	30,000 to 3 million system gates	Maximum 616 I/Os
Altera Corp	Cyclone	Altera builds the Cyclone series of FPGAs from the ground up for cost-sensitive, high-volume applications. These low-cost devices provide application-focused features, such as embedded memory, external-memory interfaces, and clock-management circuitry.	3000 to 20,000 LEs (logic elements), as many as 250,000 equivalent ASIC gates	LVDS at 640 Mbps, DDR at 167 MHz, maximum clock frequency at 200 MHz
	Cyclone II	Cyclone II devices include customer-defined FPGA features for low-cost applications, including a wide range of density, memory, embedded-multiplier, and packaging options.	5000 to 70,000 LEs (logic elements), as many as 875,000 equivalent ASIC gates	LVDS at 805 Mbps, DDR at 167 MHz, DDR2 at 167 MHz, maximum clock frequency at 260 MHz
	Cyclone III	Cyclone III FPGAs combine low power, high functionality, and low cost.	5000 to 120,000 LEs (logic elements), as many as 1.5 million equivalent ASIC gates	LVDS at 840 Mbps, DDR at 167 MHz, DDR2 at 200 MHz, maximum clock frequency at 280 MHz
	Arria GX	Arria GX devices target high-volume, cost-sensitive, transceiver-based markets, such as wireless communications, video processing, military, industrial, and computation and storage.	21,500 to 90,200 LEs (logic elements), as many as 1.2 million equivalent ASIC gates	Performance varies based on design, I/O LVDS at 840 Mbps, support for DDR2 at 233 MHz
Lattice Semiconductor	LatticeECP2	Lattice ECP2 devices target high-volume applications in which I/O and DSP performance previously required the use of high-performance and high-cost FPGAs.	300,000 to 5 million ASIC gates	350-MHz logic, 840-Mbps I/O
	LatticeECP2M	Lattice ECP2M devices target high-volume applications in which I/O and DSP performance, SERDES (serializer/deserializer), or memory capacity previously required the use of high-performance and high-cost FPGAs.	5 million to 20 million ASIC gates	350-MHz logic, 840-Mbps I/O, and 3.2-Gbps SERDES (serializer/deserializer)
	LatticeXP2	Lattice XP2 devices target high-volume applications requiring the smallest board area, instant availability of logic at power-up, and FPGA security.	725,000 to 4 million ASIC gates	320-MHz logic, 840-Mbps I/O
Xilinx	Spartan-3 generation	The Spartan-3 generation targets high-density, high-pin-count, and highly integrated data-processing applications.	50,000 to 5 million system gates	622-psec data-transfer rate per differential I/O, 33-MHz PCI, DDR and DDR2 support as fast as 333 Mbps, 18- to 280-MHz DCM (digital-clock-manager) input frequency, as many as 74,880 logic cells, as many as 784 single-ended I/Os, as many as 344 differential-I/O pairs, as many as 104 multipliers

	Hard-wired logic	On-chip memory	Material	Power requirement	Price range
	PLL	As many as 112 blocks of 4608-bit embedded SRAM (variable configurations); 1024 bits of on-chip, user-accessible, nonvolatile flash ROM	Flash	5 to 294 μ W	\$1.50 to \$95
	PLL	As many as 112 blocks of 4608-bit embedded SRAM (variable configurations), 1024 bits of on-chip flash ROM	Flash	3 to 37 mW	\$1.50 to \$95
	As many as two PLLs	As much as 288 kbits of RAM	SRAM	20 to 500 mA, depending on design	Contact Altera
	As many as 150 18 \times 18 multipliers, as many as four PLLs	1.1 Mbits of RAM	SRAM	Power-up current requirement of 20 to 500 mA, depending on design; static power of 35 to 250 mA	Contact Altera
	As many as four PLLs, as many as 288 18 \times 18 multipliers	As much as 4 Mbits of RAM	SRAM	Power-up current requirement of 10 to 500 mA, depending on design; static power of 35 to 160 mA	EP-3C5E144C8: \$4 (500,000)
	Four to 12 SERDES (serializer/deserializer) blocks at speeds as high as 2.5 Gbps, 10 to 44 DSP blocks, 230 to 538 high-speed user-I/O blocks	1.2 to 4.5 Mbits	SRAM	Design-dependent power-up-current requirement	\$46 to \$280
	sysDSP blocks, pre-engineered logic supporting 533-Mbps DDR2, 400-Mbps DDR, 750-Mbps SPI4.2, 840-Mbps generic interfaces	55 kbits to 1 Mbit	SRAM	130- to 237-mW static power plus design's switching power	\$4.50 to \$40 (high volumes)
	3.2-Gbps SERDES (serializer/deserializer), sysDSP blocks, pre-engineered logic supporting 533-Mbps DDR2, 400-Mbps DDR, 750-Mbps SPI4.2, 840-Mbps generic interfaces	1.2 to 5.3 Mbits	SRAM	150- to 285-mW static power plus design's switching power	\$15 to \$120 (high volumes)
	sysDSP blocks, pre-engineered logic supporting 400-Mbps DDR2, 400-Mbps DDR, 840-Mbps generic interfaces	166 to 885 kbits	Hybrid SRAM/flash on single die	90- to 195-mW static power plus design's switching power	\$5.50 to \$30 (high volumes)
	18 \times 18-bit multipliers, 18-kbit block RAM, DCMs (digital-clock managers), advanced-I/O block with DDR registers, 24 differential- and single-ended standards, single-ended and differential termination	As much as 1872 kbits of block RAM, as much as 520 kbits of distributed RAM	SRAM	13.5- to 193.5-mA typical quiescent current	XC3S4000: \$19.95 (250,000)

Spartan-3E platform	The Spartan-3E platform is logic-optimized for logic integration, DSP coprocessing, and embedded control.	100,000 to 1.6 million system gates	270-MHz block RAM, 270-MHz multiplier, more-than-622-Mbps data-transfer rate per differential I/O, DDR and DDR2 support as fast as 333 Mbps, as many as 33,192 logic cells, as many as 376 single-ended I/Os, as many as 156 differential-I/O pairs, as many as 36 multipliers
Spartan-3A platform	The Spartan-3A platform targets applications requiring extensive I/O, such as bridging, differential signaling, and memory interfacing.	50,000 to 1.4 million system gates	270-MHz block RAM, 280-MHz multiplier, more-than-622-Mbps data-transfer rate per differential I/O, DDR and DDR2 support as fast as 400 Mbps, as many as 25,344 logic cells, as many as 502 single-ended I/Os, as many as 227 differential-I/O pairs, as many as 32 multipliers
Spartan-3AN platform	The nonvolatile Spartan-3AN platform targets applications requiring nonvolatile system integration, security, or large amounts of user-accessible flash.	50,000 to 1.4 million system gates	270-MHz block RAM, 280-MHz multiplier, more-than-622-Mbps data-transfer rate per differential I/O, 66-MHz PCI, DDR and DDR2 support as fast as 400 Mbps, 5- to 320-MHz DCM (digital-clock-manager) input frequency, as many as 25,344 logic cells, as many as 502 single-ended I/Os, as many as 227 differential-I/O pairs, as many as 32 multipliers
Spartan-3A DSP platform	The Spartan-3A DSP platform targets digital-signal processing in applications requiring integrated DSP MAC (multiply/accumulate) operations and expanded memory.	1.8 million to 3.4 million system gates	270-MHz block RAM, 287-MHz DSP48A/multiplier, more-than-622-Mbps data-transfer rate per differential I/O, DDR and DDR2 support as fast as 333 Mbps, as many as 53,712 logic cells, as many as 519 single-ended I/Os, as many as 227 differential-I/O pairs, as many as 126 DSP48A slices (advanced multiply/accumulate elements) or 126 18×18-bit multipliers

	18×18-bit multipliers, 18-kbit block RAM, DCMs (digital-clock managers), advanced-I/O block with DDR registers, 18 differential- and single-ended standards, differential termination, multiboot-configuration logic	As much as 648 kbits of block RAM, as much as 231 kbits of distributed RAM	SRAM	16.8- to 111.5-mA typical quiescent current	XC3S100E: \$1.75 (250,000)
	Device DNA, 18×18-bit multipliers, 18-kbit block RAM, DCMs (digital-clock managers), advanced-I/O block with DDR registers, 26 differential- and single-ended standards, differential termination, power-management modes, multiboot-configuration logic with watchdog timer	As much as 576 kbits of block RAM, as much as 176 kbits of distributed RAM	SRAM	0-mA quiescent current in hibernation mode, 7.7- to 48.3-mA typical quiescent current, 4.6- to 29-mA typical quiescent current in suspend mode	XC3S200A: \$4.25 (250,000)
	Device DNA, 18×18-bit multipliers, 18-kbit block RAM, DCMs (digital-clock managers), advanced-I/O block with DDR registers, 26 differential- and single-ended standards, differential termination, power-management modes, multiboot-configuration logic with watchdog timer	As much as 11 Mbits of non-volatile, user-accessible flash; as much as 576 kbits of block RAM; as much as 176 kbits of distributed RAM	SRAM plus flash on system in package	0-mA quiescent current in hibernation mode, 7.8- to 48.4-mA typical quiescent current, 4.6- to 29-mA typical quiescent current in suspend mode	XC-3S200AN: \$4.90 (250,000)
	Device DNA, DSP48A slices (advanced multiply/accumulate elements), 18-kbit block RAM, DCMs (digital-clock managers), advanced-I/O block with DDR registers, 24 differential- and single-ended standards, differential termination, power-management modes, multiboot-configuration logic with watchdog timer	As much as 2268 kbits of block RAM, as much as 373 kbits of distributed RAM	SRAM	0-mA quiescent current in hibernation mode, 83.2- to 135.2-mA typical quiescent current, 49.8- to 81.1-mA typical quiescent current in suspend mode	XC-3SD3400A: \$44.95 (25,000)