

Company	Low-cost FPGA family	Application/ features focus	Density range	Top performance (logic, I/O)
Actel Corp	Igloo/IglooE	The Actel Igloo family of reprogrammable, full-featured flash FPGAs meets the demanding power and area requirements of portable electronics.	30,000 to 3 million system gates	Maximum 616 I/Os
	ProASIC3/ ProASIC3E	The ProASIC3/E families of flash FPGAs offer performance, density, and features for consumer-automotive and industrial applications.	30,000 to 3 million system gates	Maximum 616 I/Os
Altera Corp	Cyclone	Altera builds the Cyclone series of FPGAs from the ground up for cost-sensitive, high-volume applications. These low-cost devices provide application-focused features, such as embedded memory, external-memory interfaces, and clock-management circuitry.	3000 to 20,000 LEs (logic elements), as many as 250,000 equivalent ASIC gates	LVDS at 640 Mbps, DDR at 167 MHz, maximum clock frequency at 200 MHz
	Cyclone II	Cyclone II devices include customer-defined FPGA features for low-cost applications, including a wide range of density, memory, embedded-multiplier, and packaging options.	5000 to 70,000 LEs (logic elements), as many as 875,000 equivalent ASIC gates	LVDS at 805 Mbps, DDR at 167 MHz, DDR2 at 167 MHz, maximum clock frequency at 260 MHz
	Cyclone III	Cyclone III FPGAs combine low power, high functionality, and low cost.	5000 to 120,000 LEs (logic elements), as many as 1.5 million equivalent ASIC gates	LVDS at 840 Mbps, DDR at 167 MHz, DDR2 at 200 MHz, maximum clock frequency at 280 MHz
	Arria GX	Arria GX devices target high-volume, cost-sensitive, transceiver-based markets, such as wireless communications, video processing, military, industrial, and computation and storage.	21,500 to 90,200 LEs (logic elements), as many as 1.2 million equivalent ASIC gates	Performance varies based on design, I/O LVDS at 840 Mbps, support for DDR2 at 233 MHz
Lattice Semiconductor	LatticeECP2	Lattice ECP2 devices target high-volume applications in which I/O and DSP performance previously required the use of high-performance and high-cost FPGAs.	300,000 to 5 million ASIC gates	350-MHz logic, 840-Mbps I/O
	LatticeECP2M	Lattice ECP2M devices target high-volume applications in which I/O and DSP performance, SERDES (serializer/deserializer), or memory capacity previously required the use of high-performance and high-cost FPGAs.	5 million to 20 million ASIC gates	350-MHz logic, 840-Mbps I/O, and 3.2-Gbps SERDES (serializer/deserializer)
	LatticeXP2	Lattice XP2 devices target high-volume applications requiring the smallest board area, instant availability of logic at power-up, and FPGA security.	725,000 to 4 million ASIC gates	320-MHz logic, 840-Mbps I/O
Xilinx	Spartan-3 generation	The Spartan-3 generation targets high-density, high-pin-count, and highly integrated data-processing applications.	50,000 to 5 million system gates	622-psec data-transfer rate per differential I/O, 33-MHz PCI, DDR and DDR2 support as fast as 333 Mbps, 18- to 280-MHz DCM (digital-clock-manager) input frequency, as many as 74,880 logic cells, as many as 784 single-ended I/Os, as many as 344 differential-I/O pairs, as many as 104 multipliers

	Hard-wired logic	On-chip memory	Material	Power requirement	Price range
	PLL	As many as 112 blocks of 4608-bit embedded SRAM (variable configurations); 1024 bits of on-chip, user-accessible, nonvolatile flash ROM	Flash	5 to 294 $\mu$ W	\$1.50 to \$95
	PLL	As many as 112 blocks of 4608-bit embedded SRAM (variable configurations), 1024 bits of on-chip flash ROM	Flash	3 to 37 mW	\$1.50 to \$95
	As many as two PLLs	As much as 288 kbits of RAM	SRAM	20 to 500 mA, depending on design	Contact Altera
	As many as 150 18 $\times$ 18 multipliers, as many as four PLLs	1.1 Mbits of RAM	SRAM	Power-up current requirement of 20 to 500 mA, depending on design; static power of 35 to 250 mA	Contact Altera
	As many as four PLLs, as many as 288 18 $\times$ 18 multipliers	As much as 4 Mbits of RAM	SRAM	Power-up current requirement of 10 to 500 mA, depending on design; static power of 35 to 160 mA	EP-3C5E144C8: \$4 (500,000)
	Four to 12 SERDES (serializer/deserializer) blocks at speeds as high as 2.5 Gbps, 10 to 44 DSP blocks, 230 to 538 high-speed user-I/O blocks	1.2 to 4.5 Mbits	SRAM	Design-dependent power-up-current requirement	\$46 to \$280
	sysDSP blocks, pre-engineered logic supporting 533-Mbps DDR2, 400-Mbps DDR, 750-Mbps SPI4.2, 840-Mbps generic interfaces	55 kbits to 1 Mbit	SRAM	130- to 237-mW static power plus design's switching power	\$4.50 to \$40 (high volumes)
	3.2-Gbps SERDES (serializer/deserializer), sysDSP blocks, pre-engineered logic supporting 533-Mbps DDR2, 400-Mbps DDR, 750-Mbps SPI4.2, 840-Mbps generic interfaces	1.2 to 5.3 Mbits	SRAM	150- to 285-mW static power plus design's switching power	\$15 to \$120 (high volumes)
	sysDSP blocks, pre-engineered logic supporting 400-Mbps DDR2, 400-Mbps DDR, 840-Mbps generic interfaces	166 to 885 kbits	Hybrid SRAM/flash on single die	90- to 195-mW static power plus design's switching power	\$5.50 to \$30 (high volumes)
	18 $\times$ 18-bit multipliers, 18-kbit block RAM, DCMs (digital-clock managers), advanced-I/O block with DDR registers, 24 differential- and single-ended standards, single-ended and differential termination	As much as 1872 kbits of block RAM, as much as 520 kbits of distributed RAM	SRAM	13.5- to 193.5-mA typical quiescent current	XC3S4000: \$19.95 (250,000)

Spartan-3E platform	The Spartan-3E platform is logic-optimized for logic integration, DSP coprocessing, and embedded control.	100,000 to 1.6 million system gates	270-MHz block RAM, 270-MHz multiplier, more-than-622-Mbps data-transfer rate per differential I/O, DDR and DDR2 support as fast as 333 Mbps, as many as 33,192 logic cells, as many as 376 single-ended I/Os, as many as 156 differential-I/O pairs, as many as 36 multipliers
Spartan-3A platform	The Spartan-3A platform targets applications requiring extensive I/O, such as bridging, differential signaling, and memory interfacing.	50,000 to 1.4 million system gates	270-MHz block RAM, 280-MHz multiplier, more-than-622-Mbps data-transfer rate per differential I/O, DDR and DDR2 support as fast as 400 Mbps, as many as 25,344 logic cells, as many as 502 single-ended I/Os, as many as 227 differential-I/O pairs, as many as 32 multipliers
Spartan-3AN platform	The nonvolatile Spartan-3AN platform targets applications requiring nonvolatile system integration, security, or large amounts of user-accessible flash.	50,000 to 1.4 million system gates	270-MHz block RAM, 280-MHz multiplier, more-than-622-Mbps data-transfer rate per differential I/O, 66-MHz PCI, DDR and DDR2 support as fast as 400 Mbps, 5- to 320-MHz DCM (digital-clock-manager) input frequency, as many as 25,344 logic cells, as many as 502 single-ended I/Os, as many as 227 differential-I/O pairs, as many as 32 multipliers
Spartan-3A DSP platform	The Spartan-3A DSP platform targets digital-signal processing in applications requiring integrated DSP MAC (multiply/accumulate) operations and expanded memory.	1.8 million to 3.4 million system gates	270-MHz block RAM, 287-MHz DSP48A/multiplier, more-than-622-Mbps data-transfer rate per differential I/O, DDR and DDR2 support as fast as 333 Mbps, as many as 53,712 logic cells, as many as 519 single-ended I/Os, as many as 227 differential-I/O pairs, as many as 126 DSP48A slices (advanced multiply/accumulate elements) or 126 18×18-bit multipliers

	18×18-bit multipliers, 18-kbit block RAM, DCMs (digital-clock managers), advanced-I/O block with DDR registers, 18 differential- and single-ended standards, differential termination, multiboot-configuration logic	As much as 648 kbits of block RAM, as much as 231 kbits of distributed RAM	SRAM	16.8- to 111.5-mA typical quiescent current	XC3S100E: \$1.75 (250,000)
	Device DNA, 18×18-bit multipliers, 18-kbit block RAM, DCMs (digital-clock managers), advanced-I/O block with DDR registers, 26 differential- and single-ended standards, differential termination, power-management modes, multiboot-configuration logic with watchdog timer	As much as 576 kbits of block RAM, as much as 176 kbits of distributed RAM	SRAM	0-mA quiescent current in hibernation mode, 7.7- to 48.3-mA typical quiescent current, 4.6- to 29-mA typical quiescent current in suspend mode	XC3S200A: \$4.25 (250,000)
	Device DNA, 18×18-bit multipliers, 18-kbit block RAM, DCMs (digital-clock managers), advanced-I/O block with DDR registers, 26 differential- and single-ended standards, differential termination, power-management modes, multiboot-configuration logic with watchdog timer	As much as 11 Mbits of non-volatile, user-accessible flash; as much as 576 kbits of block RAM; as much as 176 kbits of distributed RAM	SRAM plus flash on system in package	0-mA quiescent current in hibernation mode, 7.8- to 48.4-mA typical quiescent current, 4.6- to 29-mA typical quiescent current in suspend mode	XC-3S200AN: \$4.90 (250,000)
	Device DNA, DSP48A slices (advanced multiply/accumulate elements), 18-kbit block RAM, DCMs (digital-clock managers), advanced-I/O block with DDR registers, 24 differential- and single-ended standards, differential termination, power-management modes, multiboot-configuration logic with watchdog timer	As much as 2268 kbits of block RAM, as much as 373 kbits of distributed RAM	SRAM	0-mA quiescent current in hibernation mode, 83.2- to 135.2-mA typical quiescent current, 49.8- to 81.1-mA typical quiescent current in suspend mode	XC-3SD3400A: \$44.95 (25,000)