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DIs Inside

98 Circuit for measuring motor speed uses low-cost components

100 Battery monitor also enables constant-power-boost converter

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Gain-of-two sample-and-hold amplifier uses no external resistors

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When you need to simultaneously sample a signal and amplify the signal level, you can cascade a common gain-of-one sample-and-hold amplifier and an amplifier with a voltage gain of one. With some exceptions, such an amplifier has two external resistors (**Reference 1**). These resistors dissipate power even at the steady state of the sample-and-hold amplifier. In monolithic ICs, power dissipation and the consequent generation of heat from resistors are not the only items in the list of the drawbacks of external resistors. Integrating precise resistors within a silicon chip requires more processing steps, because such resistors are thin-film NiCr (nickel-chromium) or SiCr (silicon-chromium) elements. Manufacturers laser-trim these resistors to a tight tolerance value, contributing to the cost of an IC. Because these resistors occupy more chip area than standard signal-processing transistors,

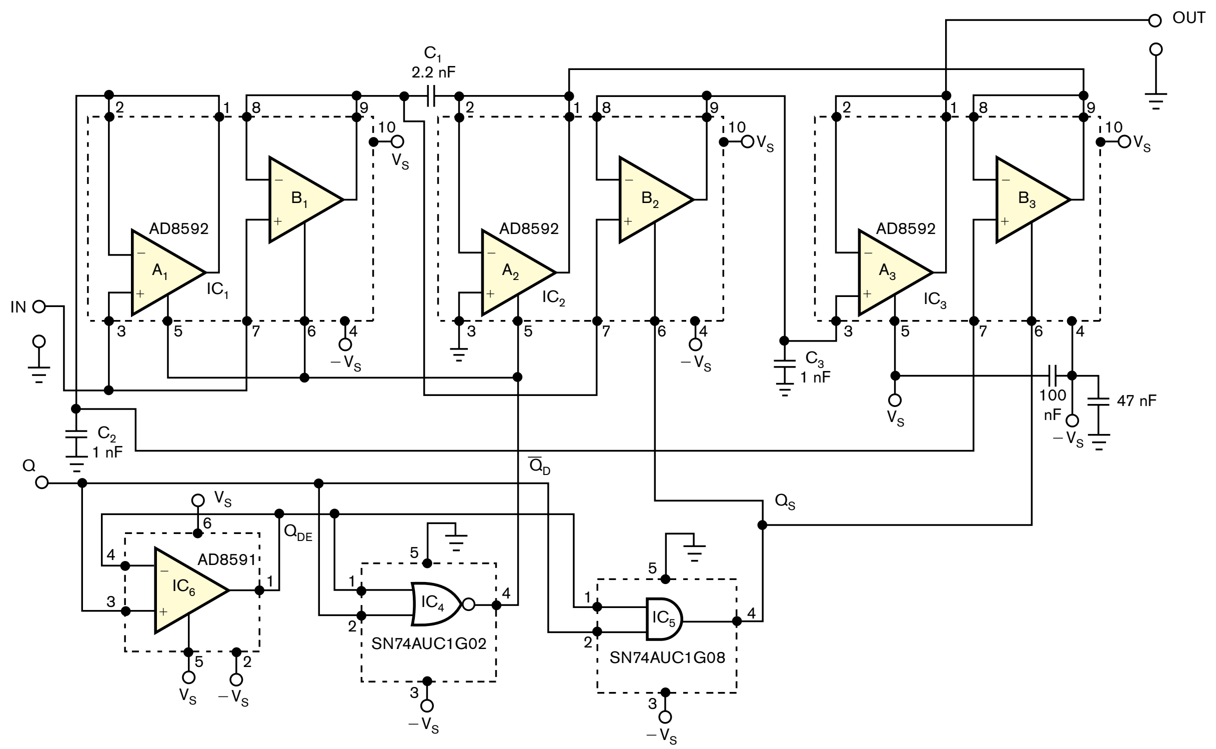

Figure 1 This sample-and-hold amplifier achieves a voltage gain of two by simultaneously tracking the input voltage on capacitors C_1 and C_2, “stacking” these capacitors within the sample interval, and storing the value of the stack’s voltage in capacitor C_3.

the chip must be larger, further increasing the final cost. It's no wonder that designers of monolithic ICs as much as possible avoid using precision resistors.

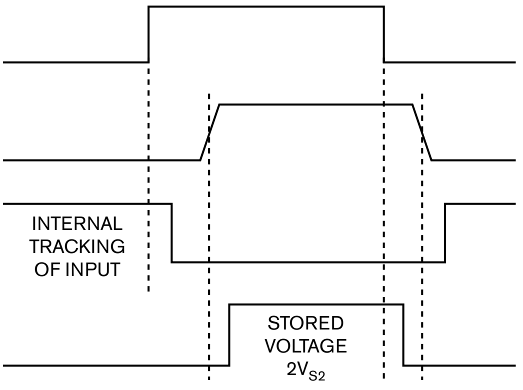

Figure 2 The external-control-logic signal, Q, splits into two quasicomplementary signals, Q_S and $\overline{Q}_D$, to avoid any internal cross-conduction in the amplifier.

If the required voltage-gain of a sample-and-hold amplifier is an integer, which it is in most cases, you can use an alternative way of increasing the magnitude of the output signal. For a voltage gain, G, the circuit can simultaneously track input voltage, V_{IN}, on temporarily ground-referenced tracking capacitors. Subsequently, an interruption occurs in tracking and cancels the ground referencing of $G-1$ of these capacitors. Meanwhile, the tracking capacitors stack on top of each other. The voltage on the stack is the sum of voltages of all of these capacitors, and it thus has the value of GV_{IN}. Upon the sample command, the constant voltage of GV_{IN} gets stored in the $G+1$ ground-referenced storing capacitor.

Figure 1 shows an example of a sample-and-hold amplifier with a voltage gain of two. Voltage followers control the potentials on capacitors C_1, C_2, and C_3 using their shutdown function. The design uses Analog Devices' (www.analog.com) AD8592 dual op amps because their output-leakage current in shutdown mode can be lower than 10 pA (**Reference 2**). You can follow the operation of the sample-and-hold amplifier with the timing diagram (**Figure 2**). The external logic-control signal, Q_S, is at a low level, and the C_1 and C_2 capacitors simultaneously track the voltage at its input. The shutdown inputs of followers A_1, B_1, and A_2 are tied together. At $\overline{Q}_D$=high, they are enabled, so the input voltage appears at the outputs of A_1 and B_1, and no voltage appears at the output of A_2. After the high-to-low transition of $\overline{Q}_D$, a dead slot follows with each of the controlled followers turning off. At Q=high, B_3 and B_2 turn on. Thus, the voltage in C_2 appears at the output of B_3. The potential of the input voltage occurs, therefore, at the lower node of C_1 (Pin 2 of IC_2). Because C_1's voltage has the same value as the input voltage and the output voltage, the B_2 follower is $2V_{IN}$. Capacitor C_3 thus charges to the voltage of $2V_{IN}$. After the high-to-low transition of Q_S, another dead slot follows to prevent any cross-conduction in the circuit. At the next high-to-low transition of Q_S, the process repeats.

The A_3 follower serves as an impedance converter, outputting the voltage in C_3. The single NOR and AND gates, together with op amp IC_6 functioning as a delay line, modify the single external-logic-control signal to create the properly timed internal logic signals, $\overline{Q}_D$ and Q_S.

For a noise analysis, assume that the noise characteristics of each of the followers are the same—namely, the standard deviation, σ_A, of the random component of the output voltage of a single follower. At the end of the tracking interval, both C_1 and C_2 charge to the input voltage. The standard deviation of the V_{C2} voltage is σ_A only for the A_1 follower. The standard deviation of V_{C1} voltage is, however, $\sqrt{2}\sigma_A$, because C_1 charges through two series-configured followers, B_1 and A_2. The standard deviation of $V_{C1}+V_{C2}$ voltage thus has the value of $\sqrt{3}\sigma_A$. The voltage of $V_{C1}+V_{C2}$ applies to C_3 through two followers in a cascade, B_3 and B_2, within the sample interval. Further, the V_{C3} voltage applies to the output through the A_3 follower. Because all of the noise sources are mutually independent and because they all effectively act in series, the standard deviation of the output voltage is $\sigma_{OUT}=\sqrt{6}\sigma_A$. Increasing the integer gain to the value of G yields $\sqrt{3G}\sigma_A$. You now pose an RSNR (relative signal-to-noise ratio) as gain, G, over a relative increment of noise at the output, yielding:

$$RSNR=\frac{G}{\dfrac{\sigma_{OUT}}{\sigma_A}}=\sqrt{\frac{G}{3}}.$$

For the sample-and-hold amplifier in **Figure 1**, the RSNR equals 0.8165, meaning that the noise characteristics of the circuit are slightly worse than those of a single follower. For a gain of three, the RSNR has the value of one, and, starting from a gain of four, at which the RSNR is 1.155, it gradually rises with increasing gain. The conclusion is that, for voltage gains of four or higher, the noise characteristics of the sample-and-hold amplifier are better than those of a single follower. EDN

IT'S NO WONDER THAT DESIGNERS OF MONOLITHIC ICs AS MUCH AS POSSIBLE AVOID USING PRECISION RESISTORS.

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Circuit for measuring motor speed uses low-cost components

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This Design Idea uses a microcontroller, a 16×2-key LCD, and a rotary encoder to measure and visualize the speed of a motor (**Figure 1**). You measure the rotor speed of the motor using an incremental encoder coupled to the motor shaft, which provides quadrature pulses with a frequency proportional to the rotor speed. The 1024-pulse rotary encoder is the RS-32-0/1024ER.11KB from Hengstler (www.hengstler.com). You can calculate the rotational speed of the motor, ω_R, by counting the number of revolutions that the encoder axis, n_V, makes during a certain time period, t_P. You calculate n_V by counting the number of pulses, n_P, that the encoder generates during this fixed period, t_P: $n_V=n_P/1024$ for this encoder. And the rotational speed is

$$\omega_R = \frac{60\times n_V}{t_P} = \frac{60\times n_P}{t_P\times 1024} = \delta\times n_P,$$

where $\delta=60/(t_P\times 1024)$ rpm represents the resolution of the measured speed. To obtain a resolution of 1 rpm for this application, the fixed period you use as a timebase is 60/1024=58.59 msec. In this Design Idea, a low-cost microcontroller, the PIC16F873, IC_1, from Microchip (www.microchip.com) performs these operations. This microcontroller also drives the LCD, IC_2, which shows the rotational speed in rotations per minute.

In a similar fashion to the circuit in **Reference 1**, you apply the quadrature pulses of the encoder to IC_1's RB0/INT input, which generates a high-priority interrupt at the rising edge of the pulse. These interruptions allow you to compute n_P by increasing a counter, which initializes after it reaches fixed period t_P. Moreover, the microcontroller's internal 8-bit timer, Timer 0, registers t_P, which generates a t_M (timer interruption) each 286 μsec for a clock frequency, f_{CLK}, of 14.3 MHz: $t_M=4\times 2^8/f_{CLK}/4=286$ μsec. This calculation means that fixing the timebase, t_P, requires 205 timer interruptions (t_P/t_M).

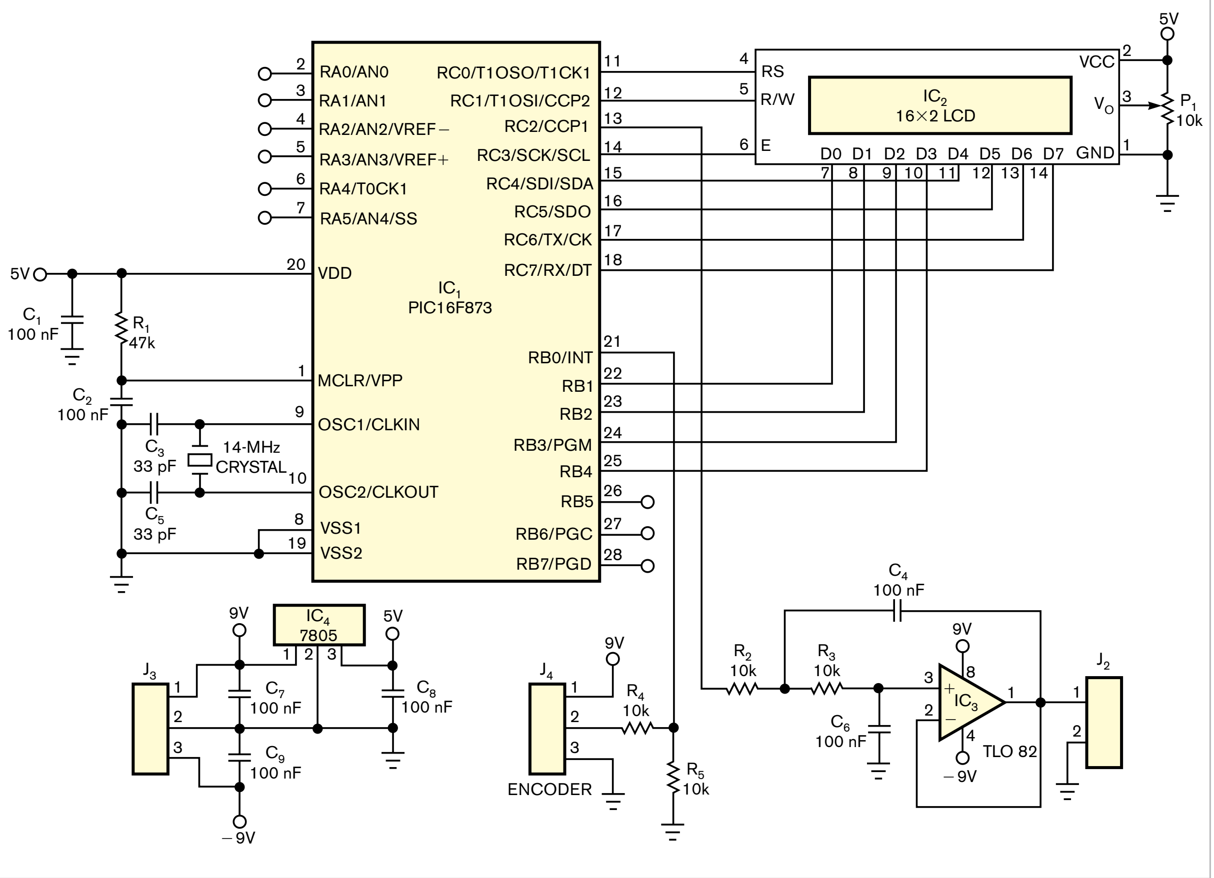

Figure 1 This circuit for measuring a motor's speed includes a PIC microcontroller and an LCD. It also provides an analog-to-digital conversion without an ADC.

When the counter reaches this time, the count, n_P, determines the rotational speed, according to the **equation**. Finally, this value appears on the screen of the LCD.

In addition, a digital-to-analog conversion is necessary if the control system must measure the rotational speed. You can do this conversion without adding an expensive DAC by applying a PWM (pulse-width-modulation) output of the microcontroller to a lowpass filter comprising R_2, R_3, C_4, C_6, and IC_3. The frequency of the PWM signal is 20 kHz, and the cutoff frequency of the lowpass filter is 160 Hz, which is much lower than the PWM frequency. In this design, the maximum duty cycle of the PWM signal corresponds to a rotational speed of 1500 rpm.

You can download the source code for IC_1's program from the online version of this Design Idea at www.edn.com/071108di1 and assemble the software with MPLab from www.microchip.com. You can alter constants within the software according to the encoder you use and your required resolution from the **equation**. **EDN**

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Battery monitor also enables constant-power-boost converter

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Some microcontrollers permit operation below a supply voltage of 3V. This feature allows powering directly from a 3V alkaline or lithium battery without the voltage drop and leakage current of a regulator. It is important to monitor the battery voltage to ensure system integrity, and you can also use this information for system purposes. The circuit in this Design Idea maintains constant power to a white-LED-display backlight by adjusting the duty cycle of a boost-power converter. However, an ADC normally needs a fixed voltage reference (**Figure 1**), which would require two input pins for this function. This Design Idea turns the ADC's architecture inside out, providing the voltage-reference function using no extra pins.

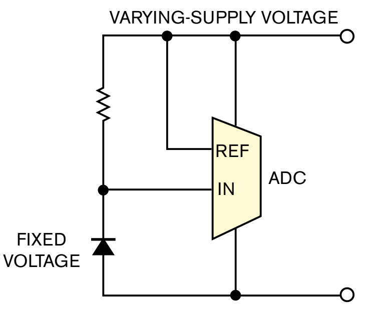

Figure 1 An ADC normally needs a fixed voltage reference, which would require two input pins for this function.

The monitor circuit in **Figure 2** integrates an ADC within the microcontroller. The converter uses the battery voltage as a reference voltage. The principle is the opposite of normal: You want to measure a fixed voltage using a variable-voltage reference (the battery). For an 8-bit converter, the result for this example is $(1.18\text{V}/V_{BAT})\times256$. Note that a high value indicates that the battery voltage is low. Also, you can use the microcomputer pin that connects to the reference for another purpose. This example normally uses Pin 6 as an output to the pulse-indicator LED, LED_1. However, by briefly changing the port direction to analog-input mode, you can complete the battery-measurement operation, including settling, sampling, and conversion, in less than 0.1 msec.

The example uses a PIC12F683 microcontroller and a voltage reference of 1.25V for the LM4041. R_1 biases the reference. R_2 ensures that the microcontroller output can rise to 3V to turn on transistor Q_1 without damag-

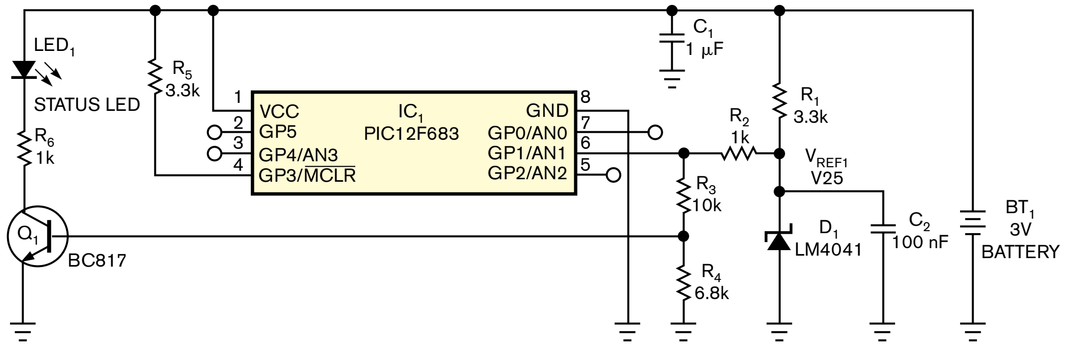

Figure 2 This monitor circuit integrates an ADC within the microcontroller. In this circuit, the converter uses the battery voltage as a reference voltage.

ing D_1. Resistors R_3 and R_4 ensure that the transistor is extinguished during the battery measurement. R_2, R_3, and R_4 introduce some attenuation, which you must take into account.

Figure 3 shows the monitor with the addition of a constant-power voltage-booster circuit. The PWM (pulse-width-modulation) output of the microcontroller drives the converter. For constant power from the booster, the required duty cycle linearly relates to the ADC's converted value.

Battery technologies vary in their discharge characteristics. Alkaline batteries have high capacity but drop their open-circuit voltage as they operate. The open-circuit voltage can provide a good estimate of battery charge. However, alkaline batteries also have internal resistance and exhibit a recovery phase after supplying a heavy load. The resistance increases with low temperature and low battery charge. To determine the battery's state, you can take measurements before and immediately after a high-current load is active. This approach allows estimation of both internal resistance and battery charge. **EDN**

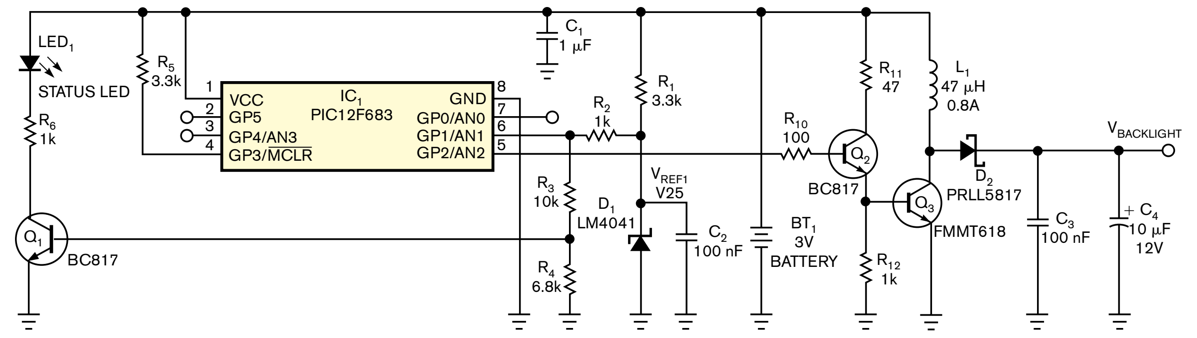

Figure 3 This monitor adds a constant-power voltage-booster circuit. The PWM output of the microcontroller drives the converter.